Operational Simulation of LC Ladder Filter Using VDTA

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In this paper, a systematic approach for implementing operational simulation of LC ladder filter using voltage differencing transconductance amplifier is presented. The proposed filter structure uses only grounded capacitor and possesses electronic tunability. PSPICE simulation using 180nm CMOS technology parameter is carried out to verify the functionality of the presented approach. Experimental verification is also performed through commercially available IC LM13700/NS. Simulations and experimental results are found to be in close agreement with theoretical predictions.

1. Introduction

Current mode approach has received a considerable attention in the last few years for analog signal processing applications due to their low power consumption, large dynamic range, higher frequency ranges of operation, better accuracy, higher slew rate, and less complexity. As a result, a large number of current mode active elements such as operational transconductance amplifier (OTA), current conveyor (CC), current controlled conveyor (CCC), current feedback amplifier (CFA), and operational transresistance amplifier (OTRA), differential voltage current conveyor (DVCC), current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA), and voltage differencing transconductance amplifier (VDTA) are published. A literature review of such analog active block is presented in [1, 2]. The VDTA is a recently proposed analog building block composed of two transconductance amplifiers and may be used to implement different analog processing application such as floating and grounded inductor simulation [3, 4], analog filter [5–10], and oscillators [11–13].

For the active simulation of higher-order LC ladder filter, mainly three methods exist, which are wave active method, topological simulation, and operational simulation. In wave active approach, a wave equivalent is developed for inductor in series branch and then it is configured for other passive components by making suitable connection [14–21]. Large numbers of active blocks are used in this approach. In the second method, topological simulation or element replacement method, the inductor of LC ladder structure is replaced by appropriate configured active elements [22, 23]. The drawback of this configuration is that a floating capacitor is generally required and this degrades the performance of the derived filter topology in high frequency application. In the third approach, operational simulation or leap-frog method [23–30], simulation is carried out for the operation of ladder rather than its component.

Literature survey reveals the operational simulation of ladder filter using operational amplifier (OA) and current controlled conveyor (CCCDI) [24], OTA [25, 26], CC [27], multiple output second generation current controlled conveyor (MO-CCCDI) [28], current feedback amplifier (CFA) [29], and CFOA [30]. This paper presents a systematic approach for operational simulation of LC ladder filter using voltage differencing transconductance amplifier (VDTA). The proposed operational simulation of LC ladder using VDTA has the following advantage over existing circuits:

(i) Lesser numbers of active blocks are used as compared to [24, 26, 28–30].

(ii) There is no use of resistors in realization, while [25, 29, 30] use both floating and grounded resistors and [27] uses only grounded resistors.
Figure 4 can be described by the voltage and current equation as in (3a), (3b), (3c), and (3d) as follows:

\[ I_i = Y_1 (V_{in} - V_2), \]
\[ V_2 = Z_1 (I_1 - I_3), \]
\[ I_3 = Y_2 (V_2 - V_o), \]
\[ V_o = Z_2 (I_3 - I_5); \]

Assume \( I_5 = 0; \)

Then \( V_o = Z_2 I_3, \)

where

\[ Y_1 = \frac{1}{R_s + sL_1}, \]
\[ V_o = \frac{1}{sC_1 + \frac{1}{R_L}}. \]
3.1. Lossy Integration. The implementation of lossy integration using VDTA is shown in Figure 5. The expression for output voltage of lossy integrator can be written as

\[ V_{\text{Out}} = \frac{1}{1 + \frac{s}{\tau}} (V_1 - V_2), \]  

(6a)

where

\[ \tau = \frac{C_V}{g_m} \]  

(6b)

with \( g_{mi} = g_{mo} = g_m \).

3.2. Lossless Integrator. Lossless integrator can be implemented using VDTA as shown in Figure 6 and its output voltage expression is

\[ V_{\text{Out}} = \frac{1}{s\tau} (V_1 - V_2). \]  

(7a)

Again

\[ \tau = \frac{C_V}{g_m} \]  

(7b)

with \( g_{mi} = g_{mo} = g_m \).
3.3. Complete Realization Using VDTA. With the help of lossy and lossless integrator of Figures 5 and 6, the complete realization of prototype 4th-order filter using operational simulation approach is shown in Figure 7.

The value of capacitor used in VDTA 1 and VDTA 4 can be calculated by comparing (6a) and (6b) with (5a) and (5d) as follows.

From (6a) and (6b) and (5a),
\[
\frac{R_s}{R_V} = 1 \implies R_s = R_V. \tag{8}
\]

And \( \tau = C_{V1}/g_m = L_1/R_V \implies C_{V1} = L_1g_m/R_V. \)

Take the value of scaling resistor
\[
R_V = \frac{1}{g_m}. \tag{9}
\]

Then
\[
C_{V1} = L_1g_m^2. \tag{10}
\]

And from (6a) and (6b) and (5d)
\[
\frac{R_V}{R_L} = 1 \implies R_L = R_V, \tag{11}
\]

\[
\tau = C_{V4} = C_4R_V \implies C_{V4} = C_2. \tag{12}
\]

Similarly, the value of capacitor used in VDTA 2 and VDTA 3 can be calculated by comparing (7a) and (7b) with (5b) and (5c) as follows.

From (7a) and (7b) and (5b),
\[
\tau = C_{V2} = C_1R_V \implies C_{V2} = C_1. \tag{13}
\]

And from (7a) and (7b) and (5c),
\[
\tau = C_{V3} = L_2g_m^2 \implies C_{V3} = L_2g_m^2. \tag{14}
\]

4. Simulation

The normalized component values of the prototype filter of Figure 3 are \( R_s = 1, L_1 = 0.7654, C_1 = 1.8485, L_2 = 1.8485, C_2 = 0.7654, \) and \( R_L = 1. \) The aspect ratio of various transistor used in CMOS implementation of VDTA is given in Table 1. The values of supply voltage and bias current for VDTA are \( V_{DD} = V_{SS} = -0.9 \text{ V and } I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150 \mu A \) (\( g_{m1} = g_{m2} = g_{m3} = g_{m4} = 627 \mu S \), respectively.

For cut-off frequency of 5 MHz, the values of capacitor used in Figure 7 can be calculated by (10), (12), (13), and (14) as \( C_{V1} = 15.28 \text{ pF}, C_{V2} = 36.9 \text{ pF}, C_{V3} = 36.9 \text{ pF}, \) and \( C_{V4} = 15.28 \text{ pF}. \) Figure 8 shows the frequency response of the low pass fourth-order Butterworth filter. The simulated cut-off
frequency is 4.99 MHz, which is very close to the theoretical cut-off frequency of 5 MHz. The electronic tunability of the filter through simulation is demonstrated in Figure 9 by varying bias current from 25 $\mu$A to 250 $\mu$A. Time domain analysis is studied by applying two signals of frequency 500 KHz and 20 MHz and of magnitude 50 mV at input. The transient response and its spectrum are shown in Figures 10 and 11, respectively. The proposed filter structure is also tested for total harmonic distortion at output and it is found that it is within acceptable limit of 3% up to 600 mV p-p signal of frequency 1 MHz as shown in Figure 12.

Noise analysis is also carried out for the proposed circuit by determining noise at output of the filter through simulation. The output noise variation within pass band frequencies is depicted in Figure 13 which shows that noise is in acceptable limit of nanovolt range. To examine effect of temperature variation on proposed filter circuit, the circuit is simulated at five different temperatures, 10°C, 25°C, 27°C, 50°C, and 100°C, and the results are depicted in Figure 14. The values of cut-off frequency for these temperatures are listed in Table 2. It is observed that cut-off frequency shifts towards lower frequencies as temperature decreases. This is due to the fact that the transconductance decreases with increases in temperature due to decrease in mobility. This shifting in cut-off frequency can be compensated through bias current.
variation from 104 µA (for $f_0 = 4.17$ MHz at 10°C) to 164 µA (for $f_0 = 5.2$ MHz at 10°C).

All the key parameters of the proposed filter structure are summarized in Table 3. The total power dissipated and output noise in simulation of the prototype filter are 2.16 mW and $5.7 \times 10^{-9}$ V/Hz$^{1/2}$, while simulated values of these parameters for the VDTA implementation of the same-order filter using wave active method are 6.48 mW and $1.65 \times 10^{-8}$ V/Hz$^{1/2}$ [20].

Experimental verification is carried out for proposed circuit through commercially available IC LM13700/NS. The VDTA implementation using IC LM13700/NS is shown in Figure 15. The circuit of Figure 7 is bread-boarded as shown in Figure 16 for experimental testing. Supply voltage of ±15 V is used. The bias current of 1.35 mA is set to obtain the transconductance of 24.89 mA/V. The capacitor values are selected as $C_{v1} = C_{v4} = 10$ nF and $C_{v2} = C_{v3} = 25$ nF for cut-off frequency of 303 kHz. The measured magnitude response along with simulated response is depicted in Figure 17. The experimental cut-off frequency is observed to be 292 kHz.

5. Conclusion

The paper presents a systematic methodology for active implementation of operational simulation of LC ladder filter. To explain the outlined approach, a 4th-order Butterworth
filter is taken as prototype, and, for active implementation, VDTA is used as an analog building block. The proposed implementation is resistorless and uses only grounded capacitors, which is suitable for IC implementation. The proposed structure also possesses electronic tunability of cut-off frequency. Workability of the proposed implementation is verified through PSPICE simulation using 180nm TSMC technology parameters. The functionality of proposed LC ladder is also verified experimentally through IC LM13700/NS.

Competing Interests

The authors declare that they have no competing interests.

References


