Research Article

Reducing the Short Channel Effect of Transistors and Reducing the Size of Analog Circuits

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1. Introduction

While the digital blocks of an integrated circuit continue to shrink (i.e., following Moore’s Law), analog one hardly shrinks at all [1]. As shown in Figure 1, this is particularly right for passive components. For example, to realize an inductance of 1nH, we need more or less 1mm of copper at metal layers and about 10fF/μm² to realize a MIM capacitor. Then, inductor- or capacitor-less designs are good candidates for analog circuits to reduce their size.

LC tanks are the most popular circuits to realize a Voltage Controlled Oscillators (VCO) for wireless applications. On the contrary, ring oscillators (RO, i.e., digital oscillators without passive elements) are known to exhibit high phase noise, but this design will address aggressively the size (only inverters) and power consumption reduction. We have still proposed a new inverter topology to realize a voltage controlled ring oscillator (VCRO) using FDSOI technology [2]. The access to UTBB (Ultra-Thin Body and Box) transistor Back-Gates (BG) offers an extended control of the threshold voltages of the transistors, opening new opportunities to exciting performances. This new complementary structure is based on a pair of BG cross-coupled inverters offering a fully symmetrical operation of complementary signals and will offer two other advantages very important for ring oscillator realization. The first one concerns the duty cycle, which has to be close to 50% and a very low jitter. Secondly, this topology enables a VCRO with an even number of inverters. This latter feature makes it easy to perform a quadrature VCO.

Moreover, due to the Short Channel Effect (SCE), we have to implement longer transistor, especially for analog cell. In this paper, we propose a new topology using some advantages of the FDSOI (Fully Depleted Silicon on Insulator) technology in order to reduce the size of analog cells. First, a current mirror was chosen to illustrate and validate a new design. Measured currents, with 35nm transistor length, have validated our new cross-coupled back-gate topology. Then, a VCRO (Voltage Controlled Ring Oscillator) based on complementary inverter is also used to remove passive components reducing the size of the circuit.
2. **Current Mirror**

2.1. **FDSOI Technology.** MOS bulk transistor is reaching its limits and some scientists have announced the end of the Moore's Law. FDSOI (Fully Depleted Silicon on Insulator) technology, as FinFET, is a solution to continue to follow this law for 22nm node and below [6]. FDSOI technology relies on a thin layer of silicon that is over a Buried Oxide (BOx). Called UTBB (Ultra-Thin Body and BOx), FDSOI transistors are built into the thin silicon layer that is fully depleted of charges and hence provides some unique advantages over bulk. One of the main features of this technology is the possibility of modulating the threshold voltage, $V_{TH}$, using the back-gate (BG) electrode of the transistors, which is particularly efficient in the UTBB-FDSOI technologies where a very thin BOx offers a tighter control. Figure 3 presents the BG contact and Figure 4 gives the influence of the back-gate biasing on the $V_{TH}$ variation [5].

FDSOI is an evolution and compatible with CMOS Bulk technology. If you consider the BG as the Bulk, you have a...
2.2. Basic Implementation of Current Mirror. Figure 5 presents the typical topology of a basic current mirror implemented with PMOS bulk transistors. This current mirror will be implemented to control the oscillation frequency of the RO.

In Figure 5, we can implement Bulk or UTBB transistor if the BG, as the bulk, is connected to the source (i.e., VDD). Figure 6 illustrates the DC simulations of this current mirror with different sizes of transistors with a constant W/L ratio which is equal to 100um/35nm (for the minimum L, red curve) and 1000um/350nm (for the maximum L, blue curve). For all cases, the input current CMin (i.e., Iref) is equal to 45μA, and the two transistors, PA and PB, are identical (same sizes).

These simulations highlight the Short Channel Effect and show that small transistors are definitively unsuitable for this kind of application. The length of the transistor has to be higher than 210nm to assume the behavior of a current generator. To determine this minimum value of L, we have plotted the same simulations with only high values of L, from 105 to 350nm. The third last curves (L=210, 280 or 350nm) are quite identical and correspond to a good current mirror. After |V_DStat|, IDS is very close to a constant which is equal to 45μA.

In this paper, we propose a new topology using some advantages of the FDSOI technology in order to reduce the size of a current mirror. This technology allows realizing new topologies of analog and mixed circuits, offering never reached performances and reducing certain limitations due to the reduction of the channel length [2]. For the current mirror, the aim is to implement very low transistor length, less than 210nm, while maintaining the functionality of a current generator.

2.3. New Design of Current Mirror. Thanks to the characteristic of the threshold voltage of UTBB-FDSOI transistors according to the back-gate biasing, we have already taken into account the benefit of the cross-coupled back-gate auto-biasing to improve the performances of digital cells [2] and the quality of signal generators [8]. We have yet adapted this concept of BG control to a current mirror. As shown in Figure 8, the design principle is as follows: both BG of the two transistors PA and PB are connected to the drain voltages of the other instead source. As VDS of PB increases, the threshold voltage of PA decreases, so we have a smaller bias voltage to get the same input current. At the same time, a smaller bias voltage (i.e., a larger threshold voltage for PB) can reduce the output current, so as to compensate the Short Channel Effect. As the input current is higher than a Bulk transistor, we have used this feature to design new analog or mixed-signal cells.

In addition, more information on this technology has been published in [7]. For example, FDSOI devices are fabricated on substrates with silicon overlayer of 12nm on top of a 25nm BOX.
The simulated results, with $CM_{in}=45\mu A$, are summarized in Figure 9.

First, simulations show that the concept of BG auto-biasing is working for analog cells. The SCE is drastically reduced. Secondly, the response (i.e., the output current) is very sensitive with the length of the transistors; the optimum value is $L=35\text{nm}$.

### 3. Test Chip and Measurement

#### 3.1. Layout and Test Chip. The current mirror is implemented in 28nm FDSOI technology and the layout, with a size of $30\times40\mu m^2$, is given in Figure 10. We have implemented both with and without back-gate control on the same die.

In fact, we have implemented on the same test chip different circuits such as only an inverter, a chain of inverters, a current mirror with (and without back-gate control), and a ring oscillator presented in Section 4. Figure II presents a picture of the die with the Pad ring; the pitch between two pads is equal to 90nm.

#### 3.2. Measurement. As explained before, this current mirror is meant to be embedded in a VCRO and was tested with three different values of current ($CM_{in}=45, 90$ or $180\mu A$). We have implemented both with and without back-gate control.

In the later, the back-gate is connected to $V_{DD}=1\text{V}$, as shown in Figure 5. The sizes of the two transistors are the same for the two configurations with the optimum $L$ value.

The respective measurements, compared with simulations, are depicted in Figures 12 and 13, where the abscissa represents the absolute value of the voltage $V_{DS}(P_B)=V_{out}-V_{DD}$.

In Figures 12 and 13, the solid-line corresponds to the measured results and the dotted-line to the simulations. We can notice some differences of the saturation voltage values between simulations and measurements ($0.1\text{V}$ for simulation and higher value for measurement). However, in the measured saturation region, there is a good agreement between measurement and simulation. We can claim that, using the cross-coupled back-gate auto-biasing technique, there is a stabilization of the current in saturation region with a value equals to $45, 90$, and $180\mu A$ respectively. Using this technique of back-gate control, it is possible to use very small transistor length by reducing drastically the small channel effect, $35\text{nm}$ compared with the minimum value of $210\text{nm}$ (cf. Figure 7).

In conclusion, for this current mirror, it is possible to reduce the size of the two transistors, $P_A$ and $P_B$, by a factor of $6\times6=36$.

### 4. VCRO Design and Measurement

#### 4.1. Complementary Logic and RO. Figure 14 depicts the implementation of a complementary inverter, using the backgate auto-biasing of UTBB transistors [9]. The main idea is as follows: each inverter is controlling through the BG biasing speed of the other one.
If, for some reasons, the speed of the two inverters are not equal, the slowest inverter will decelerate the fastest one and this fastest inverter will accelerate the slowest one, thanks to the cross coupling. So, there is a symmetrization of the two stages (inverters). The complementary outputs are sized to cross at \(V_{DD}\) divided by 2 and finally, we obtain \(t_{PHL} \neq t_{PLH}\) (which are, respectively, the time propagation Low to High and High to Low) and symmetrical output signals.

This new complementary inverter will offer two other advantages very important for ring oscillator realization. The first one concerns the duty cycle, which has to be close to 50% and low jitter [8]. Secondly, this topology enables an oscillator with an even number of inverters (cf. Figure 15). This latter feature makes it easy to perform a quadrature VCO (QVCO): four identical outputs with same amplitude and same frequency but with different phases (0°, 90°, 180°, and 270°). This QVCO topology is used in RF receiver architectures with image frequency rejection.

To validate our concept, we have realized a transient simulation of a 4 fully complementary inverters ring oscillator. The result is shown in Figure 16, where only 2 complementary outputs of an inverter are plotted. The complementary inverters are sized (i.e., PMOS: \(W_p=9.1\mu m\) and \(L_p=30\) nm; NMOS: \(W_N=7.0\mu m\) and \(L_N=39\) nm [9]) to optimize the crossing point at \(V_{DD}\) divided by 2. The simulated period, after layout extraction, is about 1378ps with \(V_{DD}=1\) V, corresponding to an oscillation frequency of 2.64GHz and a power consumption of 5.1mA.
4.2. RO Layout and Measurements. The RO was implemented in 28nm FDSOI technology. Figure 17 illustrates the layout of this 4 complementary inverters RO, with a size of 60×40 μm². The layout has been studied with specific care on the symmetries between each inverter, but also on global symmetry regarding RO outputs using common centroid design.

The test chip measurements, using a probe tester depicted in Figure 18, exhibit an oscillation frequency of 2.14GHz for V_D=1V with a power consumption of 5.9mA.

Figure 19 illustrated the measured complementary outputs of an inverter of the RO. This result exhibits a 190MHz oscillation frequency obtained with V_D=0.5V and a power consumption of 0.25mA (125μW).

Figure 19 shows that the mean value of the duty cycle is equal to 49.67% (very close to 50%). The symmetrization of the two complementary outputs is quite good. However, the output dynamics is limited by V_D, so a level shifter will be needed for the design of the VCRO.

We have modulated the power supply (V_D) to control the oscillation frequency. The tuning range of the oscillation frequency in function of V_D is presented in Figure 20. We can observe a linear part from V_D=0.6V to V_D=1V, corresponding respectively to an oscillation frequency of f_min=480MHz to f_max=2.14GHz. The central frequency f_0=1.3GHz is obtained with V_D=0.8V for a power consumption of 2.88mA (2.3mW). So, we can deduce the gain of the RO: K_VCO=4.3GHz/V. Moreover, this high gain added to the power supply stability and the process variations can explain the frequency difference between measurements and simulations.

For each value of V_D (i.e., oscillation frequency), we have also measured the power consumption, depicted in Figure 21. This result shows that this circuit is very efficient for low frequency application. For example, when V_D=0.5V for a frequency of 190MHz, the power consumption is only 0.25mA, then 125μW.

Then, we have measured the phase noise (PN) and the jitter of the RO working at f_0=1.3GHz with V_D=0.8V. Figure 22 illustrates this jitter measurement; its RMS value (standard deviation) is equal to σ=47ps.

Figure 23 depicts the phase noise and exhibits a value around PN=-84dBc/Hz@1MHz.

Using the complementary logic and the cross-coupled BG topology, the PN is improved compare with a classical RO. However, this PN has to be validated by another measurement. In fact, due to the high value of K_VCO and the variations of the power supply, it was not possible to measure directly the phase noise. The integration of this RO in a VCRO will make this measurement possible and will decrease the PN.

Table 1 gives a comparison of this circuit with two other QVCO topologies (LC tank and RTW) [10]. The figure of Merit is given by the following equation:

\[ FOM = -L(f_m) + 10 \log \left( \frac{f_0}{f_m} \right)^2 T_{\%} - 10 \log \left( \frac{P_{DC}}{1mW} \frac{S}{1mm^2} \right) \]

where f_m is the frequency offset (f_m=1MHz in our case), f_0 the central frequency, L(f_m) the phase noise, P_{DC} the power consumption, S the surface of the VCO, and T% the relative tuning range (T%=tuning range/f_0).

Although a VCRO has higher phase noise compare with LC or RTW VCO, its low power consumption and particularly its very low surface make it a good candidate for some applications (especially at low frequencies) and exhibits a higher FOM.

The next step is to implement this RO in a complete VCO, then a PLL. However, modulating the supply voltage (V_D)
4.3. VCRO Design and Future Work. We have implemented a VCRO using the current mirror studied and measured in Section 3 and the previous RO based on 4 complementary inverters. Figure 24 depicts this circuit. Moreover, as explained before, a level shifter is needed as well as a 50Ω buffer. We can notice that this buffer is realized with a complementary inverter to keep the symmetry of the outputs. The schematic of the complete VCRO is depicted in Figure 25.

The layout of the VCRO is illustrated in Figure 26 and its size is 130×64μm²=0.008mm². The simulated central frequency is 1.2GHz and the tuning range is 1GHz with a $K_{VCO}$ of 5.4GHz/V. These values have to be validated by measurements.

5. Conclusion

Thanks to FDSOI technology, we proposed to implement a novel cross-coupled back-gate technique to improve analog and mixed-signal cells in order to decrease the surface of the integrated circuit. First, this technique was applied to a
current mirror reducing the small channel effect and offering high output impedance. However, the output current is very sensitive to the channel length using the new topology. The new current mirror with back-gate control, i.e., cross-coupled auto-biasing, has been validated by simulations and measurements.

Secondly, we have implemented a ring oscillator based on complementary logic and complementary inverters. We have drastically decreased the surface of such a device, compare with LC or RTW QVCO, as well as the power consumption. The phase noise is always higher, but implementing this RO in a VCRO will improve this feature. The FOM is quite good, and this kind of VCRO is very efficient for low power and low frequency applications. For example, measurements at 385kHz with \( V_{DD}=0.2 \), presented in Figure 27, exhibit a very good quality of the output signal. The power consumption is very low 30\( \mu \)W and the duty cycle is always good with a mean value of 49.67%.

The next step is to combine the current mirror and the RO to implement a complete VCO, then a PLL. We can notice

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**Table 1: Comparison of different topologies.**

<table>
<thead>
<tr>
<th>Technology</th>
<th>RTW VCO</th>
<th>LC QVCO</th>
<th>RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>CMOS 130nm</td>
<td>CMOS 130nm</td>
<td>FDSOI 28nm</td>
</tr>
<tr>
<td>Frequency</td>
<td>11.5GHz</td>
<td>13GHz</td>
<td>1.3GHz</td>
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<tr>
<td>Tuning range</td>
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<td>900MHz</td>
<td>1.7GHz</td>
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<tr>
<td>Consumption</td>
<td>30mW</td>
<td>8mW</td>
<td>2.3mW</td>
</tr>
<tr>
<td>Surface</td>
<td>0.105mm(^2)</td>
<td>0.450mm(^2)</td>
<td>0.0024mm(^2)</td>
</tr>
<tr>
<td>PN@1MHz</td>
<td>-105dBc/Hz</td>
<td>-100dBc/Hz</td>
<td>-84dBc/Hz</td>
</tr>
<tr>
<td>FOM</td>
<td>171dB</td>
<td>165dB</td>
<td>171dB</td>
</tr>
</tbody>
</table>
that the Phase-Frequency Detector, the charge pump, and the divider will be implemented using the complementary logic and the BG control [11].

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

References
