Research Article

Sliding Mode Controller-Based BFCL for Fault Ride-Through Performance Enhancement of DFIG-Based Wind Turbines

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The fault ride-through (FRT) capability and fault current issues are the main challenges in doubly fed induction generator-(DFIG)-based wind turbines (WTs). Application of the bridge-type fault current limiter (BFCL) was recognized as a promising solution to cope with these challenges. This paper proposes a nonlinear sliding mode controller (SMC) for the BFCL to enhance the FRT performance of the DFIG-based WT. This controller has robust performance in unpredicted voltage sag level and nonlinear features. Theoretical discussions, power circuit, and nonlinear control consideration of the SMC-based BFCL are conducted, and then, its performance is verified through time-domain simulations in the PSCAD/EMTDC environment. To reduce the chattering phenomenon and decrease the reaching time, it used the exponential reaching law (ERL) for designed SMC. Also, the SMC-based BFCL performance is compared with the conventional and PI controller-based BFCL for both symmetrical and asymmetrical short-circuit faults. Simulation results reveal that the SMC-based BFCL provides better performance compared with the conventional and PI controller-based BFCL to enhance the FRT.

1. Introduction

Due to the increment of energy demand and depletion of fossil fuels, the demand for electric power generations from renewable energy resources (RESs) is gradually growing [1, 2]. The electric power generation from wind energy is growing so quickly, which can be mostly credited to DFIG-based wind turbines (WTs) due to some advantages such as using partial converter ratings (25–30%) of the nominal-rated wind generator, decoupled active and reactive power control, variable speed operation, low cost, and weight [3]. However, under grid fault conditions, the stator current increases due to the direct connection of the DFIG stator windings to the grid. It results in the transient rotor overcurrent and DC-link overvoltage due to magnetically coupling of the stator and rotor circuit. This may lead to damage in the rotor-side converter (RSC) of the DFIG and disconnecting from the grid [4, 5]. This contrasts with the fault ride-through (FRT) requirement. This requirement states that the WT should stay connected when the connecting point voltage remains above limit line 1, as shown Figure 1. Also, in the above limit line 2, all WT should be able to experience a fault without disconnection [6].

In the literature, several approaches including software [7–12] and hardware [13–32] methods have been proposed and documented. The software approaches such as robust control [7], virtual damping flux-based control [8], inductance-emulating control [9], scaled current tracking control [10], and sliding mode control [11, 12] are based on the modification of the RSC control system, which has low cost. They can satisfy the FRT requirements under low voltage sag but cannot guarantee the FRT under severe voltage sag and limiting fault current. Therefore, it is necessary to apply hardware approaches to meet the FRT requirements under severe voltage sag [13, 14].
In the literature, several hardware schemes such as application of the static synchronous compensator (STATCOM) [15], dynamic voltage restorer (DVR) [16, 17], unified interphase power controller (UIPC) [18], series dynamic resistor (SDR) [19, 20], energy storage system (ESS) [21], and fault current limiters (FCLs) [22–33] have been reported and documented. Since the most common cause of voltage drop is short-circuit fault in the downstream of the grid, many researchers are currently studying fault current mitigation techniques to reduce the voltage sag and enhance the WT FRT performance [22–24]. From this perspective, the applications of FCLs are getting more attention to meet the FRT requirements under voltage sag conditions [22–33]. Regarding this background, some studies focus on superconducting-type FCLs (SFCLs) [24–27] and bridge-type FCLs (BFCLs) [28–33]. In [24, 25], the application of the resistive-type SFCL has been suggested for FRT performance enhancement of the DFIG-based WT. In [24], scholars proposed the resistive-type SFCL in the DFIG rotor circuit to mitigate the RSC transient overcurrent and the DC-link overvoltage to meet the FRT. In [26, 27], the active-type SFCL and a flux coupling-type SFCL are proposed to enhance the DFIG FRT performance under grid fault condition. The research results confirm that SFCLs offer a promising solution to meet the FRT requirements of the DFIG-based WTs and are modelled as follows.

2. DFIG-Based Wind Turbine Model

Figure 2(a) shows the schematic diagram of the DFIG-based wind turbine. The wind turbine, drive train, generator model, and its controller are the main parts of the DFIG-based WT and are modelled as follows.

2.1. Aerodynamic Modeling of the Wind Turbine. There are two wind turbine models in the master library of PSCAD/EMTDC software. In this study, the mode 2 wind turbine model is used. In this model, the captured mechanical power is expressed by the following equation [34]:

\[ P_m = 0.5 \pi \rho R^2 C_p(\lambda, \beta)V_w, \]

where \( \rho \), \( R \), and \( V_w \) represent the air density, radius of blades, and wind speed, respectively. \( C_p \) is the power coefficient and is expressed by

\[ C_p(\lambda, \beta) = 0.22\left(\frac{116}{\lambda} - 0.4\beta - 5\right) e^{-12.5\lambda}, \]

\[ \lambda_c = \frac{1}{\left((1/(\lambda + 0.08\beta)) - (0.035/((\beta^3 - 1)))\right)}, \]

where \( \lambda \) and \( \beta \) are the tip speed ratio and pitch angle, respectively. Also, the drive train model used in this study is based on the commonly two-mass model [35] as demonstrated in Figure 2(b), which is described by the following:

\[
\begin{bmatrix}
\dot{\omega}_g \\
\dot{\delta}_tg \\
\dot{\omega}_t \\
\dot{\delta}_tg
\end{bmatrix}
= \begin{bmatrix}
\frac{D_{tg}}{2H_g} & \frac{-D_{tg}}{2H_g} & \frac{K_{tg}}{2H_g} \\
\frac{-D_{tg}}{2H_t} & \frac{D_{tg}}{2H_t} & \frac{-K_{tg}}{2H_t} \\
-1 & 0 & 0 \\
0 & \frac{1}{2H_t} & 0
\end{bmatrix}
\begin{bmatrix}
\omega_g \\
\omega_t \\
\delta_{tg} \\
\delta_{tg}
\end{bmatrix}
+ \begin{bmatrix}
-1 \\
0 \\
0 \\
0
\end{bmatrix}
\begin{bmatrix}
T_g \\
T_t \\
0 \\
0
\end{bmatrix},
\]
where $T_t$ and $T_g$ are the mechanical turbine and electromagnetic generator torque, respectively, $H_t$ and $H_g$ are the equivalent turbine-blade and the generator inertia, respectively, $\omega_t$ and $\omega_g$ are the turbine and the generator angular speed, respectively, and $K_{tg}$, $D_{tg}$, and $\delta_{tg}$ are the shaft stiffness, the damping constant, and the angular displacement between two ends of the shaft, respectively [34, 35].

2.2. DFIG Model and Control System. As demonstrated in Figure 2(a), the DFIG consists of the wounded rotor induction generator (WRIG), the rotor-side converter (RSC), DC link, and grid-side converter (GSC). Considering the equivalent circuit of the DFIG as depicted in Figure 2(c) and using the $dq$ synchronous reference frame, the $d-q$ components of the voltage and flux equations of the DFIG are expressed as follows [7]:

Figure 2: (a) Schematic diagram of the DFIG-based wind turbine, (b) two-mass drive train system, and (c) equivalent power circuit of the DFIG and its controller.
\[
V_{dq} = R_i i_{dq} + \frac{d\lambda_{dq}}{dt} - \omega_s \lambda_{dq},
\]

\[
V_{dqr} = R_i i_{dqr} + \frac{d\lambda_{dqr}}{dt} - (\omega_s - \omega_r) \lambda_{dqr},
\]

\[
\lambda_{dq} = L_i i_{dq} + L_m i_{dqr},
\]

\[
\lambda_{dqr} = L_i i_{dqr} + L_m i_{dqr},
\]

where \( L_i = L_a L_m/(L_s + L_m) \) and \( L_r = L_a L_m/(L_r + L_m) \). \( i_{dqs} \) and \( i_{dqr} \) are the \( d-q \) components of the stator and rotor currents. \( \omega_s \) and \( \omega_r \) are the supply and rotor angular frequencies, respectively. Also, the GSC and DC link dynamic equations are expressed as follows:

\[
V_{dq} = V_{dqg} + R_i i_{dqg} + L_g \frac{d\lambda_{dqg}}{dt} + \omega_s L_g i_{dqg},
\]

\[
V_{dqr} = V_{dqr} + R_i i_{dqr} + L_g \frac{d\lambda_{dqr}}{dt} + (\omega_s - \omega_r) \lambda_{dqr},
\]

\[
V_{dc} = P_g - P_r - P_{loss}.
\]

In this case, \( P_g \) and \( Q_g \) are

\[
P_g = \frac{3}{2} (V_{qg} i_{qg} + V_{dq} i_{dq}),
\]

\[
P_r = \frac{3}{2} (V_{qr} i_{qr} + V_{dqr} i_{dqr}).
\]

In addition, the active and reactive output power of the DFIG is defined as follows:

\[
P_S = \frac{3}{2} (V_{qg} i_{qg} + V_{d} i_{d}),
\]

\[
Q_S = \frac{3}{2} (V_{qg} i_{qg} - V_{d} i_{d}).
\]

Figure 2(c) demonstrates the control system of the DFIG under steady-state condition. The main objective of the RSC is controlling the output active power \( (P_r) \) and reactive power \( (Q_r) \) by regulating \( q \)- and \( d \)-axis components of the rotor currents \( (i_{qr} \) and \( i_{dr} \), respectively). To achieve this capability, the GSC regulates the DC link and coupling point voltage in the reference values by controlling the \( q \)- and \( d \)-axis components of the stator currents \( (i_{qs} \) and \( i_{ds} \), respectively.

### 3. SMC-Based BFCL

In [28], the application of the BFCL is proposed to enhance the FRT performance of the wind turbine for the first time. In this structure, the limiting resistor is configured in the DC side of the BFCL. It can control the DC reactor current to regulate the PCC voltage. In this paper, a SMC is implemented to the BFCL to regulate the terminal voltage at the determined value for different voltage sag levels by controlling the DC reactor current. The power circuit, principle operation, and designing of SMC for the BFCL are described as follows.

#### 3.1. BFCL Power Circuit

The power circuit of the BFCL is illustrated in Figure 3. It includes the following elements:

1. A three-phase bridge rectifier including diodes \( D_1-D_6 \)
2. An IGBT switch, which is represented by \( T \) to switch the limiting resistor
3. A DC reactor \( L_D \) to limit the rate of increasing of fault current and \( di/dt \)
4. A limiting resistor \( (R) \)
5. Three single-phase series coupling transformers \( (T_a, T_b, \) and \( T_c) \)

#### 3.2. Principle Operation of the BFCL

Based on the situation of the IGBT switch, two paths, low impedance path (LIP) and high impedance path (HIP), are provided to carry the normal and fault operation mode currents. Figure 3(b) demonstrates the line and DC reactor currents under normal and fault operation modes. The LIP consists of \( L_{D1}r_D \) path to carry the normal operation mode current, and the HIP consists of \( L_{D2}r_D \) path to carry the fault operation mode current. Under the normal operation mode \( (t < t_0) \), the control system of the BFCL closes \( T \). The line current \( (i_d) \) converts to DC current \( (i_d) \) and flows through the LIP. Figure 3(c) demonstrates the DC reactor current path in this mode. In this condition, the BFCL generates some power losses and voltage drop due to the BFCL switches and DC reactor resistance, which are negligible. When a fault occurs, the line current and subsequently the DC reactor current start to increase. Figure 3(c) demonstrates the DC reactor current path in this mode \( (t_0 < t < t_1) \). When the DC reactor current reaches to \( i_{iD} \), the control system of the BFCL opens \( T \) to insert the limiting resistor in the fault path. In this condition \( (t > t_1) \), the HIP carries the line current. When \( V_{PCC} < V_{TH}, T \) is turned on, and the HIP carries the line current. When \( V_{PCC} > V_{TH}, T \) is turned off to force the fault current towards the HIP and limits the fault current.

Figure 4(b) demonstrates the PI control system of the BFCL. In this approach, the PI controller is used to regulate the terminal voltage at the reference value.

#### 3.3. PI and Conventional Controller-Based BFCL

In the conventional control approach of the BFCL, the PCC voltage is used as a control signal. Figure 4(a) demonstrates the conventional control system of the BFCL. Under the steady-state operation of the system \( V_{PCC} > V_{TH}, T \) is turned on, and the HIP carries the line current. When \( V_{PCC} < V_{TH}, T \) is turned off to force the fault current towards the HIP and limits the fault current.

#### 3.4. Design and Implementation of the SMC to the BFCL

In recent years, nonlinear controllers due to their good performances in parametric uncertainties and unmodeled dynamics are extended. One of the main powerful controllers is SMC which has a robust performance for unmodeled and noisy systems [40–43]. Consider the single input-single output system by the following state equation:
Figure 3: (a) Power circuit of the BFCL, (b) BFCL performance under fault condition, and (c) equivalent circuit of the BFCL under normal and fault operation modes.

Figure 4: Different control systems of the BFCL: (a) the conventional voltage control, (b) PI control, and (c) SMC control.
\dot{x} = f(x) + b(x)u,
\end{equation}
where \( x \) and \( u \) are the state variable and system input, respectively. \( f(x) \) and \( b(x) \) are bounded nonlinear functions of state variables. Let \( \bar{x} = x - x_d \) be the trajectory error in state \( x \). The time-varying sliding surface for the system is chosen as
\begin{equation}
    s(x; t) = \left( \frac{d}{dt} + \Lambda \right)^{n-1} \bar{x},
\end{equation}
where \( \Lambda \) is a strictly positive constant and \( n \) is the order of the system. By satisfying the following term, the trajectories of the system are remained in the sliding surface:
\begin{equation}
    \frac{1}{2} \frac{d}{dt} s^2 \leq -\mu|s|,
\end{equation}
where \( \mu \) is strictly positive. The above equation can be rewritten as:
\begin{equation}
    \dot{s} \leq 0.
\end{equation}

According to (17), the reaching time will be as follows:
\begin{equation}
    t_{\text{reach}} \leq \frac{|s(t = 0)|}{\eta},
\end{equation}
where \( t_{\text{reach}} \) is the reaching time. To satisfying (17), generally, \( \dot{s} \) is considered as follows:
\begin{equation}
    \dot{s} = -K \text{sign}(s),
\end{equation}
where \( K \) is the positive constant. In [42], to decrease the reaching time and the chattering phenomenon in the input controller, the variable gain was used which was known as the exponential reaching law (ERL). Hence, according to Firouzi et al. [43], (16) can be rewritten as
\begin{equation}
    \dot{s} = -\frac{K}{D(s)} \text{sign}(s),
\end{equation}
where
\begin{equation}
    D(s) = \alpha + (1 - \alpha)e^{-\beta s},
\end{equation}
where \( 0 < \alpha < 1, 0 < \beta \). Hence, the reaching time will reduce to the following term:
\begin{equation}
    t_{\text{reach}} \leq \frac{1}{K} \left( \alpha |s(t = 0)| + \frac{(1 - \alpha)}{\beta} [1 - e^{-\beta s(t=0)}] \right).
\end{equation}

In order to design the BFCL controller, the average model of the system is used. By using Kirchhoff’s voltage law (KVL) in the DC side of the BFCL circuit, it can be written for each phase the following equation:
\begin{equation}
    V_d = R_d i_d + L_d \dot{i}_d,
\end{equation}
where \( i_d \) is the reactor DC current, \( V_d \) is the DC side voltage. It should be noted that the value of \( R_d \) can be varied by the value of the modulation index \( M_i \). Hence, \( M_i \) can be defined as follows:
\begin{equation}
    M_i = \frac{R_d}{\bar{R}}.
\end{equation}

By inserting (25) in (24), (24) can be rewritten as follows:
\begin{equation}
    \dot{i}_d = \frac{1}{L_d} (V_d - M_i R_d i_d).
\end{equation}

The sliding surface of the DC-link current of the BFCL is defined as
\begin{equation}
    s = i_d^{\text{ref}} - i_d.
\end{equation}

By taking the time derivative of (27), it becomes
\begin{equation}
    \dot{s} = i_d^{\text{ref}} - \dot{i}_d.
\end{equation}

To eliminate the tracking error, the sliding surface and time derivative of it must be zero. Hence, it can be written as
\begin{equation}
    M_i = \frac{V_d^{\text{ref}} L_D}{R_d} - \frac{K}{D(s)} \text{sign}(s).
\end{equation}

Stability proof: to prove the stability of the controller, (14) should be satisfied. Hence, by using (27)–(29), (14) will be satisfied as follows:
\begin{equation}
    -\frac{K}{D(s)} \text{sign}(s)s \leq 0.
\end{equation}

It shows that the designed controller is stable. To provide the \( T \) gate signal, the modulation index \( M_i \) obtained from (29) is compared with the triangular signal. The triangular frequency is set to be 1 kHz as shown in Figure 4(c).

3.5. DC Reactor Design. The main purpose of using the DC reactor in the BFCL circuit is limiting the rate of increase of fault current before fault detection time. The cost and inductance of the DC reactor are decisive factors. High value of the DC reactor inductance results in high power losses and cost, which are not acceptable. However, the inductance value of the DC reactor should be sufficient to achieve this purpose. Considering Figure 3(c), which presents the equivalent circuit during \( t_0 < t < t_1 \) time, the DC reactor current is approximately given by the following equation:
\begin{equation}
    V_D = ri + L \frac{di}{dt},
\end{equation}
where \( r = r_f \) and \( L = L_f \). Considering \( (t_1 - t_0) \) as the necessary time for increasing fault current from \( I_0 \) to \( i_1 \) and solving (31), the inductance value of the DC reactor is obtained by the following equation:
\begin{equation}
    L_D = \frac{r_d}{(t_1 - t_0)} \ln \left( \frac{V_D - r_i_0}{V_D - r_i_1} \right).
\end{equation}

\( V_D \) is the mean value of the source voltage on the DC side of the bridge circuit and is approximately as follows:
\begin{equation}
    V_D = \frac{3\sqrt{3}AV_m}{\pi},
\end{equation}
where \( V_m \) is the magnitude of the source voltage. Furthermore, by determining \( t_1 \) and \( t_1 \), the DC reactor inductance is designed.
3.6. Limiting Resistance Design. When a fault occurs, the BFCL inserts the limiting resistor \( R_D \) in the fault path to dissipate the excess output active power of the DFIG \( P_G \) during the fault. To make sure the least disturbance reaches to the DFIG during the fault, \( R_D \) should be sufficient to dissipate the active power transferred by the faulted line. Therefore, the active power dissipated by the BFCL \( P_D \) should be equal with \( P_G \) during the fault. \( P_D \) is determined as follows:

\[
P_D = \frac{V_{PCC}^2}{R_D} = P_G.
\]  

(34)

Using (34), the minimum value of \( R_D \) can be derived as follows:

\[
R_D = \frac{V_{PCC}^2}{P_G}.
\]  

(35)

4. Simulation and Discussion

To verify the proposed SMC-based BFCL performance, the system shown in Figure 5 is used. It includes a 2 MW DFIG-based wind turbine, which is connected to the main grid through a step-up 0.7 kV/13.8 kV transformer. Both symmetrical three-line-to-ground (3LG) and asymmetrical single-line-to-ground (SLG) short-circuit faults were applied at the PCC bus to evaluate the capability of the proposed SMC-based BFCL. The simulated system and DFIG parameters are illustrated in Table 1. Both short-circuit faults occur at \( t = 10s \) and continue for 150 ms. \( V_T \) represents the terminal voltage in Figure 5. Simulations were performed for the following cases:

- Case A: using the conventional-controller BFCL
- Case B: using the PI-controller BFCL
- Case C: using the sliding mode controller BFCL

4.1. Symmetrical 3LG Fault Condition. Figure 6 demonstrates the performance of the BFCL for three cases under 3LG fault condition. In this condition, the PCC voltage drops to zero, approximately. As demonstrated in Figure 6(a), the BFCL performances in three cases have the same trend in response to severe voltage sag. However, the SMC-controlled BFCL has the lowest voltage sag and oscillation in the fault period. Figure 6(b) demonstrates the DFIG active power for three cases. In cases A and B, the active power drops to 0.8 pu in the fault period, approximately. Also, it is increased to 1.5 pu after fault clearance in case A. However, it has the lowest fluctuation in case C by using the SMC-controlled BFCL. Figure 6(c) demonstrates the DFIG speed under this condition. It demonstrates the least rotor speed deviation for case C. Figure 6(d) demonstrates the DC link voltage of the DFIG under this condition. It can be seen from this figure that the DC link voltage remains constant during and after fault by using the SMC-controlled BFCL.

4.2. Asymmetrical SLG Fault Condition. Figure 8 demonstrates the performance of the BFCL for three cases under 1LG fault condition. As demonstrated in Figure 8(a), the PCC voltage drops to 0.75 pu for this condition. In case A, the terminal voltage of the DFIG is increased to 1.4 pu in the
Figure 6: WT response under the 3LG fault: (a) DFIG terminal voltage, (b) DFIG active power, (c) DFIG rotor speed, and (d) DC link voltage.

Figure 7: Continued.
end of the fault period. In case B, the PI control of the BFCL cannot control the terminal voltage at the reference value; however, it remains in acceptable voltage level. In case C, by using the SMC-based BFCL, the terminal voltage is controlled at the reference level by controlling the DC reactor current. Figure 8(b) demonstrates the active power of the
DFIG in three cases. As demonstrated in this figure, the active power fluctuation is lowest in the case of using the SMC-based BFCL, which leads to the least rotor speed deviation, as demonstrated in Figure 8(c). Figure 8(d) demonstrates the DC link voltage of the DFIG. It can be seen that the DC link voltage increases to 1.1 pu for scenario A. However, in scenarios B and C, the DC link voltage remains constant.

Figure 9 demonstrates the DFIG stator current for three cases under this condition. In case A, the fault current is lower than the per-fault current due to full insertion of the limiting impedance in the fault path. In cases B and C, the fault current is limited in 0.5 pu; however, the SMC-based BFCL has superior performance under fault condition.

5. Conclusions

In this paper, a sliding mode controller has been designed to control the BFCL for enhancing the FRT capability of the DFIG-based wind turbine under severe and low voltage sag levels. The DC reactor current of the BFCL has been considered as a state variable in the SMC to control the DFIG terminal voltage. Also, to show the efficiency of the proposed SMC-based BFCL, its performance has been compared with the PI- and conventional controller-based BFCL. Based on the PSCAD/EMTDC simulation results, the following points are obtained:

(i) By using the SMC-based BFCL, the DFIG terminal voltage is effectively controlled at the reference value at different voltage sag levels. This subject leads to the lowest DFIG speed and active power deviations under voltage sag conditions.

(ii) The SMC-based BFCL limits the transient fault current in both ends of the fault period.

(iii) The SMC has a robust and efficient performance under uncertainty conditions in comparison with the PI and conventional voltage control.

Data Availability

The PSCAD file data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References


