

Research Article

Single Magnetic Element-Based High Step-Up Converter for Energy Storage and Photovoltaic System with Reduced Device Count

Muhammad Arif,¹ Mohsin Shahzad,¹ Qianmu Li ,^{2,3,4} Jawad Saleem,¹ Muhammad Shamrooz Aslam ,⁵ and Abdul Majid¹

¹Department of Electrical and Computer Engineering, COMSATS University Islamabad, Abbottabad, Pakistan

²School of Cyber Science and Engineering, Nanjing University of Science and Technology, Nanjing 210094, China

³Intelligent Manufacturing Department, Wuyi University, Jiangmen 529020, China

⁴Jiangsu Zhongtian Internet Technology Co., Ltd., Nantong 226463, China

⁵School of Electrical and Information Engineering, Guangxi University of Science and Technology, Liuzhou, China

Correspondence should be addressed to Qianmu Li; qianmu@njust.edu.cn and Muhammad Shamrooz Aslam; shamroz_aslam@njust.edu.cn

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The multiport DC-DC power converter is a prominent area of research in power electronics due to its highly dense design, reduced device count, and high energy efficiency. In this paper, a nonisolated single magnetic element-based high step-up three-port converter for an energy storage system is presented. The proposed converter has two input ports and one output port. The coupled inductor with switched capacitor is used to achieve high voltage gain. The key features of the proposed converter are high conversion gain, low voltage stress, zero voltage switching (ZVS), and zero current switching (ZCS). The detailed theoretical analysis and operation of the converter are elaborated. The energy efficiency of the proposed converter is calculated and compared with the other counterparts. Ansys Maxwell is used for the coupled inductor finite element modeling. To verify the applicability and functionality of proposed converter, a 100 W converter with two inputs (48 V and 96 V) and one output 360 V at 100 kHz is tested in the laboratory.

1. Introduction

The photovoltaic (PV) power generation, owing to its high availability and cleanliness, is rapidly increasing with a total global capacity of 627 GW at the end of year 2019 [1]. The PV generation system can be operated in islanded and grid-connected mode. The islanded PV system is an optimal choice for the remote area electricity generation and distribution. However, the unpredictability of the solar energy and the electric load demand pose a challenge for the broad level exploitation of solar energy. Therefore, the PV framework needs a battery to remunerate these challenges. On the contrary, to produce 220 V AC, the inverter requires input

voltage of 380–400 V on its DC link. As the voltage generated by the PV system is less than 50 V, a step-up converter is required to keep DC link voltage constant. To address the aforementioned challenges, the power electronic converters provide best solution and efficient interface to PV source [2]. Conventionally, a separate unidirectional converter for PV is used along with a battery connected to either side of converter using bidirectional DC-DC converter. This configuration of separate converters for each source increases the system volume and cost at lower system efficiency. Therefore, various multiport converter topologies are reported in literature [3]. A multiport converter is a converter with central controls, inputs/outputs, and bidirectional ports [4]. Using multiport

converter instead of standard single converters builds the system proficiency, improves components execution, and diminishes the volume and cost [2–4].

A special type of multiport converter is the three-port converter (TPC) including a unidirectional port for power source, a bidirectional port for battery system, and the output port. Recent advances and topologies used for the integration of renewable sources are discussed in [5]. There are some challenges that need to be addressed in TPC such as minimum device count, high voltage gain, optimal control for power sharing, and smooth transition between operating modes. As an optimal design of the TPC, it is always desired that the converter should have minimum device count and high conversion gain. In traditional step-up converters, duty cycle is increased to achieve large step-up ratio. Increasing duty cycle beyond certain limit results in increased switching loss. The coupled inductors, transformers, multipliers, and switched capacitors are some of the various techniques used to achieve high voltage gain [5, 6].

Three-port converter topologies are classified as fully isolated [7–11], partly isolated where one of the ports is isolated [12–18], and nonisolated [19–33]. The isolated structures are suitable for the high power and low frequency applications, but efficiency of these structures is usually low. The partly isolated structures are good with prominent features of high power density and efficiency. The non-isolated three-port converter topologies are preferred because of reduced size, cost, and high power density [5]. The nonisolated topologies are more suitable for standalone PV and low voltage distribution and storage system [3–5]. Recent advancements in nonisolated structures are presented in [19–33]. In [19], a series-parallel connection based on the H-bridge nonisolated converter has been proposed. A 10 kW converter having input of 300 V and output of 600 V at a frequency of 20 kHz is discussed. The converter topology can be modified by increasing its gain and reducing the device count. A nonisolated TPC converter using two inductors and switched capacitors and diodes has been proposed in [20]. The converter has comparatively high conversion gain and low voltage stress on the main operating switch. However, the converter has too many components and inductive elements leading to reduced system efficiency. A three-port high gain converter for the HEV's applications has been addressed in [22]. To accomplish high gain, a coupled inductor along with series of the capacitors has been used. However, the topology can further be optimized by reducing the number of device count. In [23], a high gain converter using a Cockcroft–Walton multiplier method has been proposed. The converter has bigger size due to many passive components. In [24], a coupled inductor-based high step-up TPC with high conversion gain for PV integration has been proposed. However, the use of two coupled inductors results in increased size and cost. A soft switching high gain TPC with the merits of soft switching and demerits

of high component count and two coupled inductors is discussed in [25]. A very simple topology of TPC based on the coupled inductor for PV system is given in [26]. The topology used only coupled inductor, and its gain depends on the turn ratio of the coupled inductor. In [27–29], the authors presented modeling and control of a three-port converter for various applications.

To attain high conversion gain, one coupled inductor is used in nonisolated converter topology [30, 31]. A coupled inductor-based high gain converter is better than isolation transformer due to simpler winding structures and lower conduction losses [6]. In [30], a three-port high gain converter using a coupled inductor is introduced. The converter has the merit of high conversion gain, reduced voltage stress on the main operating switch, and soft switching. However, the converter has a coupled inductor and single inductor which increases its size. A coupled inductor with series capacitor-based high gain TPC with comparatively reduced device count and only one magnetic element has been proposed in [31]. This topology can be further improved by minimizing the device count and better design of the magnetic element. Most of the topologies reported in the literature are switched at less than 100 kHz. The switching frequency of these converter topologies can be increased and control schemes can be improved.

In this paper, a three-port bidirectional converter using one coupled inductor and switched capacitor is proposed. The switching frequency is increased up to 100 kHz in order to shrink the size, increase power compactness, and improve the dynamic response of the converter. The proposed converter has high conversion gain and soft switching capability for the main operating switches. The analysis of the converter is performed in continuous conduction mode (CCM). The operating principle and corresponding theoretical analyses of the proposed converter in different modes are discussed in detail. The presented work is based on [32, 33], with the following vital modifications and extensions:

- (1) Novel converter topology with reduced device count
- (2) Reduction in size and cost by increasing switching frequency up to 100 kHz
- (3) Finite element modeling of coupled inductor in order to improve the design
- (4) Operation of converter in different modes
- (5) Loss and efficiency analyses
- (6) Development of lab prototype and presentation of measured results

The introduction and comprehensive summary of various converter topologies are presented in Section 1, followed by the operation and analysis of the proposed converter in Section 2. The detailed proposed design and the control scheme are elaborated in Section 3 and 4,

respectively. The experimental results, loss and efficiency analyses, and comparison are given in Section 5. Lastly, the overall work is concluded in Section 6.

2. Operation and Analysis of the Proposed Topology

The proposed converter, comprised of one unidirectional port for PV and two bidirectional ports, is presented in Figure 1. The proposed converter comprises four active switches S_1 , S_2 , S_3 , and S_4 and four diodes D_{pv} , D_b , D_{c2} , and D_c . The proposed converter has three capacitors: clamp capacitor C_1 , switch capacitor C_2 , and output capacitor C_m . The proposed converter structure has only one coupled inductor. The coupled inductor along with switch capacitor C_2 is used to achieve high voltage conversion gain at output port. In order to diminish the voltage stress on the fundamental switch S_1 , the active clamp circuit is used. The primary winding of the coupled inductor is common between the inputs, i.e., battery and PV system. The proposed converter has the bidirectional power flow ability along with intersource power-sharing. The switch S_1 is the main operating switch and remains active most of the time. The switches S_2 and S_3 are used for boost and buck operations, respectively. The switch S_4 is used to control power between the PV and battery system. The converter operation is discussed for single-input single-output (SISO), double-input single-output (DISO), and single-input double-output (SIDO) modes. Large value capacitors are used to maintain constant voltage. The detailed operation of the converter in different operating modes is explained in the following sections.

2.1. Converter Operation in SISO Mode. In SISO mode, there are two modes of operation; buck and boost. In boost operation, the battery/PV provides power to the load, whereas in buck operation, the battery is charged from the DC link capacitor.

2.1.1. Boost Operation. In this mode, the power is transferred to the load either by the battery or from the PV. For a single switching cycle, the converter has five operating states. The theoretical switching waveform and current flow paths in CCM are presented in Figure 2(a). The detailed operation of the converter in five states is illustrated.

State-I [$t_0 \sim t_1$] (Figure 3(a)): this is a very short interval; the switch S_1 is turned on at t_0 , S_2 is on, and the switches S_3 and S_4 are off. The current i_{lk} increases linearly and it is equal to the magnetizing inductance current i_{lm} at time t_1 . The net current passing through the primary side is $(i_{lm} - i_{lk})$. The secondary side current i_{LS} is equal to $(n \times i_{lm} - i_{lk})$ which decreases linearly and is equal to zero at time t_1 . The diodes D_3 , D_b , and D_{pv} are reverse biased.

State-II [$t_1 \sim t_2$] (Figure 3(b)): in this interval, both the switches S_1 and S_2 are on. The current i_{lm} is increasing linearly. The current i_{LS} is also increasing linearly but in opposite direction. As the current direction and voltage

polarity are reversed on both sides of the coupled inductor, the capacitor C_1 is charging the switched capacitor C_2 through the diode D_{c2} . The current i_{dc2} increases until it equals i_{LS} at time t_2 .

State-III [$t_2 \sim t_3$] (Figure 3(c)): at time t_2 , the switch S_1 is turned off. The leakage inductance energy is transferred to the capacitor C_1 . The voltage over the switch S_1 is clamped to V_{ds1} . The currents i_{dc} and i_{dc2} through the diodes D_c and D_{c2} decrease. As this is a very short interval, the current direction and voltage polarities over the coupled inductor remain unchanged.

State-IV [$t_3 \sim t_4$] (Figure 3(d)): for this interval, the switch S_2 is on and the switch S_1 is off. The current direction and the voltage polarities change over the coupled inductor. The diode D_c is forward biased and current i_{dc} decreases. At time t_4 , the current i_{dc} become zero, and the diode D_c is reverse biased.

State-V [$t_4 \sim t_5$] (Figure 3(e)): the switch S_1 is off, whereas switch S_2 is still on. At time t_4 , the diode D_c is turned off. The current direction is the same in both primary and secondary windings of the coupled inductor. The magnetizing current i_{lm} is decreasing. The energy from the battery, magnetizing inductor L_m , and the leakage inductor L_{lk} along with the capacitor C_2 is delivered to the load.

2.1.2. Buck Operation. In SISO mode, the input is main DC link capacitor and the output is battery. The large value DC link capacitor is used. In this mode, the main operating switch is S_3 . The theoretical waveforms for this mode are presented in Figure 2(b). For one complete cycle, the operation the converter is explained for the following time intervals.

State-I [$t_0 \sim t_1$]: this is a very short interval; the switch S_3 is turned on. The magnetizing current i_{lm} and leakage current i_{lk} are decreasing and the switch S_3 is turned on at almost zero current flowing through it.

State-II [$t_1 \sim t_2$] (Figure 4(a)): in this interval, the switch S_3 is on. The coupled inductor magnetizing current i_{lm} is increasing in opposite direction. The current i_{lm} is charging the inductor L_m . The interval ends at time t_2 .

State-III [$t_2 \sim t_3$] (Figure 4(b)): at the end of time t_2 , the switch S_3 is turned off. Initially, current i_{dc} increases abruptly and then becomes zero at time t_3 . This interval ends at t_3 .

State-IV [$t_3 \sim t_4$] (Figure 4(c)): at time t_3 , the diode D_{c2} conducts and switch S_3 is off. The current i_{dc2} increases and becomes zero at time t_4 .

State-V [$t_4 \sim t_5$] (Figure 4(d)): in this interval, the switch S_3 is still off. The magnetizing current i_{lm} charges the battery through the body diode D_1 . This interval ends at time t_5 .

2.2. Converter Operation in DISO Mode. During this mode, the PV power is not enough to fulfill the load requirement.

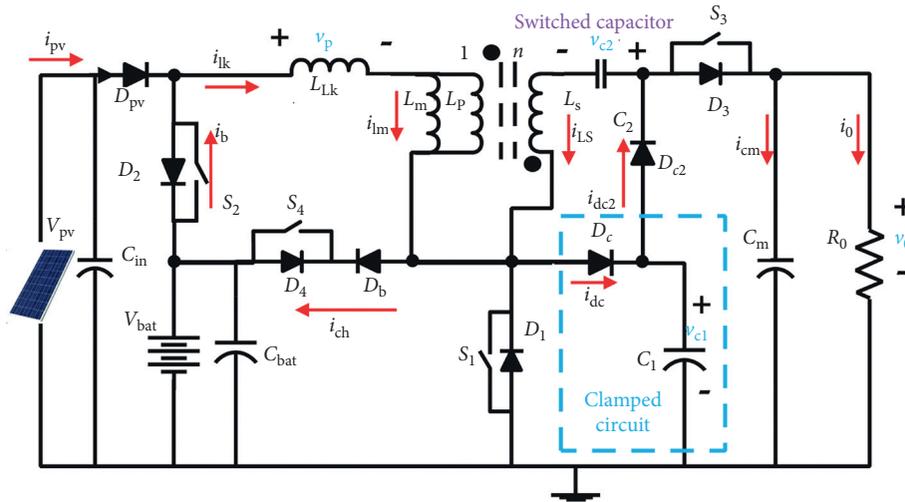


FIGURE 1: Proposed three-port converter.

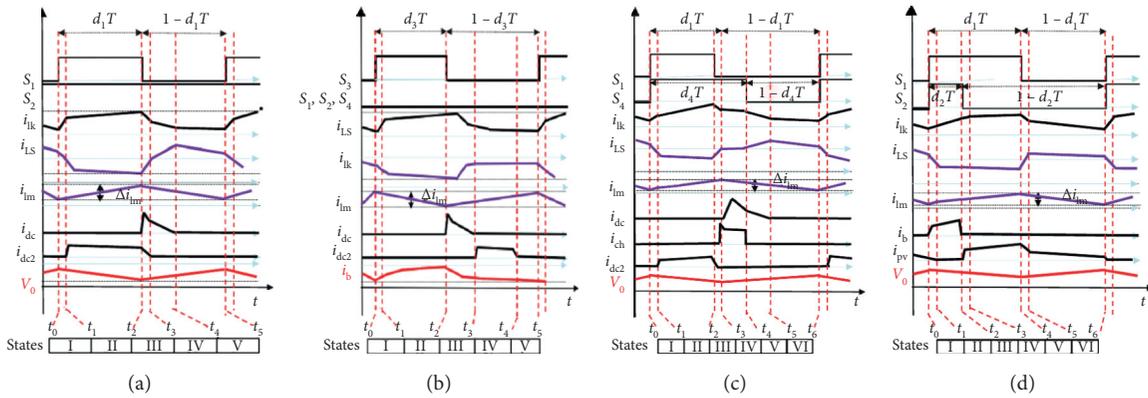


FIGURE 2: Steady-state theoretical waveform. (a) SISO mode (boost operation). (b) SISO mode (buck operation). (c) DISO mode. (d) SIDO mode.

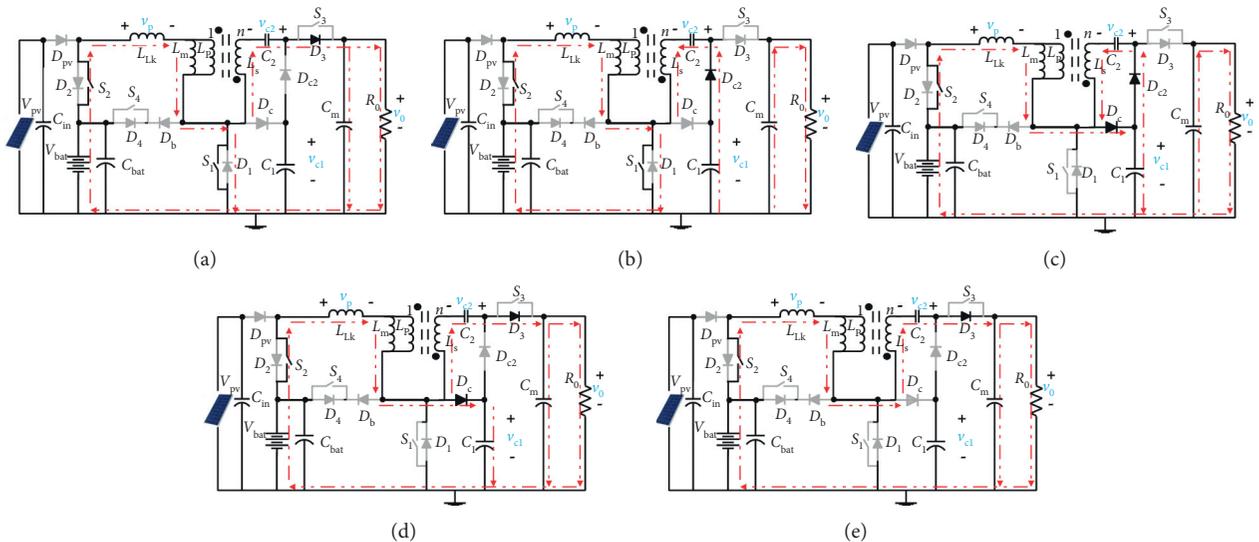


FIGURE 3: Steady-state equivalent circuits and current flow of the converter in SISO mode (boost operation). (a) $t_0 \sim t_1$. (b) $t_1 \sim t_2$. (c) $t_2 \sim t_3$. (d) $t_3 \sim t_4$. (e) $t_4 \sim t_5$.

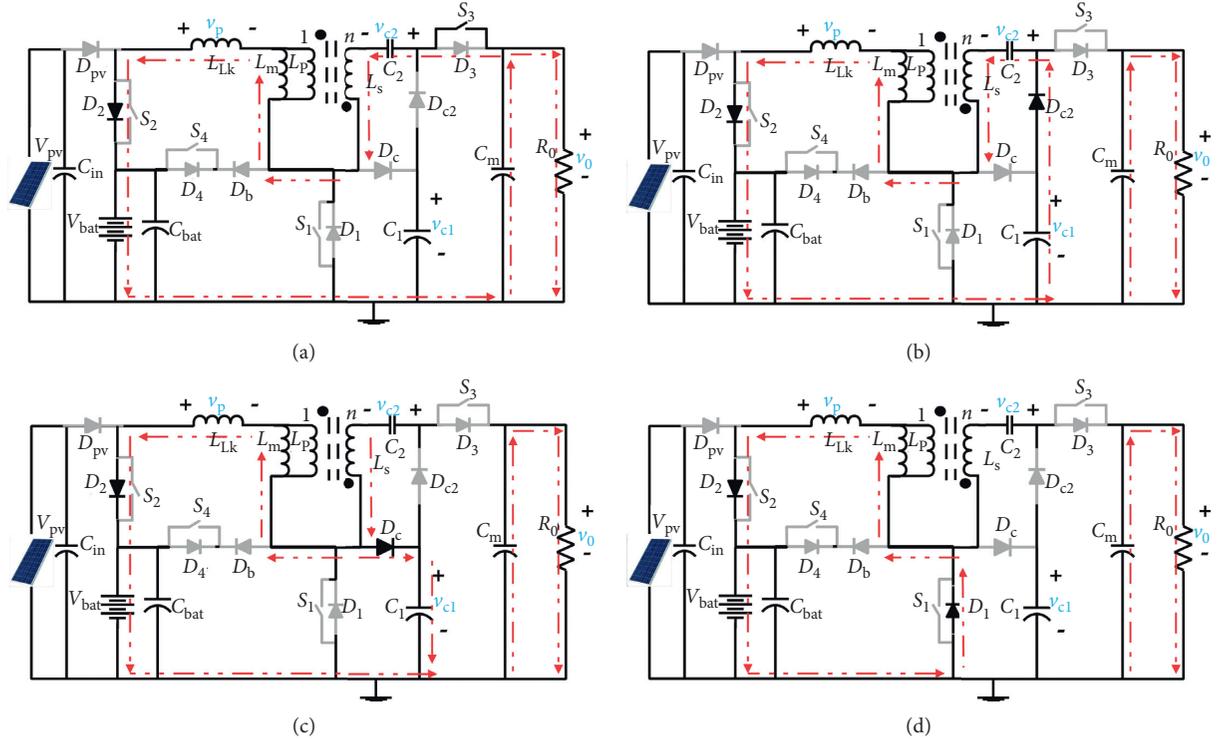


FIGURE 4: Steady-state equivalent circuits and current flow of the converter in SISO mode (buck operation). (a) $t_1 \sim t_2$. (b) $t_2 \sim t_3$. (c) $t_3 \sim t_4$. (d) $t_4 \sim t_5$.

The additional power is supplied to the load from the battery by controlling the switch S_3 . During this dual-input single-output (DISO) mode, both PV and battery provide power to load. The theoretical waveforms and current flow paths are presented in Figures 2(c) and 5, respectively. The operation of the converter during this mode is explained in six states.

State-I [$t_0 \sim t_1$] (Figure 5(a)): at time t_0 , switches S_1 and S_2 are turned on. The leakage current i_{Lk} is almost zero, and the current i_{Ls} is changing its direction. The switches S_1 , and S_2 are turned on under almost zero current. This state is similar to state-I of the SISO mode. All the relationships and equations are same for this state.

State-II [$t_1 \sim t_2$] (Figure 5(b)): this state is similar to state-II of the SISO mode. All the relationships and equations are same for this state.

State-III [$t_2 \sim t_3$] (Figure 5(c)): the switch S_1 is still on while at the end of time t_3 , the switch S_2 is turned off. The diode D_{pv} is forward biased, and the current i_{pv} increases. The current i_b decreases linearly and is zero at time t_3 . The primary voltage of the coupled inductor has been decreased from its previous value.

State-IV [$t_3 \sim t_4$] (Figure 5(d)): in this state, inductor L_m is charged through by the PV source. The switch S_4 is still on and the current i_{lm} increases linearly with a slope of (V_{pv}/L_m) .

State-V [$t_4 \sim t_5$] (Figure 5(e)): at the end of time t_4 , the switch S_1 is turned off and the diode D_c is forward

biased. The voltage V_{ds1} over the switch S_1 clamps to the voltage V_{c1} .

State-VI [$t_6 \sim t_7$] (Figure 5(f)): all the switches are off, PV is delivering power to the load, and voltage V_{pv} is boosted to V_0 . This state is similar to state-V of the SISO mode except the switch S_2 is off and diode D_{pv} is turned on.

2.3. Converter Operation in SIDO Mode. In this mode, the PV generation is greater than the load requirement and excess energy is used to charge the battery. The theoretical switching characteristics are presented in Figure 2(d). The switches S_1 and S_4 are active in this mode. The operation of the converter in different states is discussed as follows.

State-I [$t_0 \sim t_1$] (Figure 6(a)): at time t_0 , the switches S_1 and S_4 are turned on. The current i_{lk} decreases linearly and tends to reach zero, consequently turning on both S_1 and S_4 at ZCS. The operation of the converter in this state is similar to its operation in state-1 of SISO mode.

State-II [$t_1 \sim t_2$] (Figure 6(b)): in this state, the operation of the converter is similar to the operation of state-1 of SISO mode except the source. All relationships and equations are valid for this state.

State-III [$t_2 \sim t_3$] (Figure 6(c)): at time t_2 , the switch S_1 is turned off while the switch S_4 is still on. The current i_{lk} and the magnetizing current i_{lm} decrease linearly. At time t_3 , the current i_{Ls} becomes zero.

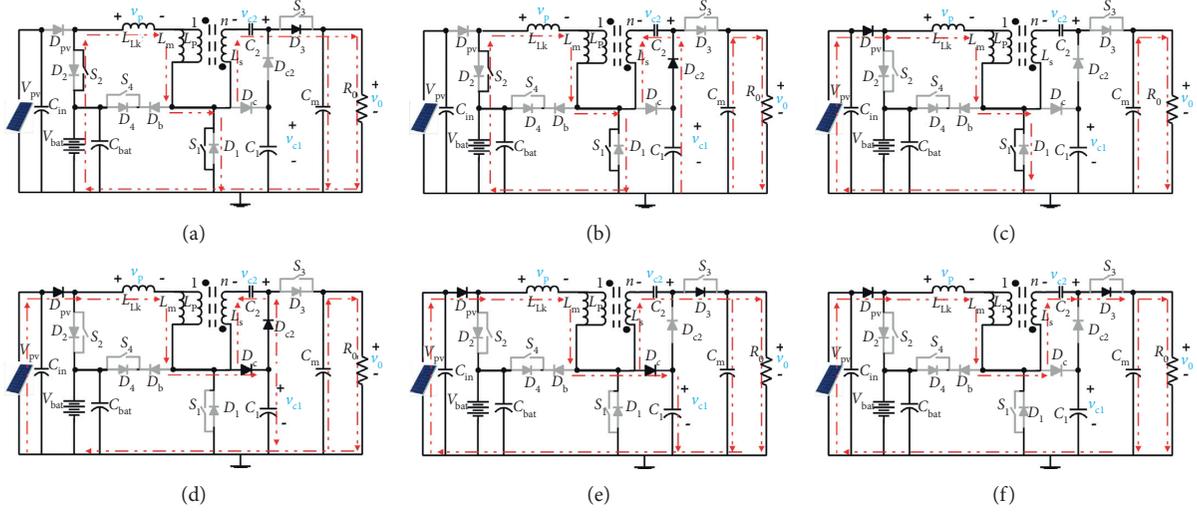


FIGURE 5: Steady-state equivalent circuits and current flow of the converter in DISO mode. (a) $t_0 \sim t_1$. (b) $t_1 \sim t_2$. (c) $t_2 \sim t_3$. (d) $t_3 \sim t_4$. (e) $t_4 \sim t_5$. (f) $t_5 \sim t_6$.

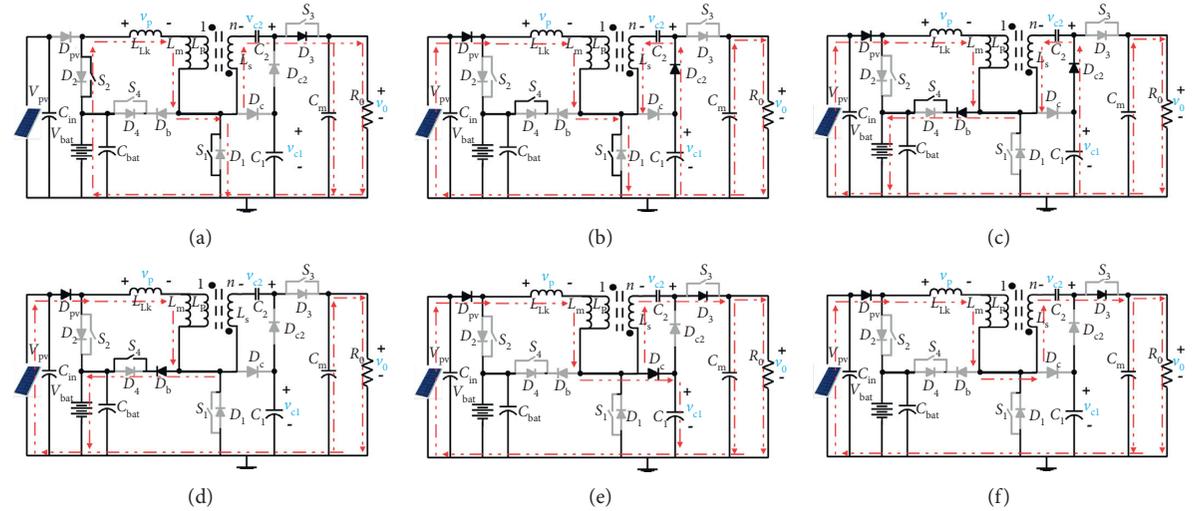


FIGURE 6: Steady-state equivalent circuits and current flow of the converter in SISO mode. (a) $t_0 \sim t_1$. (b) $t_1 \sim t_2$. (c) $t_2 \sim t_3$. (d) $t_3 \sim t_4$. (e) $t_4 \sim t_5$. (f) $t_5 \sim t_6$.

State-IV [$t_3 \sim t_4$] (Figure 6(d)): at time t_3 , the switch S_4 is still on. The leakage i_{lk} and magnetizing i_{lm} currents are equal while the secondary current i_{ls} is zero. The magnetizing current i_{lm} is used to charge the battery through the diode D_b and switch S_4 . The battery charge current i_{ch} is controlled by the duty cycle D_4 . The slope of i_{lm} is equal to $V_{bat} - (V_{pv}/L_m)$. The state ends at time t_4 when the switch S_4 is turned off.

State-V [$t_4 \sim t_5$] (Figure 6(e)): the switches S_1 and S_4 are turned off. The diode D_c conducts, transferring the leakage inductance L_{lk} energy to the clamping capacitor C_1 . This state ends at time t_5 .

State-VI [$t_5 \sim t_6$] (Figure 6(f)): all switches are off. The operation of the converter in this state is similar to

state-V of the SISO mode. The only difference is that the diode D_{pv} conducts and the source is PV. All the relationships and equations are similar to state-V of SISO mode for this state.

3. Steady-State Analysis and Design Considerations

Averaging of the converter in each mode is performed by applying voltage-second balance on magnetizing current i_{lm} equations, whereas the ampere-second method is used on all capacitors' voltage equations. The steady-state analysis results for each mode are elaborated in SISO, DISO, and SISO modes.

3.1. SISO Mode

3.1.1. Boost Operation. By applying the voltage-second balance on the magnetizing inductance L_m , the voltage over the magnetizing inductor is calculated according to the following equation:

$$V_{lm} = d_1 \times \frac{V_{bat}}{1 - d_1}. \quad (1)$$

The voltages across the capacitors C_1 and C_2 are computed according to equations (2) and (3), respectively.

$$V_{C1} = \frac{V_{bat}}{1 - d_1}, \quad (2)$$

$$V_{C2} = (n + 2) \times \frac{V_{bat}}{1 - d_1}. \quad (3)$$

The steady-state voltage across the capacitor C_m is computed by using the following equation:

$$V_{cm} = V_{bat} + V_{Lm} + nV_{Lm} + V_{c2}. \quad (4)$$

The output voltage V_0 across the load is computed by using the following equation:

$$V_0 = \frac{V_{bat} \times (2 + n + d_1(1 + n))}{1 - d_1}. \quad (5)$$

The converter gain increases significantly by increasing the duty cycle and the turn ratio “ n ” of the coupled inductor. Change in the output voltage V_0 with the change in duty cycle d_1 in SISO mode is presented in Figure 7(a). The comparison of output voltage and the input voltage at various values of the turn ratio “ n ” is presented in Figure 7(b). This shows that the output voltage increases linearly with the input voltage. The proposed converter has the gain of 8.

From the analysis, it is observed that for both the inputs (PV and battery), the voltage across the load will remain the same. The switch S_1 is used to control the output voltage for both the inputs PV and battery.

3.1.2. Buck Operation. In this mode, the battery is charged from the main DC link capacitor. The main operating switch is S3. For the steady-state operation in this mode, the voltage-second balance on the magnetizing current i_{lm} is applied. The steady-state voltage, when the battery is charged from the DC link capacitor, is given in the following equation:

$$V_{bat} = \frac{V_{cm} \times d_3}{n + 2}, \quad (6)$$

where $V_{cm} = V_0$.

3.2. DISO Mode. For this mode, the voltage-second balance on the magnetizing inductance is applied. The voltage across the magnetizing inductance is computed by using the following equation:

$$V_{lm} = \frac{V_{pv} \times (d_1 - d_2) + V_{bat} \times d_2}{1 - d_1}. \quad (7)$$

The voltage V_{C1} across the capacitor C_1 is computed by the following equation:

$$V_{c1} = \frac{V_{pv} - d_2 \times V_{pv} + d_2 \times V_{bat}}{1 - d_1}. \quad (8)$$

The voltage V_{C2} across the capacitor C_2 is determined by the following equation:

$$V_{c2} = \frac{V_{pv} \times [1 + nd_1 - d_3(n + 2)] + V_{ch}}{1 - d_1}, \quad (9)$$

where $V_{ch} = V_{bat} [d_2(n + 1) + n(1 - d_1)]$.

The output voltage V_0 across the capacitor C_m is computed by using the following equation:

$$V_0 = V_{pvnew} \times \frac{V_{pv}(d_1 - d_2) + V_{bat} \times d_3}{1 - d_1}, \quad (10)$$

where $V_{pvnew} = 2(V_{pv} + n \times V_{bat} + (2n + 2))$.

3.3. SIDO Mode. For the calculation of conversion ratio, we are applying voltage-second balance. In this mode, the only input is PV. To calculate the conversion ratio, voltage-second balance is applied on the magnetizing inductance L_m . The voltage across L_m is calculated by using the following equation:

$$V_{lm} = \frac{V_{pv} \times d_4 - V_{bat}(d_4 - d_1)}{1 - d_2}. \quad (11)$$

The voltage across the capacitors C_1 , C_2 , and C_m is calculated by using equations (12)–(14), respectively.

$$V_{c1} = \frac{V_{pv} - V_{bat}(d_4 - d_1)}{1 - d_4}, \quad (12)$$

$$V_{c2} = \frac{(n + 2)[V_{pv} - V_{bat}(d_4 - d_1)]}{(1 - d_4)}. \quad (13)$$

The output voltage over the capacitor C_m is calculated by using the following equation:

$$V_0 = \frac{n(3 + d_4)V_{pv} - (3n + 2)(d_4 - d_1)(V_{bat})}{(1 - d_4)}. \quad (14)$$

3.4. Design Consideration. The design specifications of the proposed converter are given in Table 1. The main components used in the converter design are coupled inductor, power MOSFETs, capacitors, and diodes. The appropriate selection of coupled inductor, capacitors, and power semiconductor devices is very crucial for the desired operation of the converter.

3.4.1. Coupled Inductor Design. The required parameters of the coupled inductor used in the converter topology are given in Table 1. The equivalent inductance is

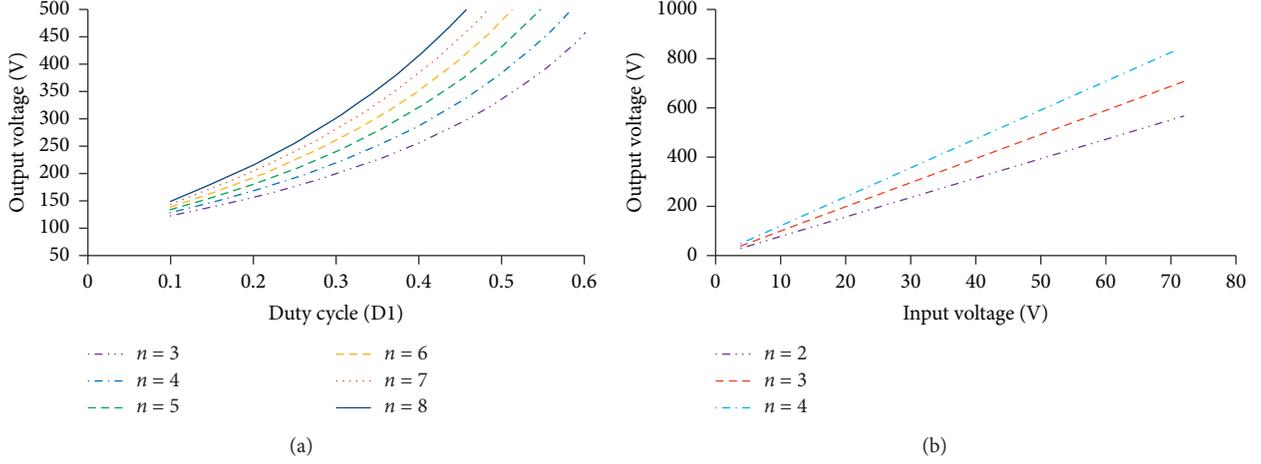


FIGURE 7: (a) Converter output vs duty cycle (d_1) in SISO mode. (b) Output vs input voltage in SISO mode with different values of “ n .”

$L_{eq} = L_p + L_s + 2M$, where M is the mutual inductance. The number of turns for the required inductance value of the L_p is calculated by using equation (15). The required peak inductor current is 6.165 A, and the duty cycle $d_1 = 0.6$. For 100 W, the core ETD-39 and wire AWG-14 are selected. The peak I_{Lpk} primary inductor current is calculated using equation (16). The peak to peak primary inductor current is $2I_{Lp}$. The peak current I_{Dpk} through diode D_3 is calculated by using equation (17). The relationship between I_{Lpk} and I_{out} is expressed in equation (18). The required values of the coupled inductor are $L_p = 5$ uH and $L_s = 20$ uH for DCM operation. For the CCM operation, inductor values are $L_p = 25$ uH and $L_s = 100$ uH.

$$B_{max} = \frac{U_{eff} \cdot U_0 \cdot N_1^2 \cdot I_{max}}{L_e}, \quad (15)$$

where N67 material is used which has the following properties: $U_{eff} = 1590$, $A_c = 97.1$ mm², $L_e = 78.8$ mm, and B_{max} = maximum flux density.

$$I_{Lpk} = \frac{V_{pv}}{L_p \times d_1 T}, \quad (16)$$

$$I_{Dpk} = \frac{V_0 - [(V_{pv}) \times (2 + n) - V_{c2}]}{L_{eq} \times (1 - D_1 T)}, \quad (17)$$

$$I_{Lpk} = \frac{I_{out} \times (2 + n + d_1 (1 + n))}{(1 - d_1)}, \quad (18)$$

$$I_{out} = I_{Dpk} (1 - d_1)^2. \quad (19)$$

The primary inductance value and its losses are calculated by using equations (20) and (21), respectively. The magnetizing inductance can be calculated by using equation (22).

TABLE 1: Parameters' symbols and values/components used for prototype and simulation.

| Parameters | Symbols | Values |
|-------------------------------|-----------------|--------------|
| Input source-1 | V_{pv} | 48 V |
| Battery voltage | V_{bat} | 96 V |
| Output voltage | V_0 | 380 V |
| Primary inductor (DCM) | L_p | 5.01 uH |
| Secondary inductor (DCM) | L_s | 20.043 uH |
| Primary inductor (CCM) | L_p | 25 uH |
| Secondary inductor (CCM) | L_s | 100.043 uH |
| Peak primary inductor current | I_{Lp} | 16 A |
| Load current | I_{Load} | 0.263 A |
| Clamp capacitor | C_1 | 5 uF, 250 V |
| Series capacitor | C_2 | 2 uF, 250 V |
| Series capacitor | C | 2 uF, 250 V |
| Main DC link capacitor | C_m | 300 uF |
| Load resistor | R_{load} | 680 Ω |
| MOSFETs | S_1, S_2, S_3 | FQA34N20 |
| MOSFETs | S_4 | G32N500 |
| Diode | D_c | MBR20200CT |
| Diode | D_{c2} | MUR840 |
| Diode | D_b, D_{pv} | MBR4060PT |
| Switching frequency | f_{req} | 100 kHz |
| Output power | P_0 | 100 W |

$$L_p = \frac{V_{pv}}{(2 + n)^2 \times I_{out} \times d_1 (1 - d_1) T}, \quad (20)$$

$$L_{p\ loss} = R_{ESR} \times \left(\frac{(n + 1)}{(1 - d_1)} \times I_{out} \right)^2, \quad (21)$$

$$L_m = \frac{n \times d_1 \times V_{pv}}{f_s \times \Delta i_{lp}}. \quad (22)$$

The secondary inductor value is calculated by using the relationship $L_s = n^2 \cdot L_p$, where $n = (N_1/N_2) = \sqrt{(L_1/L_2)}$. Here, N_1 is the number of turns on the primary side and N_2 is the number of turns on the secondary side. The coupling coefficient between the primary and secondary inductors is calculated by using equation (23), where as the power loss in secondary inductor is calculated by equation (24).

$$k = \frac{M}{\sqrt{L_p \times L_s}}, \quad (23)$$

$$L_{S\text{loss}} = R_{\text{ESR}} \times \left(\frac{(n+1)}{(1-d_1)} \times I_{\text{out}} \right)^2. \quad (24)$$

The leakage inductance value on the primary side can be calculated by equation (25), where f_r is the resonance frequency and the $C_{\text{out} s1}$ is the output capacitance of the switch S_1 .

$$L_{\text{lk}} = \frac{1}{(2 \cdot \pi f_r)^2} \cdot C_{\text{out} s1}. \quad (25)$$

The finite element model of the coupled inductor is developed in Ansys Maxwell 3D by using PExprt tool. The coupled inductor's Ansys analysis report for both the DCM and CCM operations is given in Tables 2 and 3, respectively. In Table 2, the coupled inductor performance results are shown for the DCM mode. The results show the primary and secondary inductance (L_p and L_s) values of 5 uH and 20 uH, respectively, with turn ratio $n = 2$. The current density is found to be 13.39 (A/mm²) for L_p and 3.58 (A/mm²) for L_s with the losses of 2.4 W and 438.5 mW for L_p and L_s , respectively. The value of R_{dc} is found to be 7.85Ω and 20.14Ω for L_p and L_s , respectively. The total losses for DCM mode are 4.455 W, and window filling is 36.74% and 73.1% for L_p and L_s , respectively. Similarly, the coupled inductor performance results for CCM mode are shown in Table 3. The values of the current density, coupled inductor, losses in primary and secondary windings are shown. The DC resistance value of the used wire is $R_{\text{dc}} = 3.353 \text{ m}\Omega$. Moreover, the losses in the core and winding are expressed as 971.142 mW and 200.684 mW, respectively. Furthermore, the window occupancy for both primary and secondary winding is obtained as 31.09% and 55.72%, respectively.

The finite element model (FEM) of coupled inductor for magnetic flux density is presented in Figure 8(a), whereas the FEM for the magnetic flux lines is presented in Figure 8(b).

3.4.2. Capacitor Selection. Three capacitors used in this topology are the clamping capacitor C_1 , the switched capacitor C_2 , and DC link capacitor C_m . Equation (26) gives the relationship between the clamp capacitor C_1 and the input voltage V_{bat} .

$$V_{c1} = \frac{V_{\text{bat}}}{1-d_1}. \quad (26)$$

TABLE 2: Ansys Maxwell analysis report: coupled inductor performance results (DCM).

| | Primary inductor (L_p) | Secondary inductor (L_s) |
|-------------------------|----------------------------|------------------------------|
| Current density | 13.39 (A/mm ²) | 3.579 (A/mm ²) |
| Inductance | 5.01 uH | 20.043 uH |
| Losses | 2.405 W | 438.504 mW |
| R_{dc} | 7.857Ω | 20.144 mΩ |
| <i>Losses</i> | | |
| Losses (winding) | 3.360 W | |
| Losses (core) | 95.104 mW | |
| Total losses | 4.455 W | |
| <i>Window occupancy</i> | | |
| Window filling (%) | 36.74 | 73.10 |

TABLE 3: Ansys Maxwell analysis report: coupled inductor performance results (CCM).

| | Primary inductor (L_p) | Secondary inductor (L_s) |
|-------------------------|----------------------------|------------------------------|
| Current density | 2.88 (A/mm ²) | 1.22 (A/mm ²) |
| Inductance | 25.00 uH | 100.043 uH |
| Losses | 815.77 mW | 119.917 mW |
| R_{dc} | 3.353 mΩ | 29.379 mΩ |
| <i>Losses</i> | | |
| Losses (winding) | 200.684 mW | |
| Losses (core) | 971.142 mW | |
| Total losses | 1.172 W | |
| <i>Window occupancy</i> | | |
| Window filling (%) | 31.09 | 55.72 |

The blocking voltage over the switch S_1 is expressed in the following equation:

$$V_{\text{DS1}} = \frac{V_{\text{bat}}}{1-d_1}. \quad (27)$$

The minimum value of the capacitors C_1 and C_2 is calculated by using equations (28) and (29), where as the value of the output capacitor C_m is determined by equation (30). The voltage across the capacitor C_2 is determined by equation (31).

$$C_{1\text{min}} \geq \frac{V_{\text{bat}} \times d_1 \cdot T}{2 \times R_{\text{dson1}} \times \Delta V_{c1}}, \quad (28)$$

$$C_{2\text{min}} \geq \frac{V_{c1} \times d_1 \cdot T}{2 \times R_{\text{dson1}} \times \Delta V_{c2}}, \quad (29)$$

$$C_m \geq \frac{V_{\text{pv}} \times d_1 \times T}{2 \times R_{\text{load}} \times \Delta V_{\text{cm}}}, \quad (30)$$

$$V_{c2} = \frac{V_{\text{pv}} \times (-1 + 2 \cdot d_1 + 2 + n)(1 + n(1 - d_1))}{(1 - d_1)}. \quad (31)$$

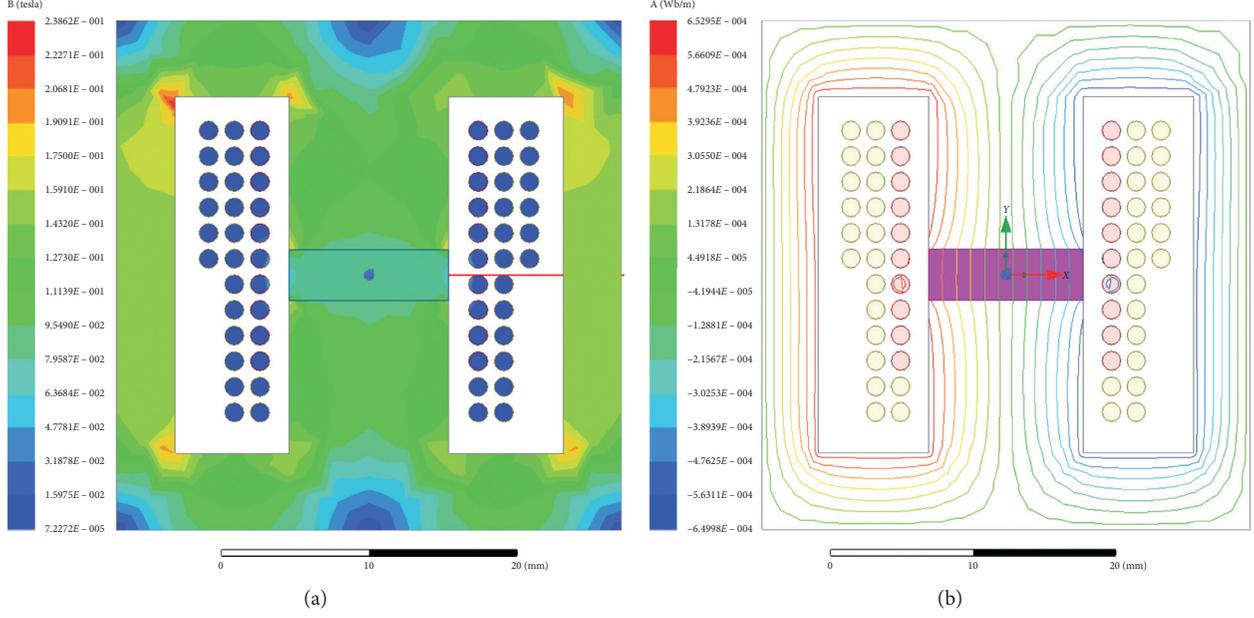


FIGURE 8: FEM. (a) Magnetic flux density. (b) Magnetic flux lines.

3.4.3. Selection of Switches and Diodes. The switches S_1 , S_2 , and S_4 have low voltage blocking capability while switch S_3 has high voltage blocking capability. The maximum voltage stress across the main switch S_1 and the diode D_c is calculated by the following equation:

$$V_{ds1} = \frac{V_{in}}{1 - d_1}, \quad (32)$$

where V_{in} is the input voltage at PV or battery port. The switch S_3 and the diode D_{c2} bear maximum voltage stress, and it can be expressed as follows:

$$V_{ds3} = V_{in} \times \frac{(2 + n + d_1(1 + n))}{(1 - d_1)}. \quad (33)$$

The voltage stress across the switch S_2 and the diode D_{pv} is expressed as follows:

$$V_{ds2} = V_{bat} - (1 + n)V_{lp} + V_{c2} + V_0, \quad (34)$$

whereas the voltage stress across the switch S_4 and the diode D_6 is given as follows:

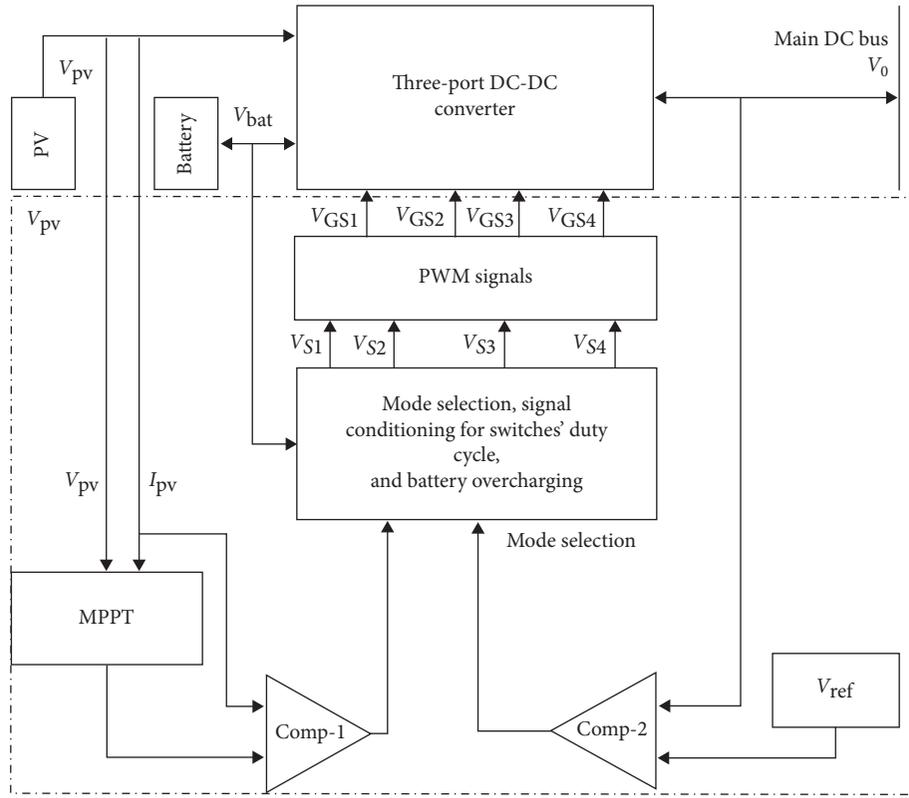
$$V_{ds4} = V_{bat} - (V_{d6} + V_{c1}). \quad (35)$$

The maximum current stress across the switches and diodes of the proposed converter occurs if only one source is serving the load. The current stress on the switches S_1 and S_2 and the diodes D_{pv} and D_c is equal to I_{Lpk} as expressed in equation (18). The current stress on the switch S_3 is equal to I_{Dpk} and is expressed in equation (20). The peak current through the diode D_{c2} is $I_{dp} = (I_{Dpk}/n)$, where I_{Dpk} is expressed in equation (17).

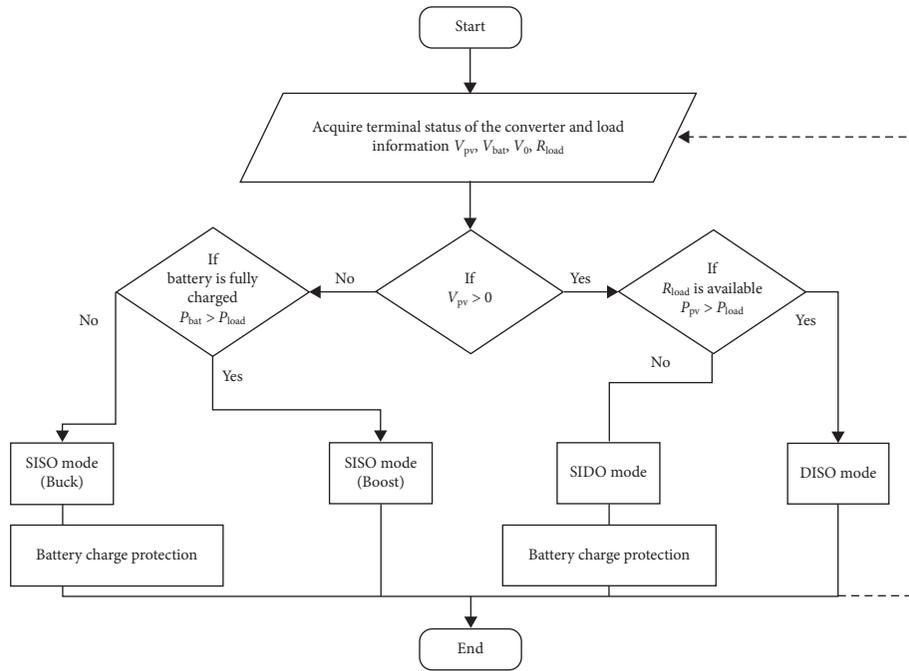
A fast recovery diode is selected for D_c , and an ultrafast recovery diode is chosen for D_{c2} , whereas the ordinary rectifier diodes with required current and voltage blocking capability are selected for D_{pv} and D_b . The ratings of components used in simulation or prototype are given in Table 1.

4. Control Scheme and Operational Mode Selection

Generally, output of the converter is regulated to satisfy the load requirement and also for the constant input to the inverter. The objective of the control scheme is to regulate the main DC link capacitor C_m voltage V_0 in SISO (boost operation) and DISO modes. In SIDO mode, the voltage V_0 over the main DC link capacitor C_m is regulated at constant value. The charging and discharging battery is also regulated in this mode. In SISO (buck operation), the objective is to direct the battery voltage V_{bat} and control the charging current i_b . The charging and discharging battery is also regulated in this mode. The mode selection and pulse width modulation (PWM) block is presented in Figure 9(a). The flow diagram explains the power flow and conditions for the transition in different modes. In this figure, V_{GS1} , V_{GS2} , V_{GS3} , and V_{GS4} are the gate driving/control signals for switches S_1 , S_2 , S_3 , and S_4 , respectively. The control signal V_{GS1} is the main control signal applied to switch S_1 in all modes. There are separate control loops for the input and output voltage ports. The comp-1 regulator keeps the PV system power at the maximum value while comp-2 regulates the output voltage at V_{ref} . The activity mode is resolved by present working conditions, for example, load power, battery condition of charge, and accessible PV power. The control algorithm which determines the opera-



(a)



(b)

FIGURE 9: (a) Control system block diagram. (b) Control flow diagram.

tional mode is presented in Figure 9(b). Initially, values of all terminal variables, i.e., V_{pv} , V_{bat} , V_0 , and R_0 , are acquired. If the battery is fully charged and PV power is not available, then the converter will operate in SISO (boost) mode. The converter

operates in SISO (buck) mode when the PV power is not available and there is light load.

If both the PV power and load are available, the converter will operate in DISO Mode. As the converter is

developed for the standalone PV system, the equation $P_{pv} + P_{bat} = P_{load}$ is always true, and hence the intermittence in PV power is always compensated by the battery system. Moreover, the converter is operated in SIDO mode; otherwise, the battery charge protection is active. The switch S_4 is used to control the battery power. The transition between modes is very smooth. For example, in SIDO mode, if $P_{pv} > P_0$ with constant load, V_{GS4} is used to control the battery power until $P_{pv} = P_0$. The converter operates in SISO mode (buck) and battery is charged from the main DC link capacitor C_m , and the control signal is V_{GS3} . This ensures smooth and soft transition between the ports.

5. Results and Discussion

In order to examine the exhibition of proposed topology and hypothetical investigation, a 100 W converter is tested in the laboratory. The proposed converter has high gain in SISO, DISO, and SIDO modes. The complete analytical and experimental results for SISO, DISO, and SIDO modes are presented. Main parts of the converter are common to all the ports. The parameters of different parts utilized in this model are given in Table 1. There are only minor changes in the values of parameters; however, shapes of the current and voltage waveforms remain the same. Design and selection of the components is performed by considering the possible maximum rating values. As the converter has only one coupled inductor, n can be expanded by keeping the duty cycle constant in order to increase the gain of the converter.

5.1. Experimental Results. A hardware prototype is developed and tested to prove the operational concepts of the proposed converter. The photographs of laboratory workstation and converter topology are presented in Figures 10(a) and 10(b), respectively. A four-layer PCB is developed by using Altium Designer, with one power plan and one segmented ground plan. In the design of PCB, the number of controlled interfaces is reduced. This reduces the common mode voltage between the interface ports so that there is less coupling from the cables into or out of the system. In order to minimize the return current path impedance, the return current path is kept closer to the signal path. "Moats" in PCB ground plan are avoided. All power and ground rails are carefully checked to ensure they do not offer common impedance routes within or outside the unit. The parameters and particulars of different segments utilized in equipment model are expressed in Table 1. For the generation of control signals, TI Launchpad-F28379D is used. The instruments used for measurements are GDS-810C, a measuring module (USM-3IV), an oscilloscope, and a multimeter.

The measured waveforms of the converter for SISO boost operating modes are presented in Figure 11. The magnetizing current i_{lm} and gate driving signal (V_{GS1}) are presented in Figure 11(a). The duty cycle d_1 for the switch S_1 is 0.6. The peak to peak voltage V_{GS1} is 12 V. The gate driving signal (V_{GS1}) vs coupled inductor leakage current i_{lk} is presented in Figure 11(b), whereas the gate driving signal

(V_{GS1}) and coupled inductor secondary current i_{LS} is presented in Figure 11(c).

Because of the leakage inductance of coupled inductor, the switch S_1 is operated under ZCS. The leakage inductance is calculated according to equation (26). The measured series resonance inductance which is combination of leakage inductance and stray inductance is 0.98 μ H. The equivalent capacitance obtained from the output capacitance of primary and synchronous switches is 100 pF. The switch S_1 is also operated under almost ZVS condition without using the external inductors and capacitors. There are some ripples in the measurement of the current due to the low sensitivity of the measuring module. The measured gate signal of switch S_1 and currents I_{Dc} are presented in Figure 11(d), whereas the V_{GS1} vs I_{Dc2} curves are plotted in Figure 11(e) which are in close similarity with the theoretical results plotted in Figure 2(a).

The gate signal of switch S_1 and corresponding drain source voltage are plotted in Figure 12. It is obvious from the results that drain source voltage of S_1 becomes zero before application of gate signal. In this case, almost ZVS is achieved by the series resonance tank L_{lk} - C_{outs1} tank circuit. The tank circuit consists of the primary side leakage inductance of the coupled inductor and the output capacitance C_{outs1} of the switch S_1 . During the off time of the signal V_{GS1} , the L_{lk} - C_{outs1} circuit resonates. As the output capacitance of the switch S_1 has been discharged by the series resonant circuit, this results in power savings and improvement in the energy efficiency of the converter.

The measured results for the SISO mode (buck operation) are presented in Figure 13. The duty cycle d_3 is equal to 0.3. The gate signal V_{GS3} and magnetizing current i_{lm} are presented in Figure 13(a). There are some ripples in the current due to the measuring setup and coupled inductor leakage inductance. The gate signal V_{GS3} of switch S_3 and corresponding drain source voltages V_{DS3} are presented in Figure 13(b). It is obvious from the figure that switch S_3 is operated under almost ZVS. In Figure 13, switching gate signal V_{GS3} and inductor's secondary current i_{LS} are presented. During the turn on of the switch S_3 , both currents i_{lm} and i_{LS} are same.

The measured results of converter in DISO mode are presented in Figure 14. The duty cycle of switch S_1 is 0.6, and the duty cycle of switch S_2 is 0.5. The gate signals V_{GS1} and V_{GS2} and the current i_b are presented in Figure 14(a). Battery supplies power to the load as long as the switch S_2 is on. As the battery voltage drops below the threshold voltage, the switch S_2 is turned off and power is supplied to the load by the source V_{pv} . Due to this, all of the results are same as those of the SISO (boost operation) mode. In Figure 14(b), the gate signals V_{GS1} and V_{GS2} and magnetizing current i_{lm} are presented. The secondary current i_{LS} and gate signals V_{GS1} and V_{GS2} are presented in Figure 14(c). It is observed that the only voltage rating and polarity of C_1 and C_2 affect the performance of the converter.

The measured results of converter in SIDO mode are plotted in Figure 15. The duty cycle of switch S_1 is 0.6, and the duty cycle of the switch S_4 is 0.68. The control signals V_{GS1} and V_{GS4} and the magnetizing current i_{lm} are presented

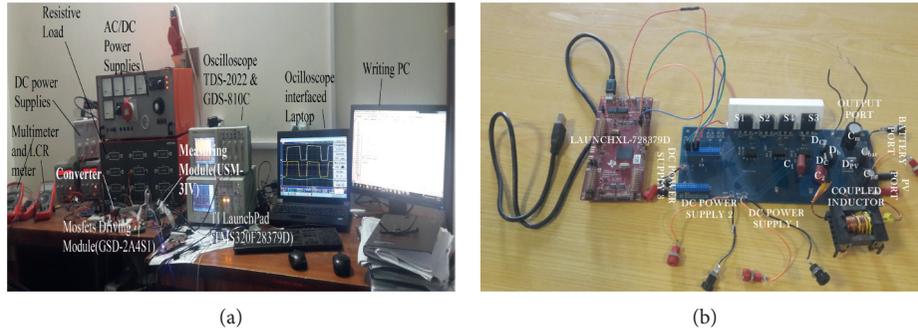


FIGURE 10: (a) Workstation photograph. (b) Hardware prototype.

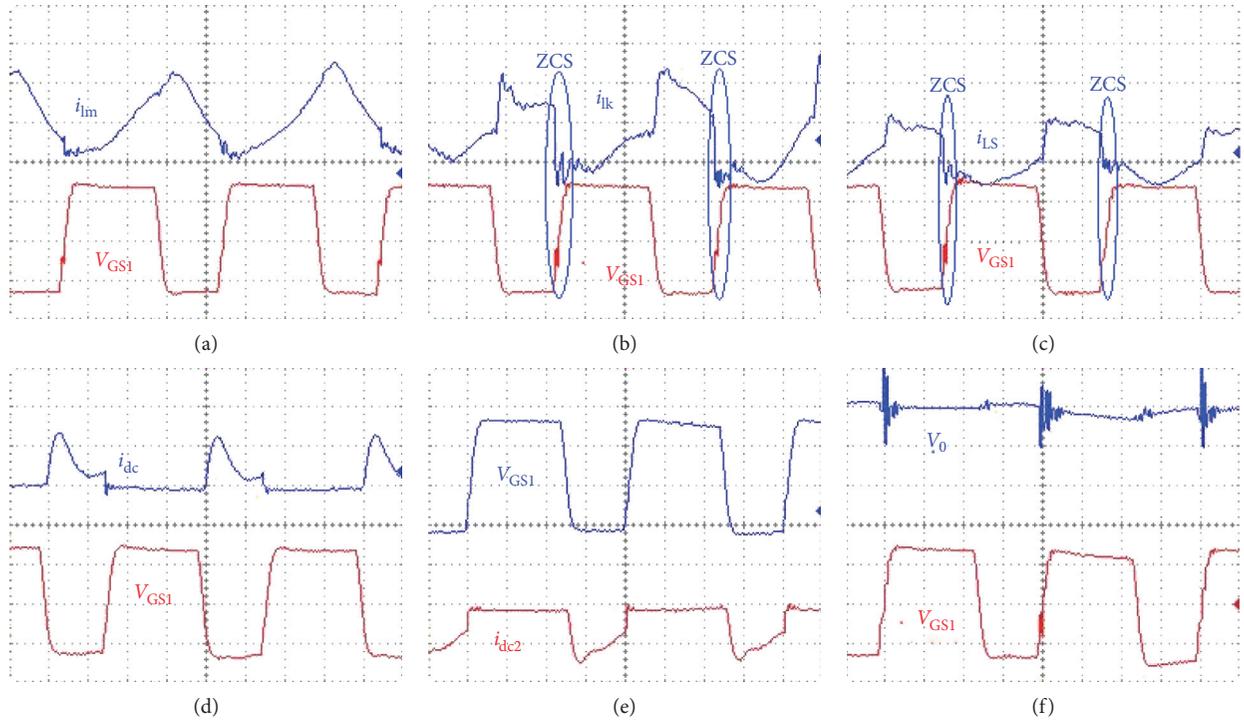


FIGURE 11: SISO (boost) mode results (scale: 5 V/DIV, 2 A/DIV, and 2.5 us/DIV). (a) Gate signal V_{GS1} and magnetizing current i_{lm} waveforms. (b) Gate signal V_{GS1} and leakage current i_{lk} waveforms. (c) Gate signal V_{GS1} and secondary current i_{LS} waveforms. (d) Gate signal V_{GS1} and diode D_c current i_{dc} waveforms. (e) Gate signal V_{GS1} and diode D_{c2} current i_{dc2} waveforms. (f) Gate signal V_{GS1} and output voltage V_0 waveforms.

in Figure 15(a). The switch S_4 is used to control the battery current i_{ch} . The excess energy generated by PV is used to charge the battery. The control signals V_{GS1} and V_{GS4} and drain source voltage V_{DS4} are presented in Figure 15(b). The gate signals V_{GS1} and V_{GS4} and secondary current i_{LS} are expressed in Figure 15(c). The diode D_c is used to transfer the voltage stress of the switch S_1 . The gate signals V_{GS4} and V_{GS1} and the current i_{dc} are presented in Figure 15(d). The current i_{ch} control signals V_{GS1} and V_{GS4} are presented in Figure 15(e). The control signals V_{GS1} and V_{GS4} and current i_{dc2} are presented in Figure 15(f)

5.2. Loss and Efficiency Analysis. The loss and efficiency of the proposed converter are analyzed in each operating mode. The SISO boost mode of operation is the main operating mode. For this mode, the efficiency of the converter as a function of output power is depicted in Figure 16(a). The converter has maximum efficiency of 96% at the power of 240 W with $V_{bat} = 96$ V in SISO mode. For input $V_{pv} = 48$ V, the converter has maximum efficiency of 95.5%. The converter efficiency is calculated by using equation (36). Table 4 shows the measured values of the input (rms) current, output current, resistive load, and efficiency values. The

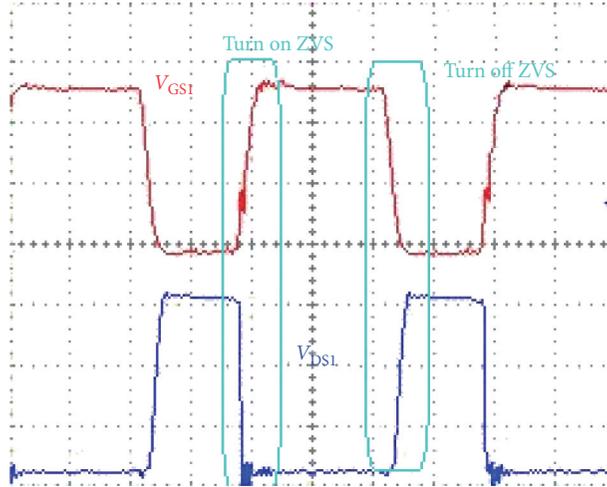


FIGURE 12: V_{DS1} and V_{GS1} during ZVS.

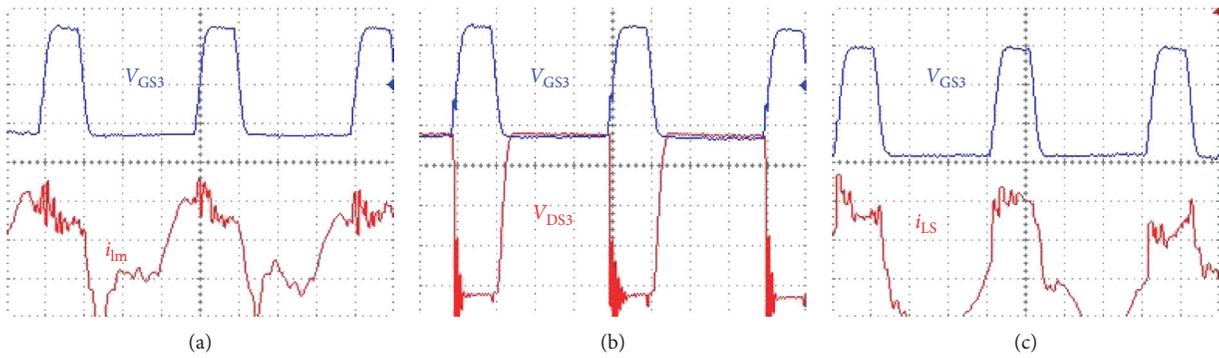


FIGURE 13: SISO mode results (buck operation) (scale: 5 V/DIV, 2 A/DIV, and 2.5 μ s/DIV). (a) Gate signals V_{GS3} and magnetizing current i_{lm} . (b) Gate signals V_{GS3} and blocking voltage V_{GS3} of switch S_3 . (c) Gate signals V_{GS3} and secondary current i_{LS} .

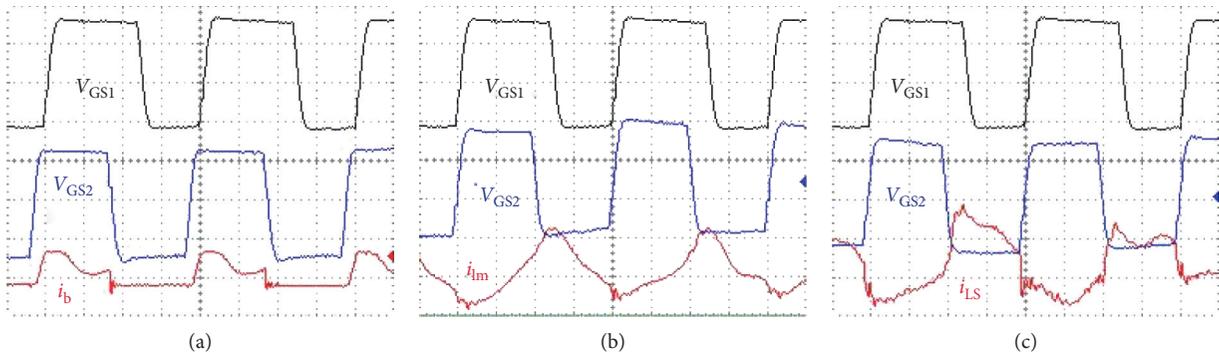


FIGURE 14: DISO mode results (scale: 5 V/DIV, 2 A/DIV, and 2.5 μ s/DIV). (a) Gate signals V_{GS1} and V_{GS2} and current i_b of switch S_2 . (b) Gate signals V_{GS1} and V_{GS2} and magnetizing current i_{lm} . (c) Gate signals V_{GS1} and V_{GS2} and secondary current i_{LS} .

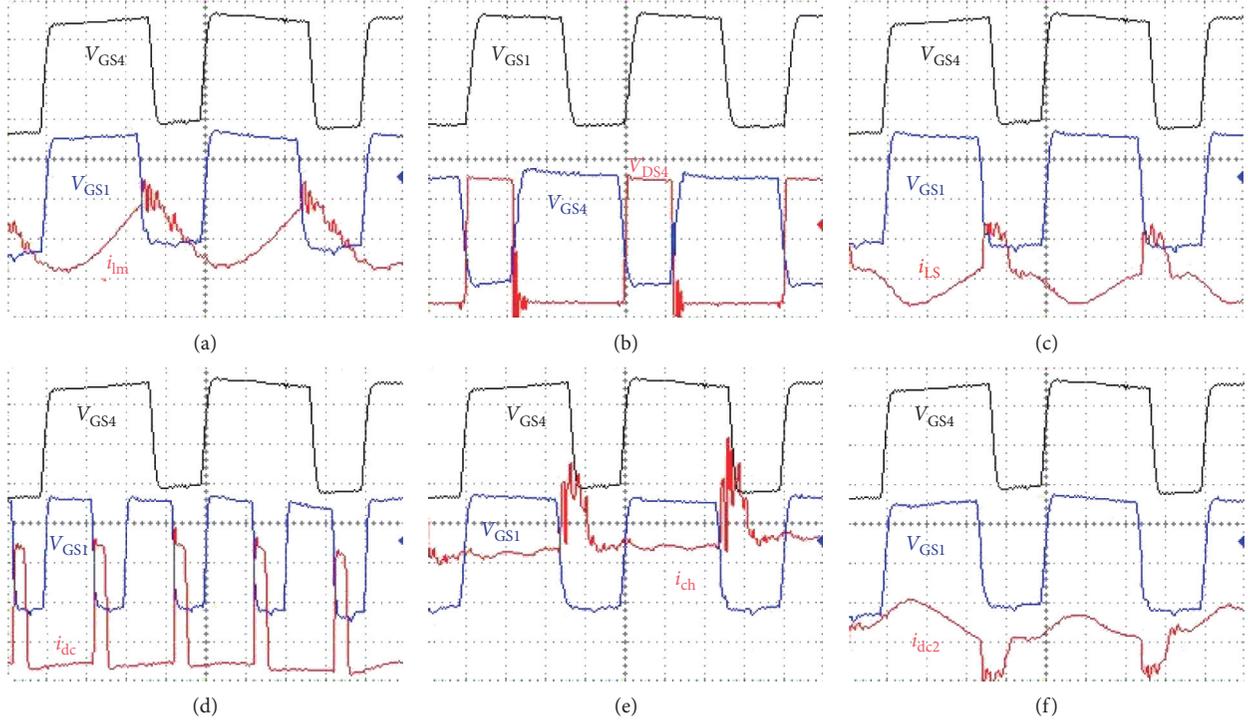


FIGURE 15: SIDO mode results (scale: 5 V/DIV, 2 A/DIV, and 2.5 us/DIV). (a) Gate signals V_{GS1} and V_{GS4} and magnetizing current i_{lm} . (b) Gate signals V_{GS1} and V_{GS2} and blocking voltage V_{DS4} of switch S_4 . (c) Gate signals V_{GS1} and V_{GS4} and secondary current i_{LS} . (d) Gate signals V_{GS1} and V_{GS4} and current i_{dc} of diode D_c . (e) Gate signals V_{GS1} and V_{GS4} and current i_{ch} of diode D_{ch} . (f) Gate signals V_{GS1} and V_{GS4} and current i_{dc2} of diode D_{c2} .

converter efficiency increases with the output power up to 240 W. Beyond this point, the energy efficiency remains constant. Under these conditions, the losses in the converter are estimated and illustrated in the pie diagram in Figure 16(b). At the output power of 100 W, the efficiency of the converter is 93% with input voltage V_{pv} and 94.5% with the input voltage V_{bat} . The maximum contribution in the loss is due to the main operating switch S_1 , i.e., FQA34N20 with $R_{DS(ON)} = 75 \text{ m}\Omega$. The switch loss can be calculated by using equation (37). The coupled inductor has the second highest losses with the exact value of 1.172 W. The series capacitor contributes about 15% and input diode has the share of 10% in the total losses. Rest of the components have relatively low loss contribution.

$$\% P_{\text{eff}} = \frac{((1+n) \times I_{\text{out}})}{(1-d_1) \times V_{\text{pv}} \times I_{\text{in}}(\text{rms})} \times 100, \quad (36)$$

$$P_{\text{loss-sw}} = R_{\text{ds}}(\text{on}) \times \frac{d_1 \times ((1+n))}{(1-d_1)}. \quad (37)$$

For the DISO mode of operation, the main power loss is the same as that of the SISO mode, but there is additional power loss due to the diode D_{pv} and the switch S_2 . The losses due to diode D_{pv} and switch S_2 are calculated by using equation (38) and equation (39), respectively.

$$P_{\text{loss-Dpv}} = V_f \times I_f * d_1, \quad (38)$$

$$P_{\text{loss-S}_2} = R_{\text{ds2}}(\text{on}) f \times I_b^2, \quad (39)$$

where I_{db}^2 is the discharging current of the battery.

The power loss in the SIDO mode is investigated by considering the loss of the diodes D_{pv} and D_b and the switch S_4 . The conduction losses for the diodes D_{pv} and D_b are computed by using equation (38) and equation (40), respectively. The switch S_4 conduction loss can be computed by using equation (41).

$$P_{\text{loss-S}_2} = V_f \times I_f, \quad (40)$$

$$P_{\text{loss-S}_2} = I_{\text{ch}}^2 \times R_{\text{ds4}}(\text{on}). \quad (41)$$

5.3. Comparison Study. The proposed converter is compared with several similar converters suitable for standalone PV system in Table 5. The comparison of proposed converter with [24, 30, 31] is performed. The proposed converter has higher switching frequency and uses less number of components to construct more useful features such as bidirectional power flow ports.

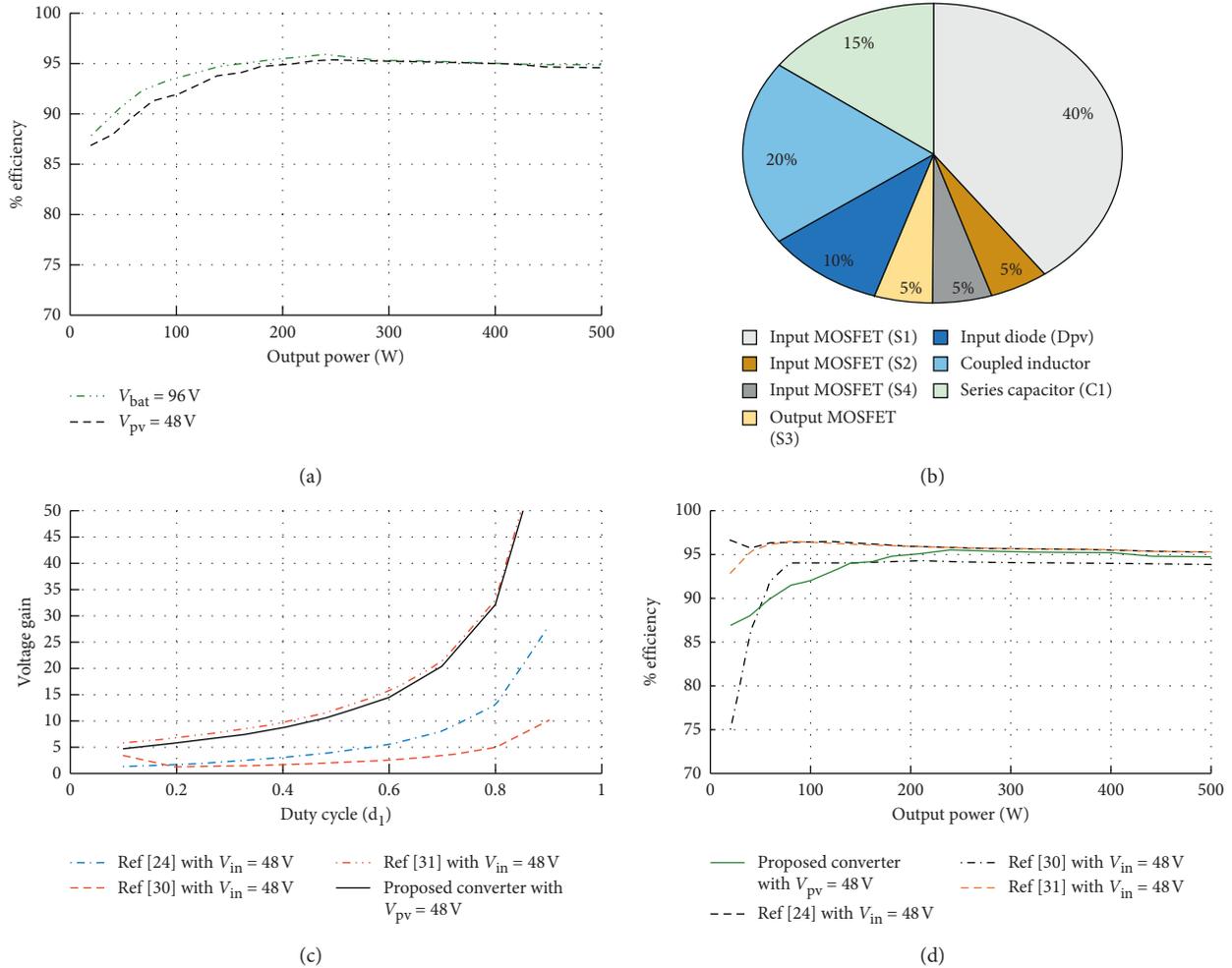


FIGURE 16: (a) Efficiency vs output power. (b) Measurement results: loss distribution on the main components of the converter at 100 W power. (c) SISO mode comparison of the proposed converter with other converters with $n = 2$. (d) Efficiency comparison of the converters.

TABLE 4: Power results in mode 1 with $V_{pv} = 48V$, $V_0 = 260V$, and $V_{bat} = 96V$.

| I_{in} (rms) (A) | I_{out} (A) | R_{load} (Ω) | % P_{eff} |
|--------------------|---------------|-------------------------|-------------|
| 11.2 | 1.314 | 288 | 93.26 |
| 9.99 | 1.2 | 300 | 95.02 |
| 8.9 | 1.06 | 340 | 94.28 |
| 7.95 | 0.95 | 400 | 94.6 |
| 7 | 0.844 | 450 | 95.5 |
| 6.13 | 0.729 | 500 | 94.14 |
| 5.2 | 0.6 | 750 | 91.34 |
| 4.98 | 0.587 | 850 | 93.31 |
| 4 | 0.469 | 950 | 92.82 |
| 3.5 | 0.4 | 1000 | 90.47 |

The proposed converter has only one conversion stage with common coupled inductor for both inputs. It has only one magnetic element, i.e., coupled inductor, four MOSFETs, two capacitors, and two diodes, whereas the converter in [24] has two coupled inductors, two inductors, and five switches. Similarly, the converter in [30] has one coupled

inductor and one inductor along with three MOSFETs, six diodes, and three capacitors. The size of the converter is relatively small. The converter proposed in [31] has one coupled inductor, three MOSFETs and capacitors each, and six diodes. The converter has no extra inductor.

The conversion gain in SISO mode is presented in Figure 16(c). The gain of the proposed converter is almost equal to the converter explained in [31], but with minimum number of device count and size. In terms of device count, operational modes, and efficiency, the proposed converter outperforms its competitors. The operational comparison of the converters in terms of the efficiency in different operating modes is presented in Figure 16(d). In comparison with other counterparts by considering the input voltage 48V, the proposed converter has the maximum efficiency of 96% which is the same as that of [24, 31], but the proposed converter is operated at 100 kHz while others are operated at 20 kHz.

A topological comparison of the proposed converter along with its other recent counterparts is presented in Table 6. The advantages and disadvantages of the various

TABLE 5: Comparative analysis of proposed converter with latest benchmarks converters.

| | [24] | [30] | [31] | Proposed converter |
|---------------------|-----------------------------------|---|-------------------------------------|--------------------------|
| Coupled inductor | 2 | 1 | 1 | 1 |
| MOSFETs | 5 | 3 | 3 | 4 |
| Inductors | 2 | 1 | 0 | 0 |
| Capacitors | 5 | 3 | 3 | 2 |
| Diodes | 5 | 6 | 6 | 2 |
| Soft switching | ZVS turn on | Almost ZCS turn on | Almost ZCS turn on | Almost ZVS turn on |
| Voltage stress | $((V_{IN} \times (n+1))/(1-d_1))$ | $((1-d_1) + d_1 \times V_{pv})/(1-d_1)$ | $((2(n+1) + n d)/(1-d))$ | $(V_{IN}/(1-d_1))$ |
| Voltage gain (SISO) | $(n \times (d+1)/(1-d))$ | $((2+n \times d)/(1-d_1))$ | $((2n+1) + (n+1) \times d/(1-d_1))$ | $((2+n+d_1(1+n))/(1-d))$ |

TABLE 6: Topological comparison of the proposed converter with other benchmarks: advantages, disadvantages, and applications.

| Converters | Topology | Advantages | Disadvantages |
|--------------------|---|---|---|
| [8] | Full bridge fully isolated | Galvanic isolation Simultaneous power management ZVS operation of the switches High gain | Large size Cost inefficient Low efficiency |
| [10] | Interleaved-boost-full-bridge | Uncoupled control ZVS and ZCS operation | Large size Less efficient |
| [12] | Flyback forward topology | High gain Galvanic isolation Multiple operating modes | Complex control Large size Less efficient |
| [13] | Full bridge partly isolated | High gain Simple structure and control Galvanic isolation | Large size Less efficient Not suitable for MPPT |
| [14] | Transformer with LCL | High gain Simultaneous power flow Good for MPPT | Less efficiency Complex control |
| [15] | Fully isolated-interleaved boost | High gain ZVS and ZCS Reduced voltage stress Smooth transition | Large size Complex control |
| [18] | Partly isolated using boost-flyback forward converter and voltage doubler | Simple structure ZCS | Low gain Not efficient Large size |
| [24] | Nonisolated coupled inductor | High gain Simple control strategy | Large size Less efficient |
| [30] | Coupled inductor | High gain Simple structure | Large size Complex control Low efficiency |
| [31] | Coupled inductor | High gain High efficiency Low voltage stress Almost ZVS operation | Complex control Limited power sharing |
| Proposed converter | Coupled inductor | High gain Reduced device count Almost ZVS and ZCS Increased efficiency | Shared control |

recent structures are given. In [8], the converter provides good galvanic isolation, ZVS operation, and high conversion gain. The converter has large size, and this makes the converter costly with lower efficiency. The converter is good

for the AC/DC integrated DC microgrid applications. In [10], the proposed converter has single conversion stage for each port which makes the control scheme simpler. It also has the ZVS and ZCS operation for all the switches.

However, the large size and low efficiency limit the converter applications. In [12], the converter has the merits of high conversion gain and flexible operation between different modes. However, the converter has large size leading to the low efficiency. Merits and demerits of some other converters [13–15, 18] are summarized in Table 6.

The coupled inductor-based topologies are discussed in [24, 30, 31]. Brief overview of these topologies is given in Table 6, whereas detailed comparative analysis is given in Table 5. These topologies are preferred for the renewable energy integration with DC microgrid.

The proposed converter has the merits of high gain, simple structure, low voltage stress on the main switches, and high efficiency. The only challenging part is the need of decoupling control as most of the components are common in the structure which can be overcome with suitable control scheme.

6. Conclusions

A three-port bidirectional power converter using a coupled inductor and a switched capacitor is proposed. Size of the converter is reduced by increasing the switching frequency. Higher voltage gain is achieved by using active clamp and switch capacitor technique. Operation of the converter is illustrated in three distinct modes, i.e., SISO, DISO, and SIDO. The converter has high gain in all operational modes. The use of the clamp circuit results in the reduction of voltage stress on the switches. All the main operating switches are operated under ZVS and ZCS. The converter efficiency is calculated and loss analysis is performed using analytic, simulated, and experimental models. The proposed converter has 96% efficiency in SISO mode. A prototype of a 100 W converter is developed by using 48 V and 96 V inputs and 380 V output voltage. The measured results of the converter are in close comparison with simulation results.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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References

- [1] REN21, “Renewables 2020: Global status report,” REN21 Secretariat, Paris, France, 2020, <http://www.ren21.net>.
- [2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, “Power electronics as efficient interface in dispersed power generation systems,” *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1184–1194, 2004.
- [3] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Family of multiport bidirectional DC-DC converters,” *IEE Proceedings - Electric Power Applications*, vol. 153, no. 3, pp. 451–458, 2006.
- [4] A. Bhattacharjee, S. M. Ieee, N. Kutkut, S. Member, and I. Batarseh, “Review of multi port converters for solar and energy storage integration,” *IEEE Trans. on Power Electronics*, vol. 8993, 2018.
- [5] N. Zhang, D. Sutanto, and K. M. Muttaqi, “A review of topologies of three-port DC-DC converters for the integration of renewable energy and energy storage system,” *Renewable and Sustainable Energy Reviews*, vol. 56, pp. 388–401, 2016.
- [6] M. Forouzes, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, “Step-Up DC-DC converters: a comprehensive review of voltage-boosting techniques, topologies, and applications,” *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, 2017.
- [7] V. N. S. R. Jakka, A. Shukla, and G. D. Demetriades, “Dual-transformer-based asymmetrical triple-port active bridge (DT-ATAB) isolated DC-DC converter,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4549–4560, 2017.
- [8] P. Wang, X. Lu, W. Wang, and D. Xu, “Hardware decoupling and autonomous control of series-resonance-based three-port converters in DC microgrids,” *IEEE Transactions on Industry Applications*, vol. 55, no. 4, pp. 3901–3914, 2019.
- [9] H. Wu, R. Chen, J. Zhang, Y. Xing, H. Hu, and H. Ge, “A family of three-port half-bridge converters for a stand-alone renewable power system,” *IEEE Transactions on Power Electronics*, vol. 26, no. 9, pp. 2697–2706, 2011.
- [10] M. C. Mira, Z. Zhang, A. Knott, and M. A. E. Andersen, “Analysis, design, modeling, and control of an interleaved-boost full-bridge three-port converter for hybrid renewable energy systems,” *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1138–1155, 2017.
- [11] S. S. Dobakhshari, S. H. Fathi, and J. Milimonfared, “A new soft-switched three-port DC/DC converter with high voltage gain and reduced number of semiconductors for hybrid energy applications,” *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3590–3600, 2020.
- [12] Y. Hu, W. Xiao, W. Cao, B. Ji, and D. J. Morrow, “Three-port DC-DC converter for stand-alone photovoltaic systems,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3068–3076, 2015.
- [13] D. Debnath and K. Chatterjee, “Two-stage solar photovoltaic-based stand-alone scheme having battery as energy storage element for rural deployment,” *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4148–4157, 2015.
- [14] J. Zeng, W. Qiao, and L. Qu, “An isolated three-port bidirectional DC-DC converter for photovoltaic systems with energy storage,” *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3493–3503, 2015.
- [15] J. Deng, H. Wang, and M. Shang, “A ZVS three-port DC/DC converter for high-voltage bus-based photovoltaic systems,” *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10688–10699, 2019.

- [16] X. Sun, Y. Shen, and W. Li, "A novel LLC integrated three-port DC-DC converter for stand-alone PV/battery system," in *Proceedings of ITEC Asia-Pacific*, pp. 1–6, Beijing, China, August-September 2014.
- [17] Y.-E. Wu and K.-C. Hsu, "Novel three-port bidirectional DC/DC converter with three-winding coupled inductor for photovoltaic system," *Energies*, vol. 13, no. 5, p. 1132, 2020.
- [18] Y.-E. Wu and I.-C. Chen, "Novel integrated three-port bidirectional DC/DC converter for energy storage system," *IEEE Access*, vol. 7, pp. 104601–104612, 2019.
- [19] L. Li, Y. Li, G. Wu, and X. Hu, "Input-parallel output-series DC-DC converter for non-isolated high step-up applications," *Electronics Letters*, vol. 52, no. 20, pp. 1715–1717, 2016.
- [20] J. Garcia, R. Georgious, P. Garcia, and A. Navarro-Rodriguez, "Non-isolated high-gain three-port converter for hybrid storage systems," in *Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1–8, Milwaukee, WI, USA, September 2016.
- [21] B. Zhang, P. Wang, T. Bei, X. Li, Y. Che, and G. Wang, "Novel topology and control of a non-isolated three port DC-DC converter for PV-battery power system," in *Proceedings of the 20th International Conference on Electrical Machines and Systems (ICEMS)*, pp. 1–6, Sydney, NSW, Australia, August 2017.
- [22] C. M. Lai and M. J. Yang, "A high-gain three-port power converter with fuel cell, battery sources and stacked output for hybrid electric vehicles and DC-microgrids," *Energies*, vol. 9, no. 3, pp. 6–9, 2016.
- [23] L. Muller and J. W. Kimball, "High gain DC-DC converter based on the cockcroft-walton multiplier," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6405–6415, 2016.
- [24] Y.-M. Chen, A. Q. Huang, X. Yu, X. Yu, and S. Student Member, "A high step-up three-port DC-DC converter for stand-alone PV/battery power systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5049–5062, 2013.
- [25] R. Faraji and H. Farzanehfard, "Soft-switched nonisolated high step-up three-port DC-DC converter for hybrid energy systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10101–10111, 2018.
- [26] V. R. Teja, S. Srinivas, and M. K. Mishra, "A three port high gain non-isolated DC-DC converter for photovoltaic applications," in *Proceedings of the 2016 IEEE International Conference on Industrial Technology (ICIT)*, pp. 251–256, Taipei, Taiwan, March 2016.
- [27] F. Nejabatkhah, S. Danyali, S. H. Hosseini, M. Sabahi, and S. M. Niapour, "Modeling and control of a new three-input DC-DC boost converter for hybrid PV/FC/battery power system," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2309–2324, 2012.
- [28] L.-Y. Chang, J.-H. Chang, K.-H. Chao, and Y.-N. Chung, "A low-cost high-performance interleaved inductor-coupled boost converter for fuel cells," *Energies*, vol. 9, no. 10, p. 792, 2016.
- [29] M. Das, S. Member, and V. Agarwal, "Generalized small signal modeling of coupled inductor based high gain, high efficiency DC-DC converters," in *Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 2691–2695, Charlotte, NC, USA, 2015.
- [30] L.-J. Chien, C.-C. Chen, J.-F. Chen, Y.-P. Hsieh, and Y. Hsieh, "Novel three-port converter with high-voltage gain," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4693–4703, 2014.
- [31] B. Honarjoo, S. M. Madani, M. Niroomand, and E. Adib, "Non-isolated high step-up three-port converter with single magnetic element for photovoltaic systems," *IET Power Electronics*, vol. 11, no. 13, pp. 2151–2160, 2018.
- [32] M. Arif, "A novel high gain bidirectional multiport DC-DC converter to interface PV, battery, and ultracapacitor with microgrid system," in *Proceedings of the 2017 International Conference on Frontiers of Information Technology (FIT)*, pp. 121–126, Islamabad, Pakistan, December 2017.
- [33] M. Arif, J. Saleem, Q. Abbas, I. Todorovic, and A. Majid, "High gain bidirectional multiport DC to DC converter for DC microgrid," in *Proceedings of the 2017 International Symposium on Power Electronics (Ee)*, pp. 1–6, Novi Sad, Serbia, October 2017.