Hindawi Publishing Corporation
International Journal of Aerospace Engineering
Volume 2014, Article ID 808374, 13 pages
http://dx.doi.org/10.1155/2014/808374

Research Article

Boost Full Bridge Bidirectional DC/DC Converter for Supervised Aeronautical Applications

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Received 18 August 2013; Revised 11 November 2013; Accepted 12 November 2013; Published 22 January 2014

Academic Editor: Nicolas Avdelidis

The More Electrical Aircraft concept requires electronic devices able to efficiently and safely convert electrical power between different voltage levels. The entire realization of a bidirectional DC/DC converter, from design to validation phase, is here discussed in detail. First, a boost full bridge electrical structure is selected, adopting a Parallel Input Parallel Output (PIPO) interleaving technique and an optimal turns ratio selection for the transformers in order to reduce both weight and size of the equipment. Next, modulation schemes in both step-down and step-up modes are discussed. Successively ad hoc PI regulators for both operative modes are presented. A key idea of the paper is that the converter behavior must be related not only to the control strategy but also to a global supervision logic able to safely conduct the converter operations and to react from external stimuli. Thus, a finite state machine (FSM) approach is employed. An innovative strategy called buffer mode is presented, defined as an intelligent combination of buck and boost modes. Extensive simulations and experimental results are shown, in order to confirm the effectiveness of the proposed approach.

1. Introduction

Classical onboard aircraft systems use different power sources: mechanical, electrical, hydraulic, and pneumatic. To overcome the classical drawbacks of nonelectrical or only partially electrical equipment, the More Electrical Aircraft (MEA) concept has been introduced, having as target the use of electrical power sources only. This strategy has some advantages as follows:

(i) higher reliability;

(ii) ease of maintenance;

(iii) lower consumption of fuel;

(iv) lower production costs and maintenance.

An immediate consequence of this new approach is the necessity of electrical power sources, distribution, and sharing of the power redesign phase, in order to accommodate for new technologies insertion inside classical aircraft systems. To limit the section area of the electrical power conductor and to simplify the dynamical connection/disconnection of one or more power generators (without necessity of synchronization as for AC sources), the MEA's study [1] suggests to use as main bus a high-voltage DC bus. The new standards assume ±270 VDC or +270 VDC for the main bus and 28 VDC, 115 VAC@400 Hz, and 230 VAC@400 Hz for secondary bus. As a result, in modern aircraft different kinds of power electronic converters, such as AC/DC rectifiers, DC/AC inverters, and DC/DC choppers, are required. In particular, bidirectional DC/DC converters are used in battery charge/discharge units and in very critical situations where the aircraft auxiliary power source represented by a battery can be assumed as the final source of backup power. Therefore, to manage correctly the different voltage levels, the future aircraft electrical power systems will employ multiconverter power electronic systems [2].

In this paper the entire process of design, realization and testing of a bidirectional DC/DC converter (assuming 28 V and 270 V as low-voltage and high-voltage side reference values, resp.) will be investigated, providing a set of guidelines for a correct development of an electronic device that must fulfill different requirements. The current paper mainly refers

to [3, 4] contributions of the same authors, but here providing a more comprehensive view of the overall implementation process, specifically focusing on the buffer mode implementation, main innovation in the field of DC/DC converter control.

Focusing on the converter design phase, it must be accomplished keeping in mind the following general key points:

(i) bidirectionality;

(ii) high efficiency for the whole power conversion process;

(iii) wide variations of input voltage versus fixed output voltage;

(iv) necessity of low dimensions and weight for better system integration and cost reduction;

(v) very high reliability during emergency operations.

Furthermore, the operative context of the DC/DC converter must be investigated in order to derive additional requirements that will steer the project phase. The present paper deals with a converter able to deliver 6 kW at 28 V side in step-down (or buck) mode and 12 kW at 270 V side in step-up (or boost) mode. A battery will be directly connected to the 28 V side, while the energy for recharging operations flows from a 270 V bus, fed by a primary electrical source.

DC/DC converters are usually required in many industrial applications where energy conversion is essential for a variety of purposes.

Selection of the best converters topology is usually very complex for different reasons.

The main point is the impossibility to realize a comparative study between different converters adopting the same technology, size, and operative conditions, starting from experimental results. In fact, nontheoretical factors like quality of the electrical constitutive elements, aging, and skills of operators involved in hardware construction will heavily affect the global realization of the converter and could suggest a nonoptimal choice, preferring an easier and more efficient technological realization rather than a more sophisticated solution [5].

Focusing firstly on DC/DC converter design phase in boost mode, consider that high-voltage ratio between input/output voltages cannot permit the use of boost topology because maximum value of duty cycle is limited due to the nonideality of power components [6, 7]. To achieve a high step-up voltage ratio, transformer or coupled-inductor or also transformerless based converters are usually the right choices [6, 8–10]. Paralleling of converter power stages is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size of power transformers and inductors [9–13]. The reference PIPO configuration for our purposes is reported in Figure 1, referring to a DC/DC converter based on a 4-modules structure. Focusing the attention on isolated topology, various isolated hard switching power converters can be studied, further reducing them to boost or buck derived topology.

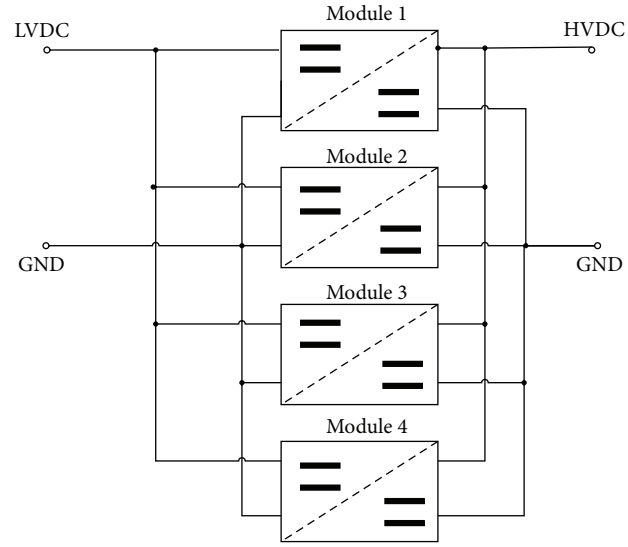

Figure 1: PIPO connection scheme.

It can be proved [5] that boost-derived converters are more efficient than buck-derived in almost all operative conditions. For high-power applications, boost full bridge converter is a good choice which reduces voltage stress of switches, removes the necessity of reset circuits for the transformer, and, finally, is bidirectional [14].

One approach to realizing a large power converter system is the use of a "cellular" architecture in which many quasi-autonomous converters, called cells, are paralleled to create a single large converter system [15].

Cells share the same input and output busses, but each one requires only to process a fraction of the total system power, thus obtaining the known benefits in adopting cellular DC/DC converters [16, 17].

2. Electrical Structure

2.1. Converter Topology. Subject of this paper is a cellular converter, where all the cells are connected to each other in PIPO mode (Parallel Input Parallel Output).

The interleaving technique is used to reduce components size (in particular the size of the inductor) [18], current ripple, and EMI [19] and to improve the reliability [20, 21], as previously discussed. Each cell is a boost full bridge converter, rated at 3 kW as reported in Figure 2.

An active clamp [22] was inserted to permit the converter to work in different operative modes: buck and boost without external circuit for start-up and furthermore to allow overvoltage clamping across the switch. In buck mode, the active clamp can be excluded to permit the LC filter ($L1, C2$) to work correctly. In boost mode, when duty cycle $\delta < 0.5$ switches *ACABIL* and *ACASW* are closed, to configure $C2$, $L1$, and $C3$ as a π input LCL filter and to avoid overvoltage due to the nonzero current in the $L1$ inductor, occurring when all the low-side switches are open.

The control strategies of the active clamp will be discussed in detail in Section 2.3.

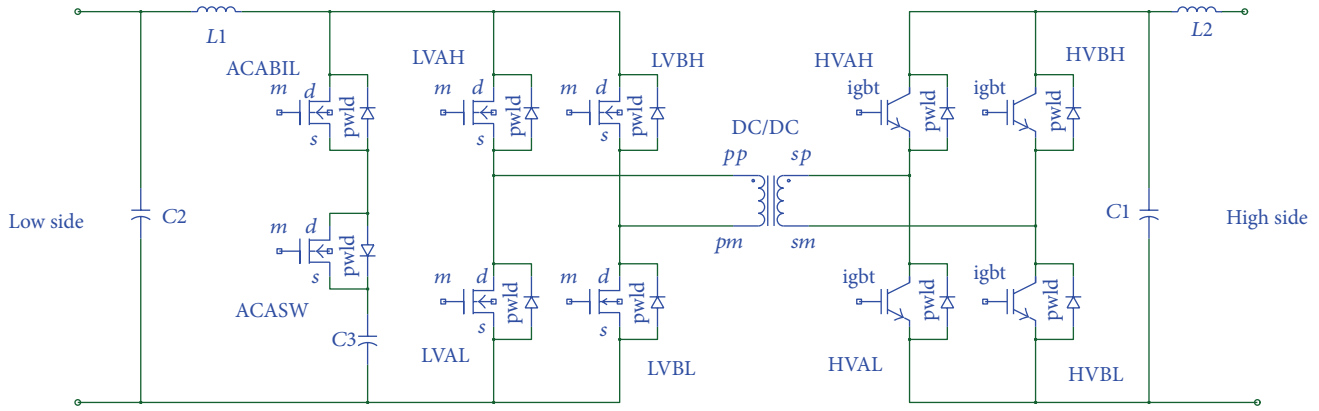

Figure 2: Boost full bridge with active clamp scheme.

To limit inrush currents on the connection of the converter to the power bus, high/low side $C1$ and $C2$ capacitors are connected in series to precharge resistors, not reported in Figure 2, that can be excluded at the end of the start-up phase. This solution, in combination with the usage of paralleled switches for the proposed topology, particularly for steady state operations, is used to reduce the current flowing at the current-fed side in both buck and boost modes. Another key aspect of the interconnection of the converter to the power bus is the capability of the converter to connect/disconnect itself automatically to avoid damage of hardware. Protection logic is discussed in detail in Section 4.1.

2.2. Optimal Transformer Turns Ratio Selection. The sizing of the transformer is a critical point for the converter design process. In fact, an erroneous transformer sizing process leads to incorrect choices of the power electronic components, resulting in the unfulfillment of the required specifications.

To illustrate the turns ratio selection process, first consider the boost or step-up mode. Starting from the steady state equation of the converter in boost mode:

$$\frac{V_o}{V_i} = \frac{k}{2\,(1-\delta)}, \tag{1}$$

where V_o is the output bus voltage, V_i the input battery voltage, and k the transformer turns ratio, we can write a relationship between the duty cycle and the voltage ratio, considering the turns ratio a parameter to be optimally selected. The constraints to be considered are the input/output voltage and the admittable duty cycle that have to be confined in a narrow range to avoid undesirable effects such as overcurrents, overvoltages, and overtemperatures, further satisfying the global requirements [6]. For our application, we consider $V_i = [23, 30]$ V, $V_o = [260, 280]$ V, and $\delta \in [0.5, 0.8]$. Adding a term $\varphi = 0.9$ to take into account nonideal elements effects, it can be proved [23] that turns ratio must satisfy the following inequalities:

$$\begin{aligned} k &\geq 2\Gamma_{\min}\left(1-\delta_{\max}\right)\frac{1}{\varphi}, \\ k &\leq 2\Gamma_{\max}\left(1-\delta_{\min}\right)\frac{1}{\varphi}, \end{aligned} \tag{2}$$

where $\delta_{\min}$ and $\delta_{\max}$ are the minimum and maximum admittable duty cycle values, respectively, and $\Gamma_{\min}$ and $\Gamma_{\max}$ are minimum and maximum $V_{\text{out}}/V_{\text{in}}$ ratios, respectively. For a correct selection, we must define a desirable value of the duty cycle δ in the nominal point of work. Different factors can be considered to support the above choice, for example, maximization of the utilization factor or minimization of the switch stress. Solving (2) we obtain $\delta_{\min_{\text{opt}}} = 0.6$ and $\delta_{\max_{\text{opt}}} = 0.77$ as converter duty cycle optimal value thresholds; therefore solution must lie inside the highlighted blue area of Figure 3.

As a first partial result, we obtain that $k \in [7.14\text{–}7.63]$. The converter bidirectionality requires to ensure that the k value choice is correct in both cases. Therefore, it is necessary to repeat all the calculation already performed for step-up mode, starting from the steady state relationship of the converter in buck mode:

$$\frac{V_o}{V_i} = \frac{2\delta}{k}. \tag{3}$$

As for boost mode, we have a linear relationship between duty cycle value and turns ratio parameter. The duty cycle is limited to 0.5 as maximum value. Besides, it is possible to define the Γ parameter range taking into account the allowed input and output voltage values. Following the same approach as in boost, thus defining the input and output voltage ranges $V_o = [27, 30]$ V and $V_i = [260, 280]$ V, and also $\delta_{\text{opt}} \in [0.35, 0.48]$, two inequalities can be derived:

$$\begin{aligned} k &\geq 2\Gamma_{\min}\delta_{\min}\varphi, \\ k &\leq 2\Gamma_{\max}\delta_{\max}\varphi. \end{aligned} \tag{4}$$

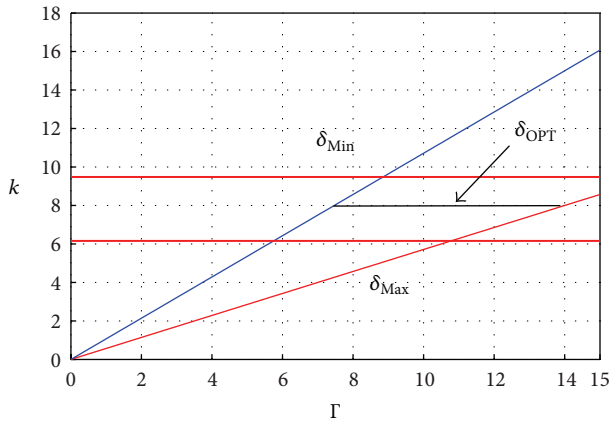

Figure 3: Range of the solutions in boost mode.

For buck mode we obtain that $k \in [6.68 - 11.08]$. Merging the solutions obtained for both buck and boost mode selection process, the unique turns ratio must lie in the intersection of two calculated ranges. The value 7.5 has been chosen as final turns ratio for the DC/DC converter transformers.

2.3. Modulation Strategies. The control strategy of the converter must guarantee bidirectional functionalities and regulation of the output voltage, acting on both duty cycle and modulations. No additional hardware is required for bidirectionality. To avoid transformer magnetic core saturation, bidirectional magnetization is used adopting "voltage cancellation" technique [24] and the low-voltage full bridge is driven as a synchronous rectifier to improve efficiency of the converter. Active clamp circuit is disabled to permit the correct functionality of the LC filter ($L1$, $C2$).

The basic idea is to alternate the DC bus voltage on the HV side, in order to let the transformer reduce its average value and provide a rectification stage using the full bridge on the LV side, as reported in Figure 4. The turn on/off sequence of the different switches in buck mode is reported in Figure 5, focusing on a single period T. Details about the different configurations and electrical variable evolutions in each different switches configuration are not reported here, as well as for boost mode.

This global behavior is obtained also in boost mode, clearly reversing the electrical flows. In boost mode, modulation strategies change depending on the duty cycle value, as reported in Figure 6, and high-voltage full bridge works as a rectifier.

When $\delta \geq 0.5$ we can observe two main phases [14], that is, the boost inductor charging followed by the energy transfer through the transformer, as reported in Figure 6. The active clamp is used to limit extra voltages across power switch due to the transformer leakage inductance. Another key point is the necessity to have a zero state for the converter (i.e., $V_o = 0$ with $V_i \neq 0$) to permit the startup without precharge of the high voltage capacitor ($C1$) and also the shutdown. We can observe that the modulation of Figure 6 with $\delta < 0.5$ cannot be used, due to possible damage of the converter when the inductor has a nonzero current value.

3. Control Stage

The main objective of the control section is the regulation of the output voltage V_{out} at a reference level V_{ref}, depending on the selected mode (i.e., 28 V for step-down mode and 270 V for step-up mode), while fulfilling standard power quality requirements (e.g., defined by MIL-STD-704F for aeronautical equipment). The standard approach involves the classic PWM modulation in order to convert the duty cycle $\delta \in [0, 1]$ into on/off signals for the full bridges switches. The duty cycle value must be regulated by using a feedback control strategy in order to guarantee robustness to disturbances effects and to voltage level variations on both sides, typically due to charging/discharging of the battery and undervoltages/overvoltages on the high-voltage bus.

Different PI controllers have to be tuned in order to switch among them, depending on the converter state [25]. Specifically, in boost mode an inner control loop is required to achieve a faster response when a power demand is issued by an upper level command [26]. Further, smooth duty cycle variations between two successive control cycles and soft startup/shutdown must be guaranteed on the controlled variables.

The control scheme adopted for buck and boost modes, respectively, reported in Figures 7 and 8.

In buck mode, initially an open-loop control is used by increasing linearly the duty cycle, whose slope is determined by acting on K_r gain, until $V_{out} > V_{ref}$. Then, until buck mode is active, a PI strategy is adopted, with control gains tuned by using standard self-tuning procedures. The obtained gains are $K_p = 0.0001$ and $K_i = 0.001$.

Also, in boost mode, an open loop linearly increasing duty cycle is initially used, choosing an appropriate K_r gain. Then, when $V_{out} > V_{ref}$, a feedback PI controller is designed, with control gains again tuned in MATLAB. Moreover, for each module an inner control loop implemented via PI controller is used. The gains $K_p = 0.0001$ and $K_i = 0.001$ have been selected, again using standard tuning techniques.

Note that, due to the linearity of (3), a PI controller is sufficient to guarantee the regulation of the imposed voltage at a fixed level (28 V in buck mode or 270 V in boost mode) by acting directly on duty cycle. Therefore these ad hoc regulators, basically modified PI controllers, have been preferred to more complicated, optimal controllers.

4. Converter Supervision

4.1. Finite State Machines Approach. The DC/DC converter is a complex electrical system; therefore clearly the necessity of a supervision strategy arises, in order to define the converter behavior through a predefined sequence of paths. The outlined finite state machine approach is closely linked to the hybrid systems supervisory control [27], just differing for a minor mathematical formalism and a more intuitive framework. A simple partition of the converter state-space

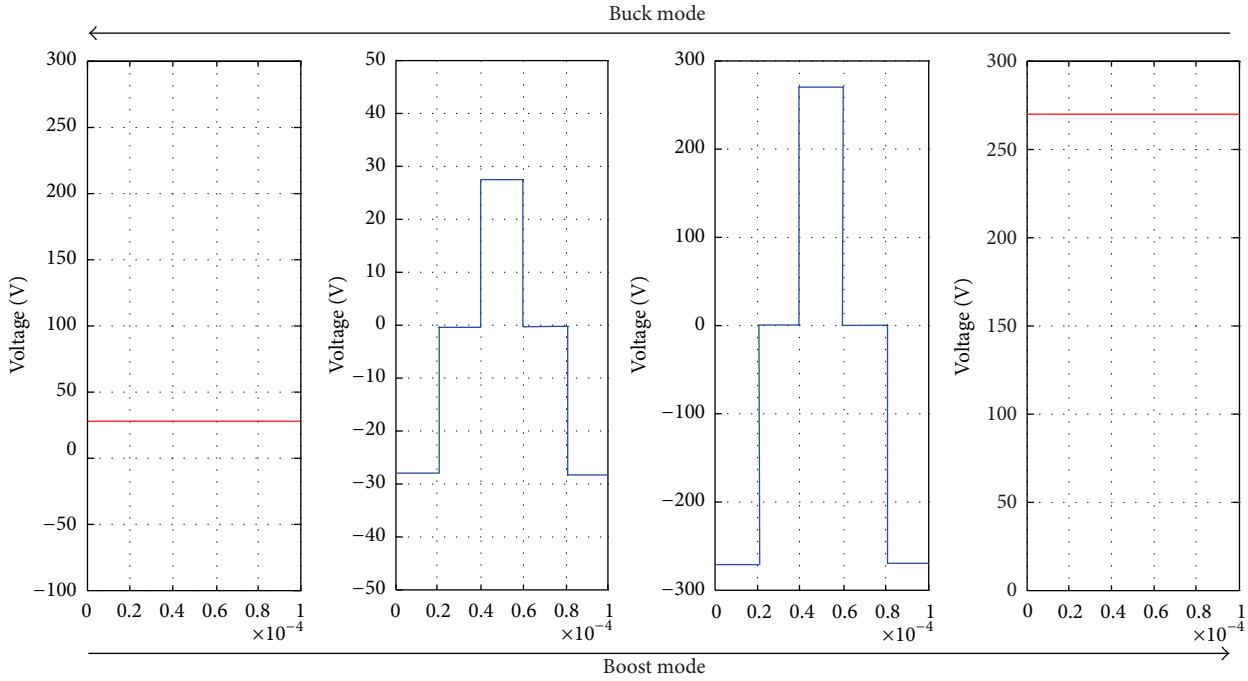

Figure 4: Voltage transformations in buck and boost mode.

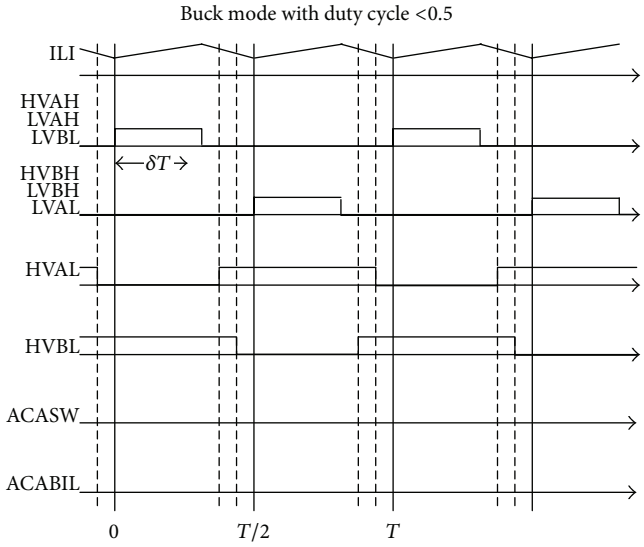

Figure 5: Buck mode modulation.

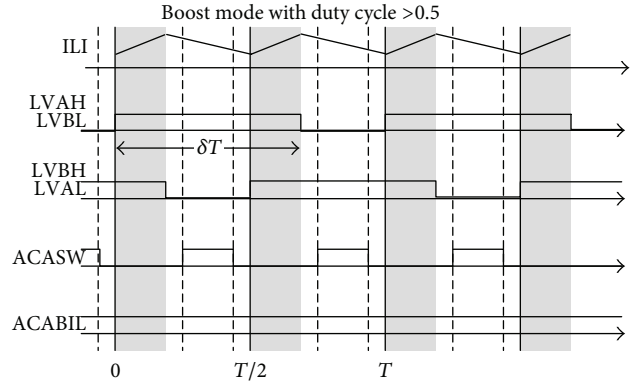

Figure 6: Boost mode modulation, $\delta \geq 0.5$.

has been selected, based on time events (i.e., transient, steady state) and simplifying the task of finding all the successor states, considering only a logical succession of converter well-known configurations.

4.1.1. Buck and Boost Mode Supervision. The buck mode state machine for supervision is reported in Figure 9, where "time" is the measured time since the electrical power-on of the converter, V_{lv} is the output voltage, "fault" is a converter failure event, and "start" is the power-on signal.

Every state is associated with a converter specific condition as follows:

(i) *S0*: initialization of the electrical components and of the communication protocol with FPGA;

(ii) *S1*: deactivation of precharge resistor;

(iii) *S2*: enabling of protections; output voltage is at steady state.

A state transition can be determined by a time value (e.g., from *S0* to *S1*), a voltage value (e.g., from *S1* to *S2*), or an external signal (e.g. a "start" signal to *OFF* as in transition from *S2* to *S0*). The upper and lower bounds for low-voltage side are 32 V and 24 V and for high-voltage 290 V and 250 V, respectively (for both sides, at steady state). If any of these bounds is overcome and the converter is in the appropriate

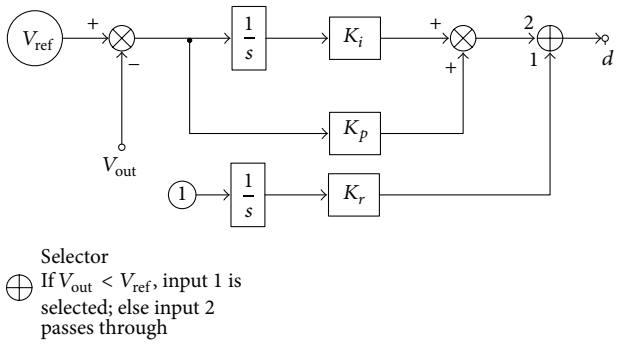

Figure 7: Buck mode controller.

state, it is quickly turned off by decreasing the duty cycle value to zero. Using a variable (i.e., *BuckStatus*, initialized to 0 and different for each state) the FSM can be easily translated into a microprocessor firmware.

The boost mode state machine is reported in Figure 10. The associated FSM is straightforward and considers also the possibility of an already active high-voltage network, inserting a secondary loop where a safety procedure is executed before its connection to the PEPDC (Primary Electrical Power Distribution Center).

4.1.2. Buffer Mode Concept and Supervision. DC/DC converters in aeronautical electrical systems are used to connect networks at different voltage levels (i.e., 270 V and 28 V). In emergency conditions, energy can be recovered from the low-voltage network, usually a battery pack recharged during normal operations, and transferred to the high-voltage network thanks to the conversion operation performed by the converter, until it is necessary. Switching from buck to boost mode, and vice versa, should be a automatic process, completely transparent to an human operator. A challenging problem is the definition of a suitable logic devoted to confer autonomy to the converter, able to sense the boundary conditions and decide between step-up and step-down modes.

The power quality impairment event can be easily defined as in MIL-STD-704F, where only the lower boundary is considered and the transient starts if a voltage lower than 260 V on high-voltage side is detected. The decision about the boost-to-buck transition is difficult, since the converter regulates the voltage to 260 V; hence sensing the high-side voltage is useless. Some information on the overload status could be derived from the high-voltage side generator current measurement, but an external variable from an additional current sensor should be considered. The buffer mode key idea, instead, is a smart combination of buck and boost modes considering only internal measurements. Besides, in dedicated boost mode, due to the impossibility of sustaining two voltage sources in a parallel configuration onto an electrical network, the converter regulates its output current (not the voltage) with a hysteresis control and supports the PEPDC until its contribution is no longer necessary (i.e. the duty cycle is regulated to zero value, as a natural consequence of the control strategy). When this event occurs, the converter automatically commutates again from boost to buck mode, returning to the initial state. In Figure 11 the state machine for buffer mode implementation is reported.

As for boost FSM, two loops are present because in buck mode also the converter is a power load for the electrical network and could be itself the cause for the power quality impairment. The variables "Timer," "Duty," and V_{hv} have been already defined. V_{inf} is the lower threshold to be respected. It is necessary to describe each state for a better comprehension of buffer mode as follows:

(i) *S*0: initialization of the electrical components and of the communication protocol with FPGA;

(ii) *S*1: buck logic FSM; the converter works in buck mode; transition for *S*2 is active at buck steady state;

(iii) *S*2: high-side voltage is less than 260 V; begin comparison with lower bound of Figure 16 in MIL-STD-704F;

(iv) *S*3: voltage loss is critical for PEPDC; decrease duty cycle in buck and prepare to start boost control;

(v) *S*4: PEPDC is overloaded but operative, wait for end of voltage transient or switch to boost-buffer mode;

(vi) *S*5: converter is not charging battery; verify if the power saved is sufficient to restore power quality on PEPDC;

(vii) *S*6: activation of boost-buffer mode; converter hysteresis current control is started;

(viii) *S*7: activation of buck-buffer mode; the duty cycle is regulated with a double hysteresis control.

If the converter operates in *S*6 or *S*7 state, the usual PI control is neglected and replaced by two different hysteresis controllers.

The single hysteretic controller generates an increasing duty, supplying the load on low-side voltage for regulation in a narrow band (i.e., between 28 V and 29 V). In this case, the duty is decreased until the upper hysteresis limit is reached, where again the duty is decreased, and so on. The integral action is saturated at a duty cycle d_{max} and cannot be lower than zero. The described logic permits an autoregulation of the duty cycle value, depending on the electrical network characteristics. The hysteretic controller implemented for boost-buffer mode works as follows. If high-side current does not exceed a given threshold, here chosen as $I_{max} = 40$ A, V_{hv} is regulated to the average value $(V_{HTH} + V_{LTH})/2$, where V_{HTH} and V_{LTH} are the higher and lower hysteresis thresholds, respectively. Otherwise, the duty cycle is driven to zero, in order to switch off the converter. The autoregulation of the duty depends on the output voltage, that increases as the PEPDC fault condition terminates, and on the current sensed at the high-voltage side. The hysteresis threshold have been chosen as $V_{LTH} = 260$ V and $V_{HTH} = 264$ V. As evident, the converter controller active in this buffer state does not permit the overcoming of the bus voltage, and consequently the converter behaves like a current source, providing the overload current in order to restore (if possible) the nominal conditions.

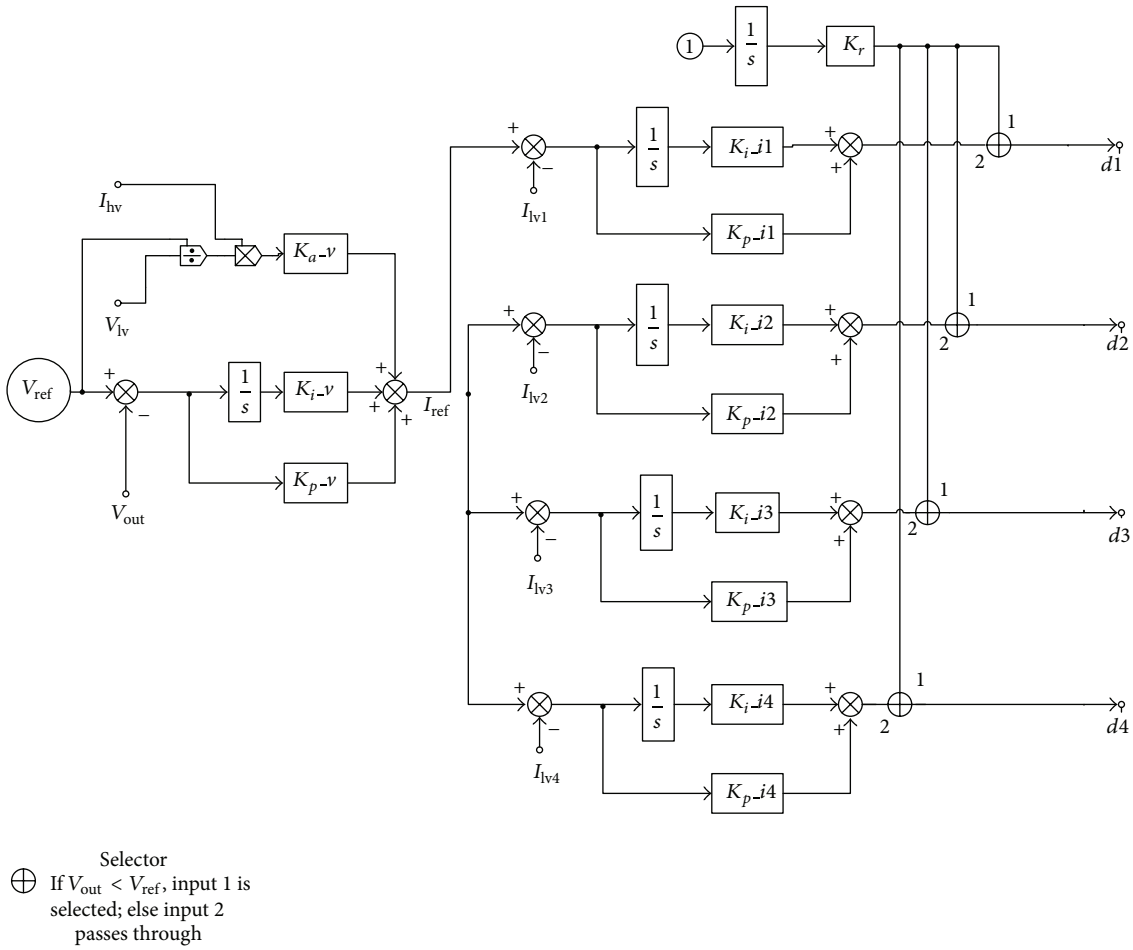

Figure 8: Boost mode controller.

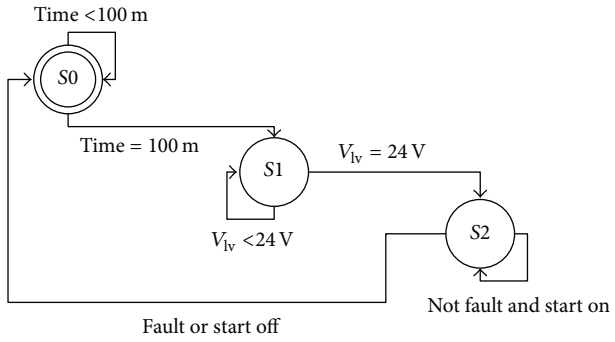

Figure 9: Buck mode state machine.

5. Simulation and Experimental Results

5.1. Behavioral and Functional Schemes in SABER Environment. Two different simulation levels have been considered at this stage, both in SABER environment. A "behavioral" scheme has been realized for taking into account all electrical details, in particular switching effects. On the other hand, a "functional" scheme has been implemented to investigate only "average" effects, removing the switches and adopting a transfer function strongly based modeling. While electrical structure has been already discussed and shown in Figure 2, functional scheme key idea is the replacement of a switching element with a voltage controlled generator. A detailed description of functional modeling for a DC/DC converter is discussed in [28].

5.2. Buck and Boost Mode Results. To validate the converter SABER schemes, different tests have been performed, stressing the equipment also in critical conditions (i.e., short circuits, overloads, and load disconnection). For buck mode, due to space limitations, only a typical test bench is reported in this paper, where an ideal source at 270 V nominal voltage is connected at the input side, and a resistive load is present at output side. A similar test configuration is arranged for boost mode, where the ideal source at input side is at 28 V level and an ad hoc resistor is connected to high-voltage side. A control robustness test has been performed for both step-up and step-down modes. In particular, starting for both buck and boost mode from a steady-state condition for a resistive load at half nominal power, an additional load is connected at the output side in order to obtain full power. As shown in Figures 12 and 13, the buck controller is able to react to the sudden load variation at $t = 850$ ms and regulate 28 V

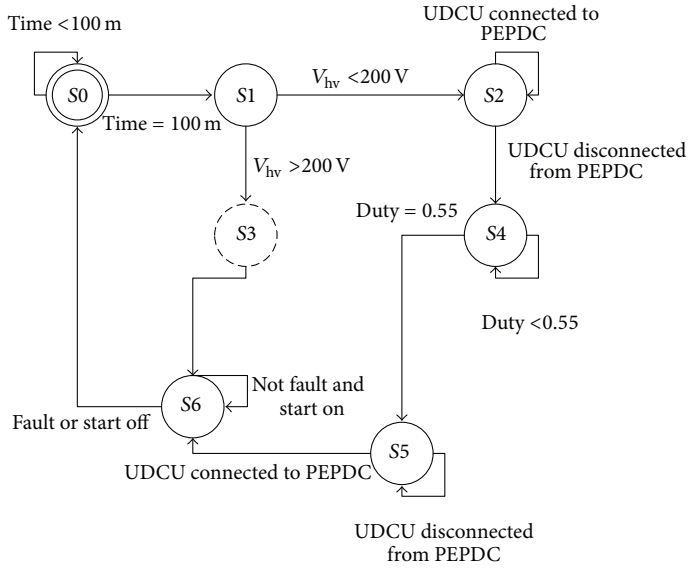

Figure 10: Boost mode state machine.

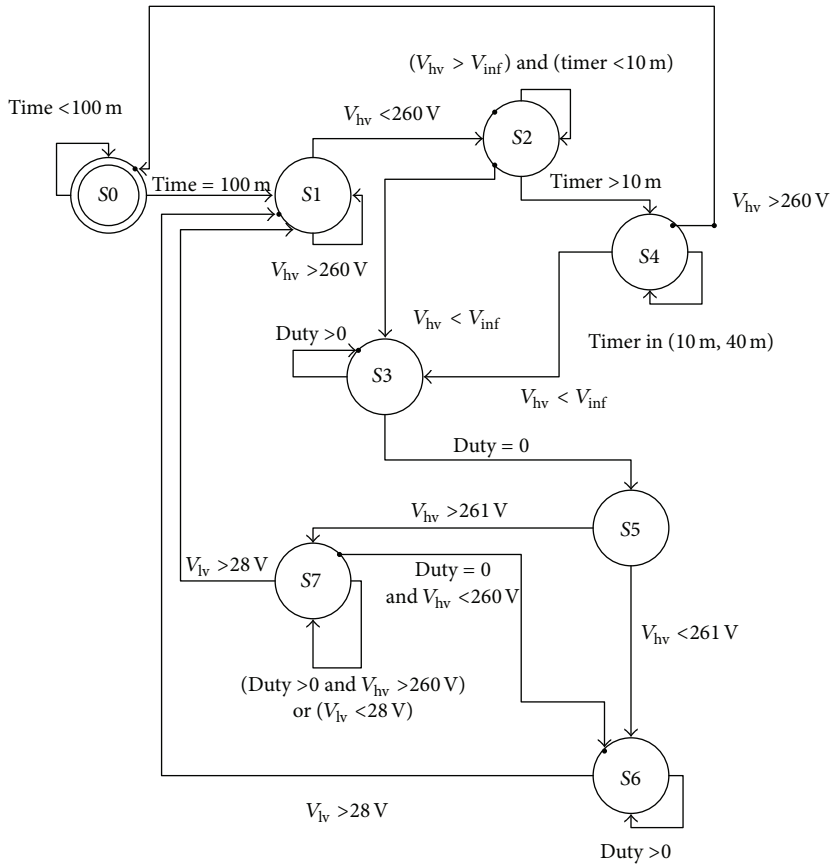

Figure 11: Buffer mode state machine.

output voltage. The robustness test is passed also in boost mode, as reported in Figures 14 and 15, where the disturbance induced by the load connection at $t = 500$ ms is fully rejected, regulating the output voltage at 270 V for both behavioral and functional schemes.

5.3. Experimental Results. To validate the proposed converter realization, starting from the results of the design phase and taking into account the simulation stage, a real prototype has been realized, performing different tests in order to validate the converter as an electronic equipment suitable for

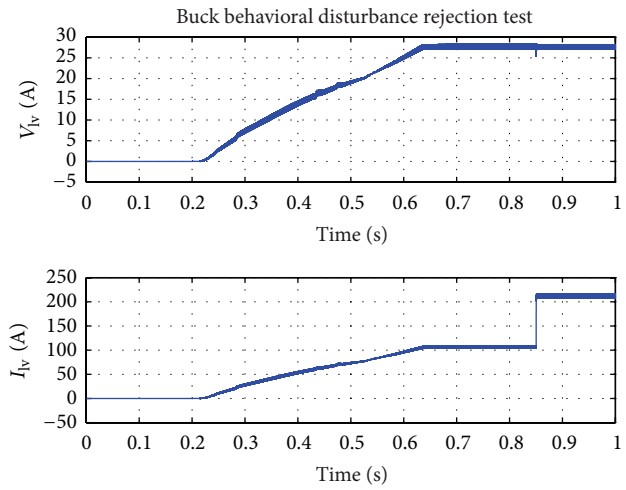

Figure 12: Buck mode test for behavioral robustness test.

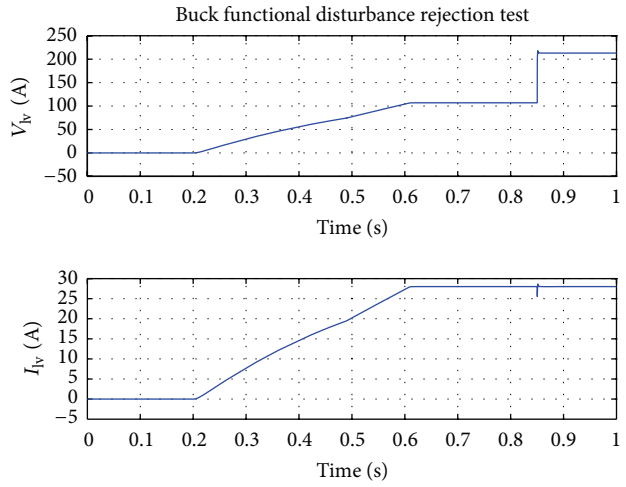

Figure 13: Buck mode test for functional robustness test.

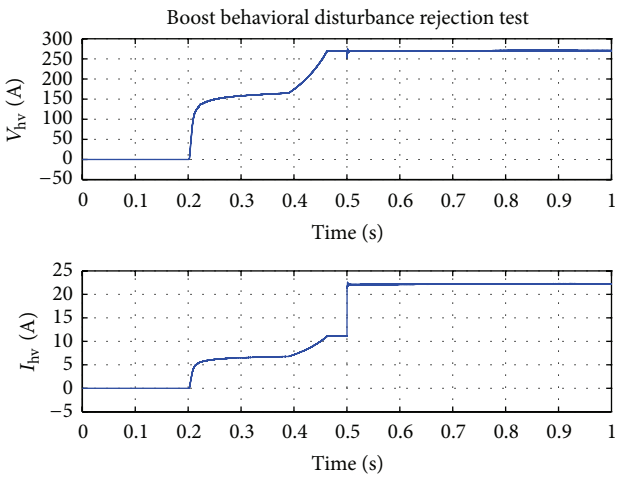

Figure 14: Boost mode test for behavioral robustness test.

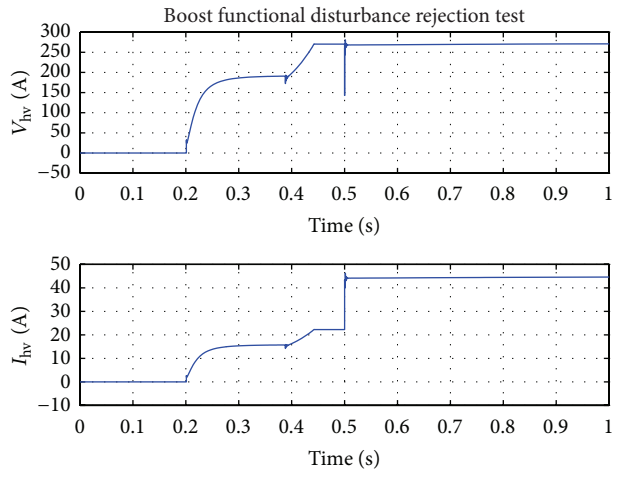

Figure 15: Boost mode test for functional robustness test.

insertion in a complex aeronautical electrical network. Main hardware components adopted for converter realization are summarized in Table 1.

High currents are very critical because large value of di/dt can destroy electronic devices. For this reason, a special care has been adopted in order to avoid this dangerous event. To limit the effects of leakage inductances, all conductors have been realized as short as possible, in close proximity of the return current path. Furthermore, stray inductance of the low-voltage full bridge is another important point. Therefore, the converter has been realized adopting a multilayer technique. A single converter cell differs only for the auxiliary electronics, while main cell is deputed to control and logic function. All the cells embed the same boost full bridge converter core and have been assembled in 19″ rack cases. A picture of the final converter, where all the components have been placed in four distinct modules, is reported in Figure 16.

Different tests have been performed in both buck and boost modes, to demonstrate how the converter meets specifications in both operating modes, first validating single cell and next performing some dedicated test for the entire converter. In boost mode single cell test, reported in Figure 17, the active clamp presence is evident due to its overvoltage limiting action, fundamental to reduce the stress for the power MOSFET at voltage less than the $V_{DS_{MAX}}$ accepted by the device. The following measurements have been recorded by an oscilloscope during the test: $V_{HV} = 272$ V, $V_{LV} = 23.4$ V, $I_{LV} = 43.5$ $\delta = 0.67$, and $\eta = 0.91$.

From Figure 17, considering an efficiency $\eta = 0.91$ for this test case, the apparent power at the transformer terminals can be, respectively, given as $P_{in} = 1.020$ KVA and $P_{out} = 0.926$ KVA. Anyway, these values strongly depend on the actual duty cycle, where the efficiency increases with the duty until a certain critical point [23]. A critical point of the entire project is the start-up phase in boost mode, because converter has to change modulation scheme as reported in Section 2.3. Proposed start-up scheme does not involve external circuit, but only a variation in the modulation strategy. In Figure 18 a test performed on a single cell is reported. This test evidences the typical waveform of the high voltage regulated by the

Figure 16: Assembled converter: front and rear.

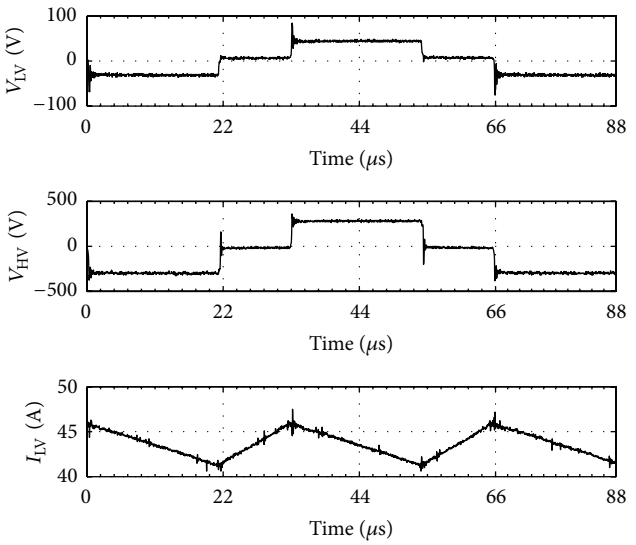

Figure 17: Boost mode test of a single cell: input: V_{LV} = 23.4 V, avg(I_{LV}) = 43.5 A, and δ = 0.677; output: V_{HV} = 272 V.

Table 1: Converter main electrical components.

Item	Parameter
Inductor $L1$	10 μH
Inductor $L2$	100 μH
Capacitor $C1$	0.2 mF
Capacitor $C2$	10 mF
Capacitor $C3$	470 μF
Transformer turns ratio n	7.5
MOSFET	3x IRF2907 (V_{DSS} = 75 V, I_D = 90 A)
IGBT	IRG4PC50UD (V_{CES} = 600 V, I_C = 27 A)
Switching frequency	15 kHz

converter that behaves like a buck converter if δ <0.5 and a boost converter if $\delta \geq 0.5$.

In Figure 19 a variation of the load in boost mode is reported to study the control dynamics. It must be pointed out

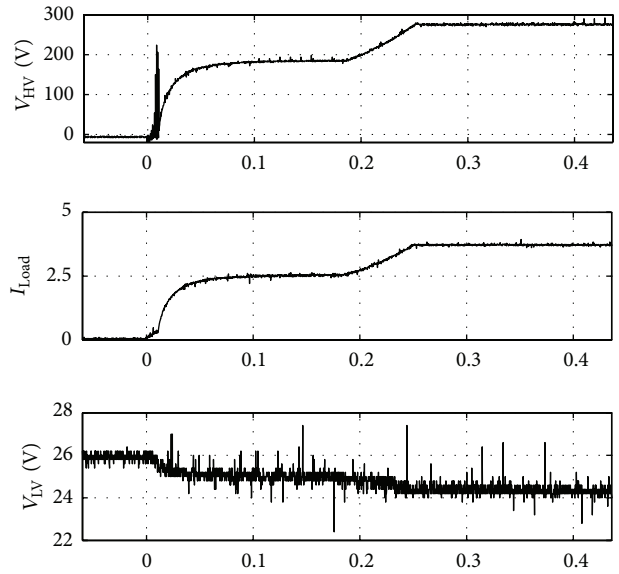

Figure 18: Start-up phase of converter in boost mode, R_{LOAD} = 74 Ω.

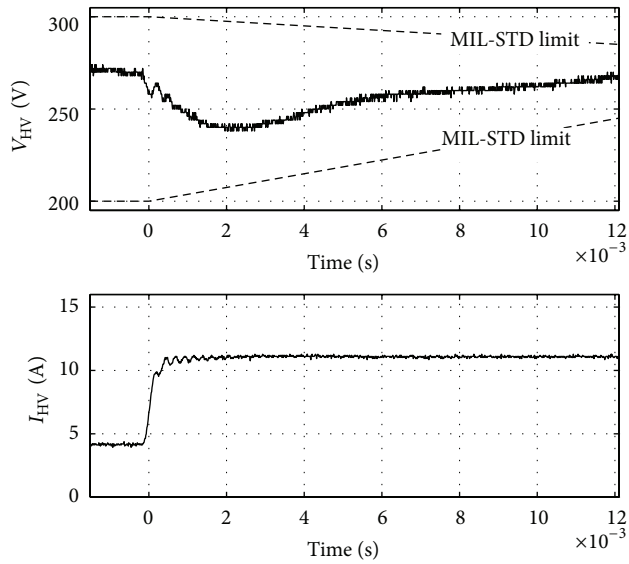

Figure 19: Boost test, variation of load: 1.5 kW → 3 kW.

that the output voltage does not overcome MIL-STD-704F thresholds, evidenced in the same figure.

5.4. Buffer Mode Simulations and Experimental Results. Buffer mode results are particularly significant in order to test effectiveness of FSM approach. In fact, as evident in Figure 11, the buck state machine is fully reused in Buffer state machine construction. Furthermore, a fully representative test can be performed by simply traversing all state machine paths and selecting ad-hoc conditions in order to enable the complete transition set.

The SABER testbench adopted for buffer complete test is reported in Figure 20.

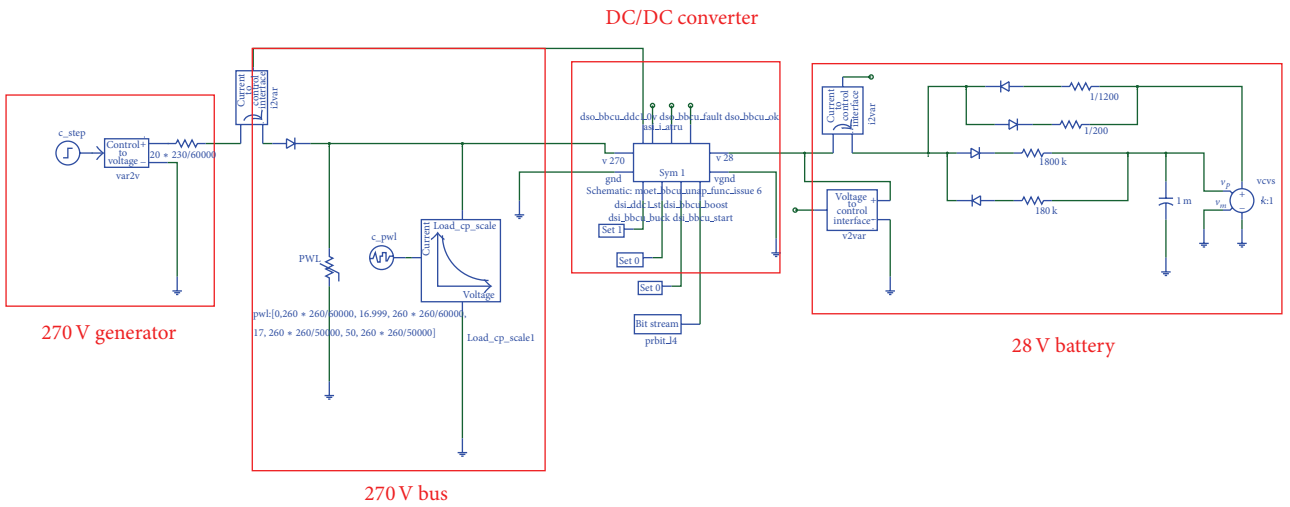

Figure 20: Test bench used for buffer mode.

The DC/DC converter is connected to a 270 V bus, represented by a variable resistor and a dynamic load specified in terms of power absorbed by the bus. From the combined effect of these blocks, it is possible to reproduce occurring/vanishing of overload conditions. Besides, the voltage generator source is Thevenin-modeled in order to obtain an initial condition of 260 V@60 kW bus absorbed power, and the 28 V battery is modeled as a voltage controlled voltage source, whose charge/discharge times are simulated through a diode-based circuit. Due to an excessive simulation time required for behavioral scheme, only functional tests have been performed for buffer mode. In details, referring to Figure 21, the state sequence is the following.

$S0-\cdots-S7-S6-S1-\cdots-S6-S1-\cdots-S7-S1$.

In Figure 21, 270 V bus voltage and current, battery voltage, and duty cycle values are reported, marking at the top of the figure each result subset with the corresponding buffer state.

First transition, from $S0$ to $S7$, is an overload condition that can be solved by entering partial buck mode, where the battery is recharged only partially. Successively, in $S7$ to $S6$ transition, an additional load is activated at the high-voltage side, and the boost mode is entered. Successively, overload condition is removed and initial buck mode becomes the current state. During the second logical succession of states (i.e., $S1$ to $S6$), a critical overload condition is simulated and boost state is directly reached. As for the first test, successively normal operative condition is restored and the converter operates again in initial state. Finally, the bus voltage collapses due to battery full recharge effect, entering $S6$ state from $S1$, but now the converter is able to deliver enough current to the battery, obtaining 28 V nominal voltage at its terminals. The net effect is $S6$–$S1$ transition enabling, completing the third logical state sequence and also the buffer complete test.

Once the simulation phase has been performed, it is possible to implement buffer logic also for real equipment. As for buck and boost state machines, also buffer logic microprocessor firmware has been derived from SABER MAST

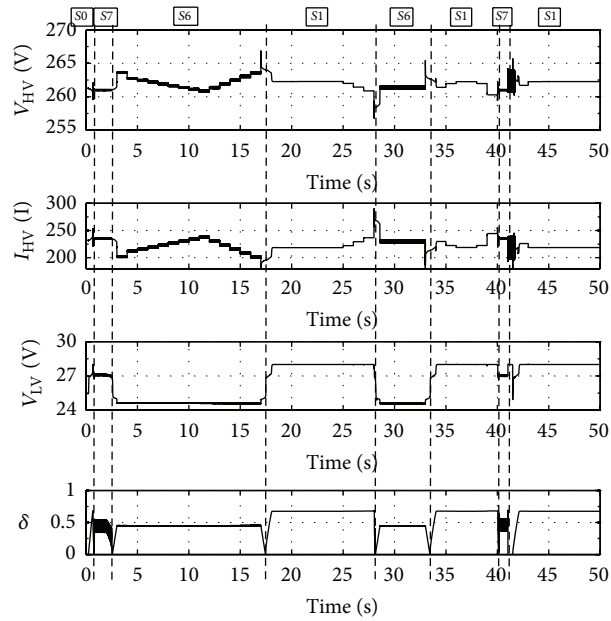

Figure 21: Buffer mode test results.

language, in particular for a Microchip *dsPIC33FJ256GP710* target controller. The testbench is composed of a battery pack at 28 V nominal voltage and an adjustable voltage supply initially set to 270 V. The overload condition has been realized by gradually decreasing high-side voltage and increasing it in order to restore standard conditions.

Transitions buck-to-boost and boost-to-buck are, respectively reported in Figures 22 and 23 as particularly interesting operative conditions for buffer logic. The waveforms acquired by the oscilloscope are reported, where Channel 1 (in yellow) is for high-side voltage, Channel 2 (in blue) for low-side voltage, and Channel 3 (in purple) for low-side current.

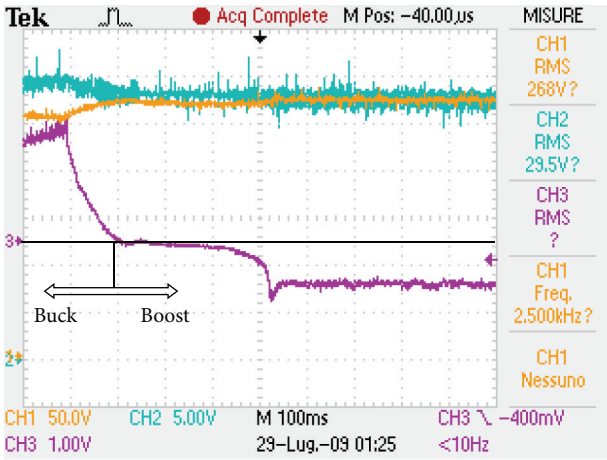

FIGURE 22: Transition buck to boost in buffer experimental test.

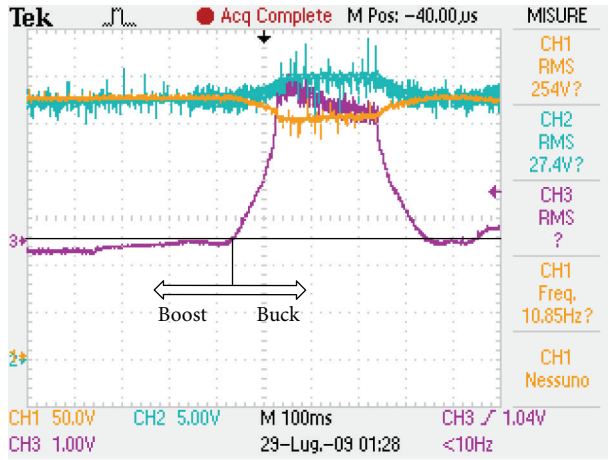

FIGURE 23: Transition boost to buck in buffer experimental test.

Considering Figure 22, the mode change from buck to boost is evident at 100 ms, where the high-side voltage increases and the battery current begins to flow in the opposite direction. If the end of power quality impairment is detected, the buffer state machine condition returns to full buck mode (i.e., it returns to *S*1 state). This event is reported in Figure 23, where the buck mode starts but the network cannot sustain the full charge of the battery. For this reason, the converter state become battery refresh mode (i.e. *S*7 status), where buck conversion with a reduced duty cycle is performed.

6. Conclusions and Future Works

In this paper, the entire process of design, realization, and testing of a bidirectional DC/DC converter for aeronautical applications has been exposed. Starting from typical aeronautical requirements and constraints, first an electrical structure (i.e., boost full bridge cellular converter) has been proposed, focusing on benefits derived from this approach. The presence of a transformer for each cell is a critical design point [23], requiring an accurate selection of the optimal turns ratio. After electrical plant and modulation schemes selection, a PI controller, modified with protections in order to avoid electrical damage to the converter, has been proposed. A particular approach based on finite state machines has been selected for high-level supervision, in order to obtain a greater writing process simplicity but, at the same time, a precise description of the converter behavior in each operative condition, mainly due to the formal framework of the automaton-based processes. The buck and boost state machines have been exposed, and successively the buffer mode concept has been introduced and implemented through a dedicated state machine, demonstrating the usefulness of the FSM approach in terms of code reusability and logical description of events sequence, compared to usual sequential approach for code writing. Finally, testing stage has involved both simulation and experimental results. Different simulative and experimental tests have been performed, and the obtained results demonstrate the successful conclusion of the converter creation process.

Different conclusions can be drawn, starting from the key points of the work discussed in the present paper. The buffer mode, extensively discussed, is here considered as an innovative technology able to solve the delicate problem of automatic voltage regulation on high-voltage bus, with respect to power quality standards. However, its application range can be extremely wide (e.g., hybrid vehicles, telecommunications, railway transports, etc.). The only condition to be respected by a converter in order to implement buffer logic is the possibility to regulate the power flow direction and impose it to zero value if required, together with the presence of a magnetic coupling element (i.e. a transformer), in order to permit the coexistence of different voltage sources on the same bus.

Another key point of this paper is the finite state machine approach for the supervision of the converter. Note that the supervisory control of hybrid systems is the reference framework for a rigorous approach, in order to remove the appearance of undesirable behaviors.

Finally, the presence of intelligence onboard the converter suggests for us an interesting application of the proposed converter, in contrast to the usual centralized approach for the aeronautical electrical networks. In fact, equipping each PEPDC power converter with a buffer-like strategy could confer a high degree of autonomy to the network, due to the ability of energy flows redirection where required, depending on the actual network status. Different studies on these topics are currently ongoing, as well as two international patents requests for the buffer mode here discussed.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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