Research Article

Analysis of Power Transfer Efficiency of Standard Integrated Circuit Immunity Test Methods

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Received 23 January 2015; Accepted 15 April 2015

Academic Editor: Jiseong Kim

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Direct power injection (DPI) and bulk current injection (BCI) methods are defined in IEC 62132-3 and IEC 62132-4 as the electromagnetic immunity test method of integrated circuits (IC). The forward power measured at the RF noise generator when the IC malfunctions is used as the measure of immunity level of the IC. However, the actual power that causes failure in ICs is different from forward power measured at the noise source. Power transfer efficiency is used as a measure of power loss of the noise injection path. In this paper, the power transfer efficiencies of DPI and BCI methods are derived and validated experimentally with immunity test setup of a clock divider IC. Power transfer efficiency varies significantly over the frequency range as a function of the test method used and the IC input impedance. For the frequency range of 15 kHz to 1 GHz, power transfer efficiency of the BCI test was constantly higher than that of the DPI test. In the DPI test, power transfer efficiency is particularly low in the lower test frequency range up to 10 MHz. When performing the IC immunity tests following the standards, these characteristics of the test methods need to be considered.

1. Introduction

Advances in integrated circuit (IC) design technology have increased the density of transistors and made the structure of ICs more complex. Furthermore, the operating frequency of ICs has increased. The increase in density and high operating frequency of ICs has made the influence of electromagnetic fields on devices more complex and difficult to analyze. In addition, there are higher expectations for the performance of ICs in terms of electromagnetic immunity, because most ICs operate in environments with electromagnetic waves and disturbance signals. Therefore, the method used to predict the electromagnetic immunity level of an IC during the design stage is extremely important.

IEC proposed standards for direct power injection (DPI) and bulk current injection (BCI) [1–3] methods to measure the conductive immunity of ICs to radio-frequency (RF) current and power induced by electromagnetic disturbance. In the DPI method, the RF disturbance power is injected to ports of the device under test (DUT) via a coupling capacitor

to cause failure in operation of the DUT. In the BCI method, RF power is injected to cause failure of the DUT by the BCI probe. The maximum forward power level where the DUT still operates correctly is the electromagnetic immunity level of the DUT. Injected RF power is transferred to the chip through noise injection paths including cables, injection capacitors, injection probes, and traces. Some portion of the injected noise power is therefore consumed in the injection path. The actual power that causes chip failure is thus different from the forward power measured at the generator.

In related work [4], the authors derived an equation for the power transfer efficiency of the bulk current injection method. Power transfer efficiency was determined as the ratio of power transferred to the chip and the forward power at the RF generator. This equation was confirmed by Agilent Design Systems (ADS) [5] simulation and then applied to estimate the real injected power at the failure point of a DUT operation.

In this paper, the power transfer efficiency of the DPI/BCI methods is derived and calculated based on equivalent circuit

FIGURE 1: The concept of IC immunity test. (a) DPI test. (b) BCI test.

models of the noise injection path [6–9]. Scattering parameter measurements are used to validate the accuracy of the equivalent circuit models. The immunity of a clock divider IC is tested by DPI and BCI methods and the power transfer efficiencies are obtained. The immunity level of the clock divided circuit is evaluated as the ratio of the power measured at the RF source to the real injected power at the input of the DUT. The DPI power transfer efficiency is compared with the BCI power transfer efficiency, and differences between the two methods were analyzed. The analysis of the power transfer efficiency of the DPI method suggests that there is a significant amount of injected noise power loss due to the reflection at the input port.

The rest of this paper is structured as follows. Derivation of the power transfer efficiency equation is shown in Section 2. In Section 3, the DPI and BCI equivalent circuit models are explained. Results and discussions are presented in Section 4. Concluding remarks are provided in Section 5.

2. Power Transfer Efficiency Derivation

Figure 1 shows the basic concept underlying the DPI and BCI test methods. Noise power is generated from a RF generator and injected to the DUT via a coupling capacitor in the DPI method versus a BCI probe in the BCI method. Noise power flows through injection components and PCB traces before entering the chip. The injection path from the RF generator to the chip can be considered to be a two-port network, as shown in Figure 2. The two-port network can be divided into three main parts: RF source, injection path, and load, as shown in Figure 2(a). Figure 2(b) shows the RF power flow and the related scattering parameters. The RF generator has a matching output impedance of $Z_s = 50 \Omega$.

The power transfer efficiency, H_p , is defined as the ratio of power at the load (P_L) and forward power measured at

the RF source (P_s) of the two-port network of Figure 2(b) as expressed in the following equation:

$$H_p = \frac{P_L}{P_s}. \quad (1)$$

The forward power reported from the RF generator is the power transmitted to the load when the load impedance matches Z_s , and the forward power of the RF generator is expressed as follows:

$$P_s = \frac{1}{8} \frac{V_s^2}{Z_s}. \quad (2)$$

The relationship of V_1 , V_2 , and the scattering parameters is expressed in (3) from the signal flow graph shown in Figure 2(b) [10, 11]. Consider

$$\begin{aligned} V_1^- &= S_{11}V_1^+ + S_{12}V_2^+ = S_{11}V_1^+ + S_{12}\Gamma_L V_2^-, \\ V_2^- &= S_{21}V_1^+ + S_{22}V_2^+ = S_{21}V_1^+ + S_{22}\Gamma_L V_2^-. \end{aligned} \quad (3)$$

Using (3), the power transferred to the test chip, P_L , can be expressed as follows [4]:

$$\begin{aligned} P_L &= \frac{1}{2Z_0} (|V_2^+|^2 - |V_2^-|^2) = \frac{1}{2Z_0} |V_2^+|^2 (1 - |\Gamma_L|^2) \\ &= \frac{V_s^2}{8Z_0} \left| \frac{S_{21}}{1 - S_{22}\Gamma_L} \frac{1 - \Gamma_s}{1 - \Gamma_s\Gamma_{in}} \right|^2 (1 - |\Gamma_L|^2). \end{aligned} \quad (4)$$

FIGURE 2: (a) The 2-port circuit network diagram of the BCI test. (b) The flow of RF power with the scattering parameters and the reflection coefficient.

Γ_s , Γ_{in} , and Γ_L are the reflection coefficients at the source, input port, and load, respectively. Consider

$$\begin{aligned}\Gamma_s &= \frac{Z_s - Z_0}{Z_s + Z_0}, \\ \Gamma_{in} &= \frac{V_1^-}{V_1^+} = S_{11} + S_{12}\Gamma_L \frac{V_2^-}{V_1^+}, \\ \Gamma_L &= \frac{Z_L - Z_0}{Z_L + Z_0}.\end{aligned}\quad (5)$$

Finally, the equation for power transfer efficiency is derived as follows:

$$H_p = \frac{P_L}{P_s} = \frac{Z_s}{Z_0} \left| \frac{S_{21}}{1 - S_{22}\Gamma_L} \frac{1 - \Gamma_s}{1 - \Gamma_s\Gamma_{in}} \right|^2 (1 - |\Gamma_L|^2). \quad (6)$$

Practically, the power at the injection port of the DPI/BCI test, which is measured at node V_1 , is different from the forward power due to impedance mismatch of the RF source and the rest of the DPI/BCI network. The power at the input

of the noise injection port (P_{in}) considering the reflections at the injection equipment is calculated as follows:

$$\begin{aligned}P_{in} &= \frac{1}{2} |Z_1| |I_1|^2 \\ &= \frac{V_s^2}{8Z_0} \left| \frac{1}{1 - \Gamma_s\Gamma_{in}} \right|^2 (1 - \Gamma_s)^2 (1 - |\Gamma_{in}|^2).\end{aligned}\quad (7)$$

3. Equivalent Circuit Model

To determine the DPI/BCI power transfer efficiency, accurate equivalent circuit models for the injection capacitor, injection probe, PCB, package, and IC are needed.

3.1. Chip Model. The chip model includes the equivalent circuit model of the package and schematic netlist and parasitic interconnection of the IC. The DUT package is a 208-pin quad flat package (QFP).

The IC used in this work is a clock divider that divides the input clock into two lower frequency clocks by a factor of four and sixteen, respectively. The clock divider was designed using a 180 nm Magna process. The block diagram and operation of the clock divider are shown in Figure 3. We evaluated the RF noise immunity of the clock divider when noise was injected to the supply voltage, VDD. The parasitic

FIGURE 3: Clock divider block and function.

FIGURE 4: IC parameter extraction set-up.

RC components were added to the netlist of the IC using Calibre xRC of Mentor graphics [12] based on the layout created by Cadence [13].

To capture the IC reflection characteristics and to perform simulations using ADS, the reflection coefficient $S(1, 1)$ of the VDD pin of the clock divider design references to the VSS pin was extracted from the simulation setup shown in Figure 4. $S(1, 1)$ was extracted and imported to ADS as the chip core model.

The dimensional parameters of package pins, lead frames, and package bonding wires were determined by measuring X-ray pictures of the chip package as shown in Figure 5. The equivalent circuit model was obtained using (8) derived from [14]. In the equations, w is the width, t is the thickness, l is the length, and h is the height of the conductor. Consider

$$R = \rho \left(\frac{l}{w \times t} \right),$$

$$L = \frac{\mu_0 l}{2\pi} \left[\ln \left(\frac{8h}{w + t} + 1 \right) \right],$$

$$C = \epsilon_0 \epsilon_r l \left[1.13 \left(\frac{w}{h} \right)^1 + 1.44 \left(\frac{w}{h} \right)^{0.11} + 1.46 \left(\frac{w}{h} \right)^{0.42} \right].$$
(8)

The package equivalent circuit model shown in Figure 6 was connected to the IC core model. The VDD/VSS port

FIGURE 5: X-ray picture of the chip package.

impedance of IC is shown in Figure 7(a). The $Z(1, 1)$ parameter of the circuit including the package and IC core was simulated by ADS and the simulation model is shown in Figure 7(b). The same $Z(1, 1)$ parameter was determined by measuring the real chip and compared with simulation results to validate the package and IC core model. The comparison results are shown in Figure 7(c).

3.2. DPI Capacitor and BCI Probe Circuit Models. Accurate impedance of the capacitor was obtained from its datasheet. For the High Q/Low ESR (equivalent serial resistor) capacitor model, the ESR value was specified in the product specifications. Using the capacitor value and the resonant frequency specified in the datasheet, the equivalent serial inductance was calculated using (9):

$$L = \frac{1}{4\pi^2 f_{res}^2 C}, \quad (9)$$

where f_{res} is the resonant frequency of the capacitor. The DPI capacitor equivalent circuit is the combination of the ESR, ESL, and capacitor connected in serial. The mounting pad parasitic of the DPI capacitor was part of the PCB; thus it will be considered in the PCB model. Details of the structure of the DPI capacitor equivalent circuit and its impedance are provided in Figure 8.

An equivalent circuit model of the BCI probe was created using the method specified in related work [4, 7]. The BCI probe model was F130-1 from Fisher Custom Communications, Inc. The equivalent circuit model of the BCI probe and its insertion loss $S(2, 1)$ are shown in Figure 9.

3.3. PCB Modeling. The PCB used in this paper was designed with four layers, as shown in Figure 10. The injection trace and the DPI capacitor were located in the top layer. The second and the third layers were the ground and VDD plane, respectively. The fourth layer was an additional trace to measure the output signal of the DUT. The width of all the traces on the PCB was designed so that the PCB had a characteristic impedance of 50 Ω . The total thickness of

FIGURE 6: Equivalent circuit model of the package.

FIGURE 7: Chip model validation. (a) VDD/VSS port impedance of IC. (b) Package and IC simulation setup. (c) Chip VDD/VSS port impedance $Z(1, 1)$ comparison.

FIGURE 8: Impedance and equivalent circuit model of the DPI capacitor.

FIGURE 9: Insertion loss and equivalent circuit model of the BCI probe.

FIGURE 10: PCB dimensional structure.

the PCB was 0.8 mm, while the distance between the top and ground plane was 0.11 mm and the copper thickness was 0.035 mm. The dielectric layer was prepreg with $\epsilon_r = 4.11$.

Figure 11 shows the PCB used in the DPI test. The SMA connector was used at the injection port and the power supply port. A pad was located in the middle of the transmission trace to mount the DPI capacitor. The DPI transmission trace was divided into segments. PCB traces were located over a ground plane in the second layer; thus they are approximately modeled as a microstrip structure [15]. Each segment was modeled as a RLCG L -network as shown in Figure 12(a). The R , L , G , and C values of the L -network are calculated using the following equation:

$$\begin{aligned} C &= \epsilon_0 \epsilon_r \frac{a \times b}{d}, \\ L &= \mu_0 d \frac{b}{a}, \\ G &= 2\pi f C \tan \delta, \\ R &= R_{dc} + R_{ac} = \frac{2}{\sigma_c t} \left(\frac{b}{a} \right) + 2 \left(\frac{b}{a} \right) \sqrt{\frac{\pi f \mu_0}{\sigma_c}}. \end{aligned} \quad (10)$$

a is the trace length, b is the trace width, d is the dielectric thickness, and t is the conductor thickness. Each trace should be divided into a number of segments whose lengths are less than one-tenth of the wavelength at the maximum test frequency. A similar modeling methodology, π -segment, was applied to the vias used to mount the SMA connect on a PCB [16].

FIGURE 11: Overview of PCB trace used in DPI test.

To experimentally validate the accuracy of the equivalent circuit model of the noise injection path of the DPI, which included the PCB and DPI capacitor, simulations were performed using ADS to generate the insertion loss between port 1, which is the injection port, and port 2 at the chip footprint, as shown in Figure 11. $S(2, 1)$ of the real PCB was measured by VNA and compared with the simulation results to validate the PCB equivalent circuit model, as shown in Figure 12(b).

The overall equivalent circuit model of the DPI and BCI test method was constructed by combining all the circuit components described above. The final equivalent circuit model structures of DPI and BCI are shown in Figure 13. The cable used to connect from RF source to input port was 50 Ω coaxial cable, but the power loss in those cables was neglected in the simulation.

4. Simulation and Measurement Results

The experimental set-up for the DPI test is specified in IEC 62132 part 4 while the BCI test set-up is specified in part 3, as shown in Figure 14. In the standard, the test frequency range is 150 kHz~1 GHz. The overall simulation model was specified in the previous section, and the simulation was performed using ADS.

The normal operation output of CLK1 of the clock divider chip, which was used as the DUT of the immunity test, is shown in Figure 15(a). RF disturbance power was injected to the power pin (VDD) of the clock divider. The function generator provided the input clock, and the period jitter of the clock output (CLK1) was measured by oscilloscope to determine failure. The clock cycle of the input clock from the function generator was 100 ns, and the period of the CLK1 was 400 ns in simulation. The actual measurement results show that the period of CLK1 signal varied in a range of 399 ns~401 ns (± 1 ns) in normal condition. Therefore, in DPI/BCI

FIGURE 12: Validation of PCB equivalent circuit model including DPI capacitor. (a) Equivalent circuit model of a segment. (b) $S(2,1)$ comparison.

FIGURE 13: Overall simulation model.

(a)

(b)

FIGURE 14: Chip immunity test setup. (a) DPI test. (b) BCI test.

(a)

(b)

FIGURE 15: Measurement results of clock divider operation. (a) Operation under normal conditions. (b) Operation under failure conditions.

FIGURE 16: Power transfer efficiency (H_p) comparison. (a) DPI method. (b) BCI method.

FIGURE 17: Comparison of power transfer efficiency under different load conditions. (a) DPI method. (b) BCI method.

test, the clock divider was considered to have failed when the period of CLK1 was out-of-range by more than ± 1 ns, as shown in Figure 15(b).

The power transfer efficiencies (H_p) of the BCI and DPI methods were calculated using the equations proposed in Section 2 and compared with ADS simulations results to validate our model. The overall equivalent circuit model for ADS simulation is shown in Figure 13. A scattering parameter for all components in the BCI and DPI two-port networks was used to calculate the power transfer efficiency using the proposed equation. Simulated and calculated BCI and DPI power transfer efficiencies are compared in Figures 16(a) and 16(b). The load condition of the result in Figure 16 is the chip impedance, which is the input impedance of the VDD/VSS port of the clock divider chip as shown in Figure 7. Chip impedance includes the package and chip core equivalent circuit model. The power transfer efficiency (H_p) calculations and ADS simulation results matched well.

To further understand DPI/BCI power transfer efficiency and analyze the effect of load condition on efficiency,

DPI/BCI power transfer efficiency was plotted for two load conditions: a $50\ \Omega$ load and the chip impedance load. When applying chip impedance to the load, power transfer had complex fluctuations due to the complexity of the chip impedance. The results obtained for DPI and BCI with two different loads are shown in Figures 17(a) and 17(b), respectively. Load condition did affect the power transfer efficiency of both DPI and BCI methods.

For a perfect $50\ \Omega$ load, the power transfer efficiency was affected only by the injection path. DPI and BCI power transfer efficiencies were compared for the same $50\ \Omega$ load condition, as shown in Figure 18. At low frequencies, the BCI method had a higher efficiency than the DPI method. In particular, in the frequency range from 1 MHz to 300 MHz, the power transfer efficiency of the BCI method increased significantly due to the design bandwidth of the BCI probe model F130. The DPI power transfer efficiency crossed over the efficiency of BCI in frequency from 150 MHz to 6 GHz. The declination of power transfer efficiency of the DPI method was faster than that of the BCI method in

FIGURE 18: Comparison of DPI and BCI power transfer efficiency. (a) With $50\ \Omega$ load. (b) With chip VDD/VSS port impedance load.

FIGURE 19: Measured forward power (P_s) and calculated real injected power (P_L) by the power transfer efficiency (H_p (dB)) with chip load. (a) DPI. (b) BCI.

the frequency range higher than 4 GHz due to the slope of the power transfer efficiency.

The immunity of the clock divider chip was tested using DPI and BCI test methods under the test conditions specified in the previous section. The forward power (P_s) was measured at each frequency when the chip operation failed. The proposed power transfer equation was applied to calculate the actual delivered power to the chip, which can be used as the actual immunity level of the chip. Delivered power to the chip, P_L , was calculated from (11), which is a result of H_p in (6). Consider

$$P_L \text{ (dBm)} = P_s \text{ (dBm)} + H_p \text{ (dB)}. \quad (11)$$

The DPI/BCI immunity test results for the IC using forward power (P_s) measured at the RF source and real injected power (P_L) calculated from power transfer efficiency are compared in Figure 19.

To analyze the reason for the declination in power transfer efficiency, the forward power at source was set at 0 dBm, and

the power at the input port of the DPI and BCI network (P_{in}) was calculated using (7) and plotted in Figure 20. Due to impedance mismatch, the forward power from the RF source was reflected at the input of the DPI/BCI test equipment. The reflection coefficient $S(1,1)$ parameter of DPI and BCI method is plotted in Figure 21. At low frequencies up to 1 MHz, the reflections of both DPI and BCI method are significantly high; thus most of the forward power is reflected at the input port. From 1 MHz, the reflections are reduced, and the power entering DPI and BCI network increases. The reflection coefficient of BCI was reduced significantly at frequency range of 10~100 MHz and that of DPI was reduced at 100 MHz~1 GHz. These properties explain the differences of the power transfer efficiency between DPI and BCI methods as shown in Figure 18. At high frequencies, a significant amount of power was reflected at the input of the DPI/BCI test equipment due to the increase of the reflection coefficient. Therefore, power transfer efficiency decreases at high frequencies.

FIGURE 20: Comparison of DPI and BCI input power (P_{in}). (a) With $50\ \Omega$ load. (b) With chip VDD/VSS port impedance load.

FIGURE 21: Comparison of DPI and BCI input reflection $S(1, 1)$ with chip VDD/VSS port impedance load.

5. Conclusions

In this paper, model based equations for the power transfer efficiency of the DPI and BCI methods, defined in IEC 62132-3 and IEC 62132-4, were derived. In the DPI and BCI tests, the RF noise power is delivered to the chip through an injection path including the DPI capacitor or BCI probe, traces, and wires. From the power transfer efficiency, the loss when RF power passes through the injection path can be estimated. The real injected power which reflects the actual immunity level of the device under test can be calculated using power transfer efficiency equation. The DPI and BCI immunity tests are performed for the clock divider IC. The magnitudes of the real power that reach the test IC at the chip failure point for each standard immunity test methods are determined using the proposed model.

The power transfer efficiencies and the reflected input power of the DPI and BCI test methods are compared. For the test frequency range of 150 kHz to 1 GHz, which is defined in the standard, the power transfer efficiency of BCI method is constantly high. In the DPI test, with a default capacitor value

of 6.8 nF, the power transfer efficiency is particularly low in the lower test frequency range up to 10 MHz. This means that even though the engineers perform the DPI test on the IC, due to the high loss in the noise injection path, the RF noise will not reach the IC. If the value of the DPI capacitor is selected to be smaller than 6.8 nF, the low frequency range having small power transfer efficiency is expanded. In future IEC IC immunity test standards, these aspects of the DPI test should be considered.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (no. NRF-2014R1A2A2A01006595). This work was supported by the IC Design Education Center (IDEC).

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