Research Article

Calibration Techniques for Low-Power Wireless Multiband Transceiver

Shouyi Yin,[1,2] Jianwei Cui,[1,2] Leibo Liu,[1,2] and Shaojun Wei[1,2]

[1] *Research Center for Mobile Computing, Tsinghua University, Beijing 100084, China*
[2] *Institute of Microelectronics, Tsinghua University, Beijing 100084, China*

Correspondence should be addressed to Shouyi Yin; yinsy@tsinghua.edu.cn

The low-power wireless transceiver is the basic silicon building block of wireless sensor networks and the internet of things. In this paper, two digital calibration and compensation techniques for low-power wireless multiband transceiver are presented to adjust the VCO's tuning curves in the frequency synthesizer and eliminate the DC offset voltage in the intermediate frequency (IF) pathway. The fuzzy binary search method is applied to VCO calibration, and gain-based DC offset cancellation (DCOC) is applied. Based on these proposed methods, a multiband transceiver is designed and fabricated in 0.18 μm CMOS with 1.8 V voltage supply. Experimental results show that with 24 MHz system clock, frequency synthesizer calibration can be completed within 450 without requiring any additional calibration prescaler, achieving a calibration resolution of 1 MHz; DC offset voltage can be reduced to less than 3.5 mV for 0 to 60 dB gain, with each calibration process taking only 1.28 ms time. The proposed techniques and corresponding circuits are proved to be cost-efficient while maintaining high performance, which is suitable for multiband and multimode transceiver integration.

1. Introduction

Wireless communication is currently and will still remain as one of the most rapidly developing technologies. Over the past few decades, various short range wireless communication protocols have been proposed, such as IEEE 802.11 and Bluetooth. Wireless transceivers based on these protocols have been intensively studied, and many mature integrated solutions are proposed. Most of these solutions support a communication range of 10~100 m with relatively high data rate, but their power dissipation generally exceeds 100 mW.

In recent years, with the growing demand for universal wireless connections, many applications that have a looser requirement on communication range and data rate, but are very sensitive to power and cost, become increasingly popular, such as wireless sensor networks (WSNs), home automation, and the internet of things (IoT). Therefore, the low-power wireless transceiver is becoming the basic and most important silicon-building block of these applications. Considering the various requirements and environments of potential applications, the wireless transceiver should have a widely tunable frequency band and multiple working modes to adapt to different communication conditions.

This paper addresses the design and especially calibration techniques of multiband and multimode wireless transceiver. The major objective is to ensure expected data transmission rate while keeping its power dissipation low and area occupation small to match the requirements of WSN and IoT. As Figure 1 shows, the proposed transceiver consists of numerous circuit blocks such as LNA, image filter (which is incorporated in front-end LNA to eliminate image frequencies that might be down converted to the low IF band of interest), frequency synthesizer, down and up mixers, filters, programmable gain amplifiers (PGAs), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), low drop output (LDO) regulators, digital baseband, and digital control modules. The transceiver works in the 1.5–2.1 GHz and 375–525 MHz bands and employs MSK and FSK modulation techniques at the digital baseband. To adapt to different communication channel conditions, data transmission rate can be configured to 50 Kbps, 100 Kbps, and 200 Kbps. Though a homodyne structure has the advantage of
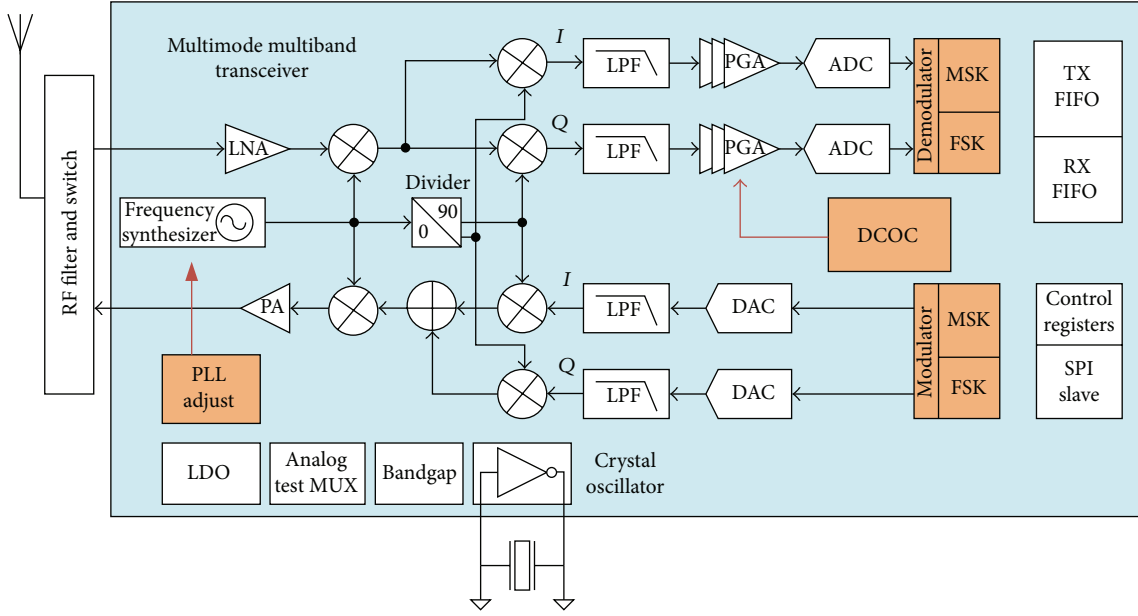
FIGURE 1: The architecture of multiband multimode transceiver.

saving the cost to implement front-end RF filter, it introduces a much higher level DC offset caused by self-mixing thus requires hardware as well as calibration time to cancel intermediate stage PGA DC offset, which is not attractive in the application where burst mode communication demands fast switching between RX and TX states. So, sliding intermediate frequency is adopted in the receiving path. The two different digital modulation circuits share the same analog and RF path for signal receiving and transmission. In such a mixed signal system, many trade-offs must be made.

One prominent challenge is to design a widely tunable frequency synthesizer that has fast lock time, low phase noise, low-power consumption, small area occupation, and constant performance across the entire tuning range. In our scenario, the synthesizer needs to cover the frequency band from 1.5 GHz to 2.1 GHz. If we use a 1.8 V supply voltage, the VCO gain will be at least 600 MHz/1.8 V = 333 MHz/V, which is so high that the phase noise will be unacceptably large. Usually in frequency synthesizer, the wide tuning range is realized by employing an LC-tuned VCO that has a switched capacitor array [1]. The array can be configured to different values to make the VCO operate on different tuning curves. Because each tuning curve can only cover a limited width of the entire tuning band, calibrating the VCO through hardware before the normal working process starts is essential. As for VCO calibration techniques, there have been some strategies presented so far [2, 3]. The period comparison method based on the time-to-voltage conversion [4] or the PFD-based edge comparison [5] work very fast, but they are complicated in structure and show speed-resolution limitations. Frequency counter-based linear search method is easy to implement but takes prohibitively long time, thus are not suitable for applications requiring fast channel switching capability. Conventional frequency counter-based binary search method

cannot guarantee the convergence to the most optimal tuning curve without a redundant comparison [6]. In addition, most of these techniques need extra calibration prescalers. In our design, we employ a modified fuzzy binary search method to guarantee the convergence to the most optimal tuning curve without a redundant comparison or any extra prescalers. The all-digital calibration block is easy to implement.

Another challenge arises from the sliding IF architecture. It suffers from the DC offset problem. The RF, LO leakage and process variation may both cause offset. The amplitude of the DC offset may be small (several micro volts) at generation, but after being amplified by the PGA chain by at most 60 dB, it can grow large enough to saturate poststage circuits. The distortion caused by DC offset can even make the ADC and digital baseband circuit unable to demodulate the received data. To solve this problem, DC offset cancellation (DCOC) circuit is indispensable. It is used to attenuate the differential mode DC offset and stabilize the DC operating point of IF circuits prior to normal receiving process. While low-power and wideband VGA have been reported before [7, 8], they consume large current and cannot provide accurate compensation because they do not compensate DC offset according to different IF gains. Also, conventional compensation techniques that work in a feedback way may suffer from stability problem [9]. In our design, a digital calibration method is adopted with a RAM storing the DC offset information of each gain. The IF analog circuit is divided into three stages, and the DC offset is compensated for each stage. With such a scheme, DC offset caused by device mismatch is effectively cancelled to below 3.5 mV within 1.28 ms for any gain word.

The rest of the paper is organized as follows. Section 2 describes the VCO calibration method in the frequency synthesizer. Section 3 presents the DC offset compensation
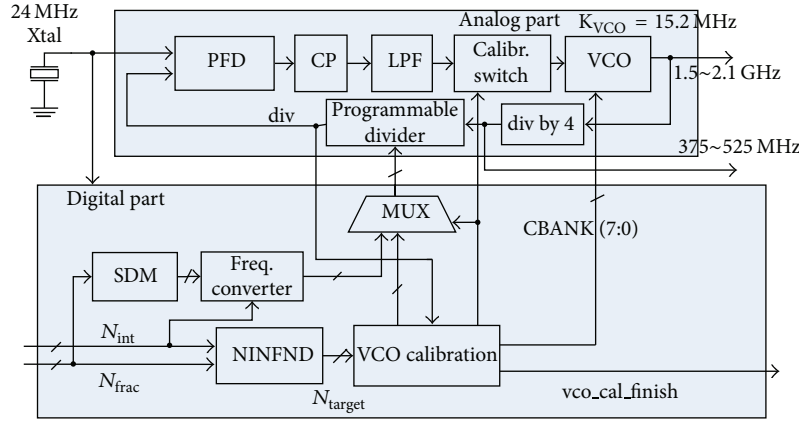
Figure 2: The 1.5–2.1 GHz fractional-N frequency synthesizer with Σ-Δ modulator and autocalibration module.

scheme. The implementation of the transceiver and test results are described in Section 4. Finally, we conclude in Section 5.

2. VCO Calibration in the Frequency Synthesizer

The local oscillation frequency needed by the transceiver is synthesized by a single loop fractional-N Σ-Δ PLL, as illustrated by the analog part in Figure 2. The output frequency of the VCO is tunable from 1.5 GHz to 2.1 GHz. After a divide-by-four module, a frequency tunable from 375 to 525 MHz can be obtained. In the analog part, the reference frequency is generated with an off-chip 24 MHz crystal oscillator. The PFD examines the phase difference between the reference frequency and the divided VCO output signal div. A charge pump receives the output of the PFD, and a configurable low pass filter (LPF) filters out the high frequency components of the signal from the charge pump and feeds the filtered output voltage to the VCO. The input voltage to the VCO has a swing from 0.4 to 1.4 V and can cover the frequency band from 1.475 to 2.215 GHz to provide enough band margin. The output of VCO passes through a divide-by-4 module and a Σ-Δ modulator (SDM) controlled programmable divider and then goes back to the PFD. To suppress the phase noise, we adopt a low K_{VCO} gain VCO with multiple subband tuning curves, controlled by an 8-bit trim word CBANK (7:0) which reduces K_{VCO} to 15.2 MHz/V at the vicinity of 0.9 V.

The traditional binary search method to obtain the CBANK value based on simple period comparison is very likely to deviate from the most optimal trim value by 1 LSB therefore cannot guarantee the convergence to the closest subband tuning curve without a redundant comparison. In our design, we use a fuzzy binary search algorithm implemented by the module's digital part to solve this problem. Simulation of VCO's characteristics indicates that a difference of 1 LSB in its trim value shall cause the subband tuning curve to move upward or downward a space not less than 2 MHz, as shown in Figure 4, which means a calibration
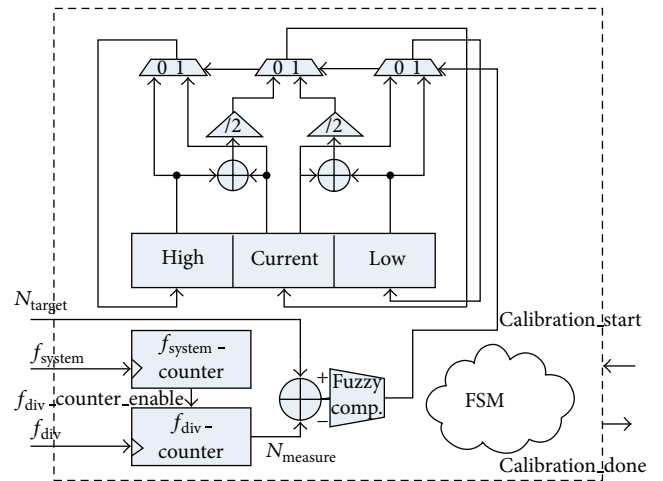

Figure 3: The VCO calibration block diagram.

resolution of 1 MHz is sufficient. The calibration resolution can be represented as

$$f_{res} = \frac{N}{k \cdot T_{clk}}. \tag{1}$$

In the above formula, N is the dividing ratio of VCO's output frequency to the frequency of the divided signal fed to the calibration module. Because in our design the programmable divider can support a minimum dividing ratio of 16, so N has a minimum value of 64. T_{clk} is the period of the system clock (24 MHz). To ensure a calibration resolution of 1 MHz, we can compute that k must at least be 1536 in our case.

The digital part of the frequency synthesizer is responsible for two tasks. One is to control the programmable divider in the analog part when the PLL is in closed loop state; the other is to conduct autocalibration to find VCO's optimal tuning curve before the frequency synthesizer is configured to work at some certain frequency.

VCO calibration circuit is demonstrated in Figure 3. It has two frequency counters, clocked by the reference clock and the divided VCO signal div, respectively. There are other
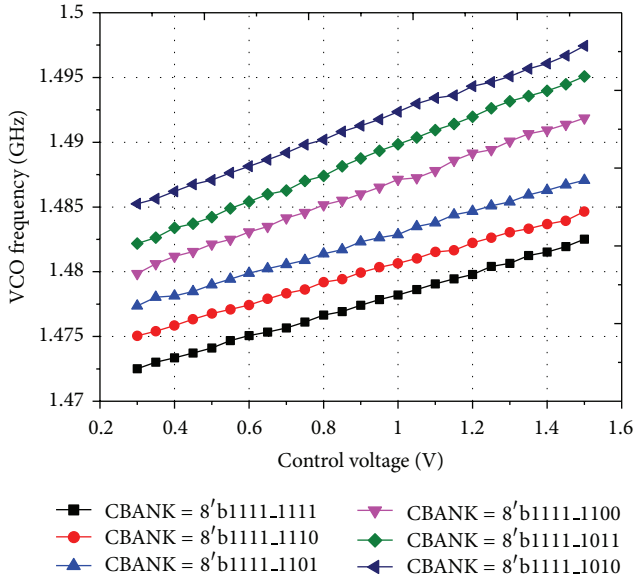
FIGURE 4: VCO's subband tuning curves under CBANK (7:0) from $8'b1111\_1010$ to $8'b1111\_1111$.

three registers high, current, and low, which are used to store the binary search values. The values in two frequency counters are arithmetically subtracted and feed to the fuzzy comparator to determine how to update the values in the three binary search registers. A finite state machine controls the calibration process and asserts the calibration done signal when the search process is finished.

The VCO calibration block updates CBANK according to the following three cases.

(i) If $N_{measure} > N_{target} + 1$, we consider that the VCO oscillates too fast, and we need to increase CBANK in the next search round. Consider the following:

$$\begin{aligned} high &= high, \\ current &= \frac{high + current}{2}, \\ low &= current. \end{aligned} \tag{2}$$

(ii) If $N_{measure} < N_{target} - 1$, we consider that the VCO oscillates too slow, and we need to decrease CBANK in the next search round. Consider the following:

$$\begin{aligned} high &= current, \\ current &= \frac{low + current}{2}, \\ low &= low. \end{aligned} \tag{3}$$

(iii) If $N_{target} - 1 < N_{measure} < N_{target} + 1$, we consider that the optimal CBANK is found, and the search process will be terminated.

This algorithm can guarantee the convergence to the closest subband tuning curve. Another advantage is that it

has a smaller expected comparing times, at the cost of just a small amount of increase in hardware. Figure 5 presents the flowchart of the proposed fuzzy binary search algorithm.

The VCO calibration process happens when (1) the frequency synthesizer is powered on to work at the default operating frequency, and (2) the division parameter is changed by user. At the beginning of the calibration process, the PLL is set to the open loop state, VCO is driven by a fixed voltage of 0.9 V, the trim word CBANK (7:0) is set to the middle value of $8'b01111111$, and the programmable divider's division value is set to $D_{constant} = 16$, so div, the signal fed to the calibration module, has a frequency, that is, 1/64 of the VCO oscillation frequency. Then, the calibration module, clocked by the global system clock of 24 MHz, measures the frequency of div in a period of time Tclk, where $k = 1536$. After that, it compares the measured result $N_{measure}$ with N_{target} based on the user-set frequency, which is calculated by hardware from the formula

$$N_{target} = floor\left\{\left(NI + \frac{NF}{2^{fw}}\right) \cdot \frac{k}{D_{constant}}\right\}, \tag{4}$$

where NI is the integer part of the desired programmable division factor, NF is the fractional part of the desired programmable division factor, and fw is the width of NF. The floor notional is due to hardware implementation limits. N_{target} is used to decide whether to increase or decrease CBANK based on a modified binary search strategy. After at most 7 searches, the optimal CBANK value must be found and registered. Then, the PLL is set to the close loop state and the SDM takes control of the programmable divider; then the calibration process is finished.

The time needed to conduct one VCO autocalibration process can be expressed as follows:

$$T_{calibration} = (T_{settle} + k \cdot T_{clk}) \cdot N_{search}, \tag{5}$$

where T_{settle} is the PLL's stabilization time in the open loop state, which is less than $1\,\mu s$ and very small compared to T_{clk} and hence can be neglected; $k \cdot T_{clk}$ is the time consumed by one in one search process; N_{search} is the search times before the optimal CBANK is found. With 24 MHz system clock, in the worst case N_{search} will be 7 and $T_{calibration}$ is approximately $450\,\mu s$. Though this amount of time is not small, it does not require extra prescalers in calibration circuits.

3. DC Offset Compensation Block

In such a low-power application, device temperature remains relatively constant during its "awake" state and supply voltage is regulated by an on-chip PMU which has very little or slow variations. Therefore, a power-on DC offset calibration and compensation is sufficient to eliminate the problem while maintaining acceptable cost. Another characteristic found by simulating the analog circuit is that DC offset at different gain words can vary greatly, which requires writing the offset compensation word for each gain word into the digital RAM for system's later lookup.

Figure 6 shows the diagram of the DCOC circuits. In this design, IF analog circuits are partitioned into three stages,
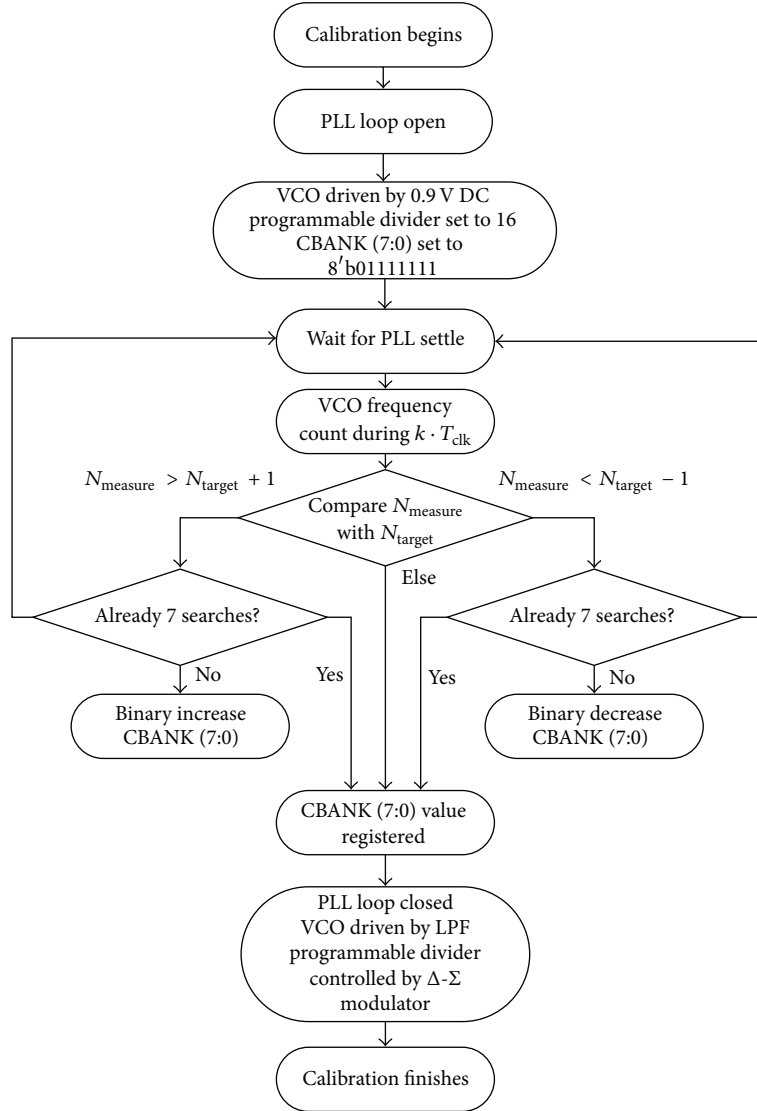
FIGURE 5: Fuzzy binary search algorithm.

with each stage having a 6-bit DAC to adjust the DC voltage. Each DAC has the same output step of 2.5 mV and a dynamic range of 160 mV. The schematic of the comparator is shown in Figure 8. When the comparator's enabled signal COMP_EN is cleared, M1 is shut off, and OUT_P and OUT_N and forced to be high, which means that this circuit consumes power only during the comparison process. In order to minimize the input offset, the size of input transistors M2 and M3 should be made large enough, but large size also causes large parasitic capacitance and degrades the speed performance. Simulation results show that the charging and discharging time of the two head-tail connected inverters need to be not less than $6\,\mu$s to give a trustworthy comparison result, so every comparing duty is set to be $10\,\mu$s to add enough time margin.

Systematic analysis indicates that calibrating offset stage by stage needs less power and hardware than calibrating at only the final stage. Our calibration strategy is as follows: at

the beginning of transceiver power-on, the mixer and PGA1 of I branch are enabled, initial value for the corresponding 6-bit DAC is set, and the differential output of PGA1 is connected to the comparator. The comparator compares the DC value of the positive and negative input signals and gives out a binary comparison result. Based on the comparison result, the digital control block either increases or decreases the control bits of the corresponding DAC. The DAC adds a correction current to PGA in the way as [10] does. After the comparator is settled at the new DAC word, the digital control module checks the comparison result and makes new adjustments. This process is continued until the comparison result reverses, and the current DAC is recorded in RAM. The calibration is applied to PGA1, PGA2, PGA3, I branch, and Q branch separately, and traverses all gain words. The principle of the DCOC calibration process is demonstrated in Figure 7. In the figure, the DC voltage on the N input terminal of the
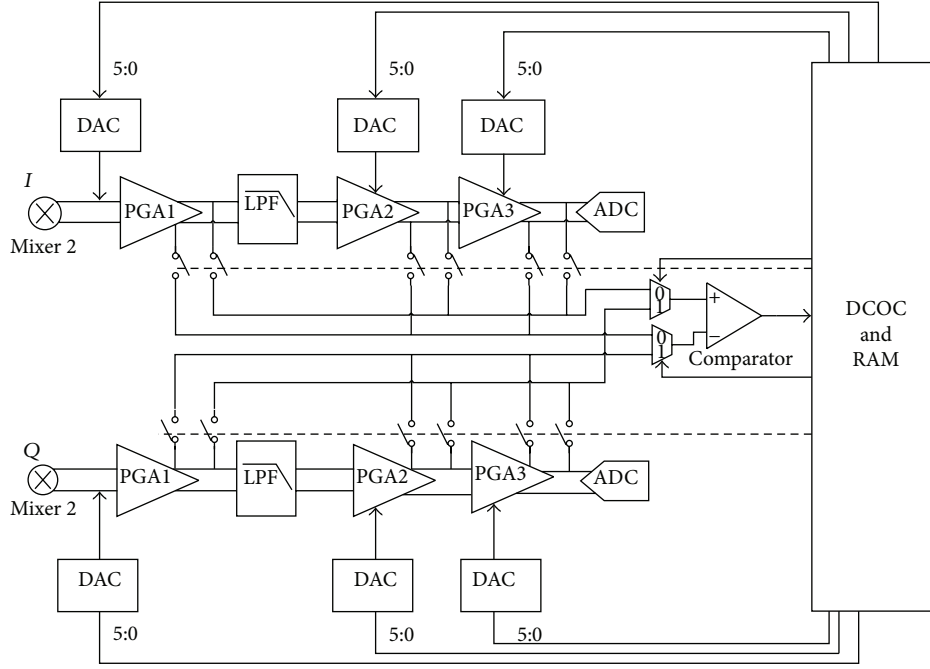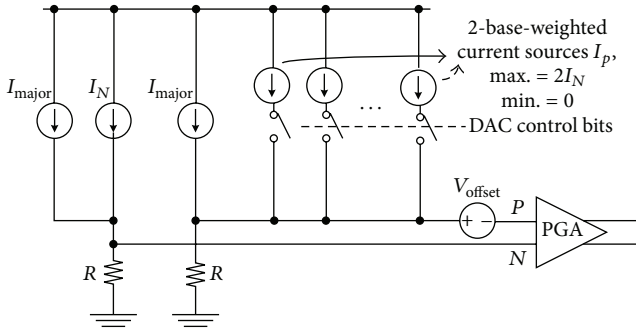
FIGURE 6: The IF and DCOC circuit.

FIGURE 7: Principle of DC offset cancellation of one stage.

FIGURE 8: The comparator circuit.

PGA is generated by a DC current divided into I_{major} and I_N. The DC voltage on the P input terminal is generated by I_{major} and a series of 2-based-weighted current sources that can be tuned from 0 to $2I_N$, so, the maximum V_{offset} that can be compensated is from $-I_N R$ to $+I_N R$.

It is easy to obtain the total calibration time as

$$T_{\text{dcoc}} = T_{\text{one}} \cdot 2 \cdot 3 \cdot N_{\text{gain}}, \tag{6}$$

where T_{one} is the time needed in one calibration process, in the worst case $T_{\text{one}} = 10 \cdot 64 \, \mu s = 640 \, \mu s$. N_{gain} is the number of the different gain words. In our design, the IF gain can be configured from 0 to 60 dB which means $N_{\text{gain}} = 61$; so in the worst case, it takes $10 \cdot 64 \cdot 2 \cdot 3 \cdot 61 = 0.2304 \, s$ to get a complete DCOC LUT. Also, the LUT RAM needs to accommodate $61 \cdot 6 \cdot 6 = 2196$ bits.

The input-equivalent offset of the comparator is below 1 mV, and the DAC gain is 2.5 mV, which leads to a theoretical 3.5 mV overall precision.
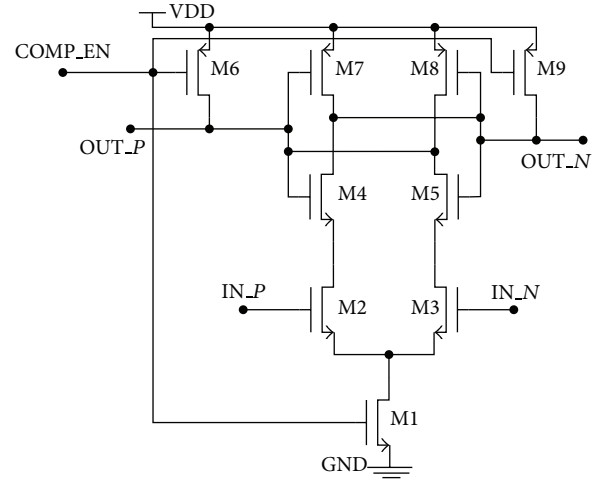
4. Implementation and Test Results

Based on the proposed calibration methods, a multiband transceiver is designed and fabricated with the 0.18 μm CMOS technology with a supply voltage of 1.8 V. As shown in Figure 9, the overall die area is 4750 μm × 4100 μm, among which the layout area of DCOC circuit is 0.38 mm^2 and autocalibrated frequency synthesizer occupies an area of 0.29 mm^2. Power measurement demonstrates that the frequency synthesizer consumes 1.2 mA and the DCOC circuit consumes 2.1 mA current.

To test the functionality of VCO calibration circuit, the target dividing ratio of 19.1 is set. Figure 10 shows the digital wave plot of critical signals during the VCO calibration
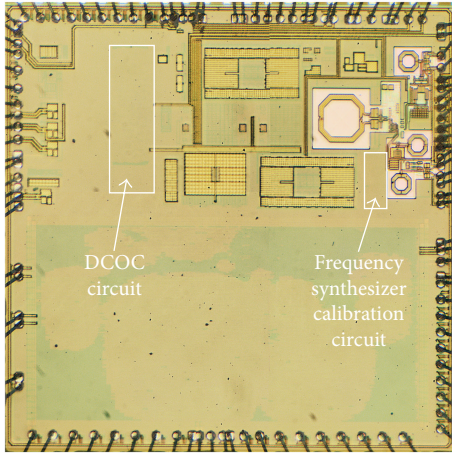
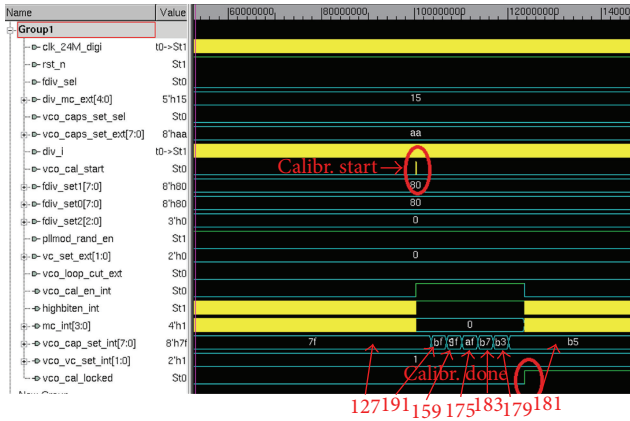FIGURE 9: Micrograph of the transceiver die, with the DCOC circuit.

FIGURE 11: Time domain autocalibration process for the target dividing ratio of 19.1.

FIGURE 10: Digital waveform of the VCO autocalibration process.

FIGURE 12: Time domain DC offset change during calibration.

TABLE 1: Frequency synthesizer performance summary and comparison.

Programmable divider's dividing ratio	VCO output frequency (MHz)	CBANK final value
16.5	1584	8′b10001110
16.9375	1626	8′b01101001
17	1632	8′b01101010
17.5	1680	8′b01001011
18	1728	8′b00110101
18.5	1776	8′b00011000
19	1824	8′b00001010
19.5	1872	8′b00000011

process. As illustrated, the CBANK is initially set to the decimal value of 127, then traverses through 191, 159, 175, 183, 179, and finally locks on 181. The result proves that the fuzzy binary search algorithm and the circuit work as expected. Figure 11 shows the VCO output frequency change. We can see that after 458 μs the calibration is successfully done and the VCO output is 1.842 GHz.

Table 1 presents the calibration outcome when the programmable divider's dividing ratio is set to different values. We can see that the CBANK value decreases when the dividing ratio increases, which is in accordance with a theoretical assumption that VCO oscillates faster when CBANK is smaller.

As for the DC offset cancellation test, a DC offset of 3 mV is intentionally added to the input of PGA1, and the gains of PGA1, PGA2, and PGA3 are set to be 26 dB, 18 dB, and 15 dB, respectively. We can see from Figure 12 that before calibration, the offset after the 1st stage is about 60 mV, the offset after the 2nd stage is about 500 mV, and the offset after the 3rd stage exceeds the supply voltage. After calibration the overall DC offset measured at the output of the 3rd stage is
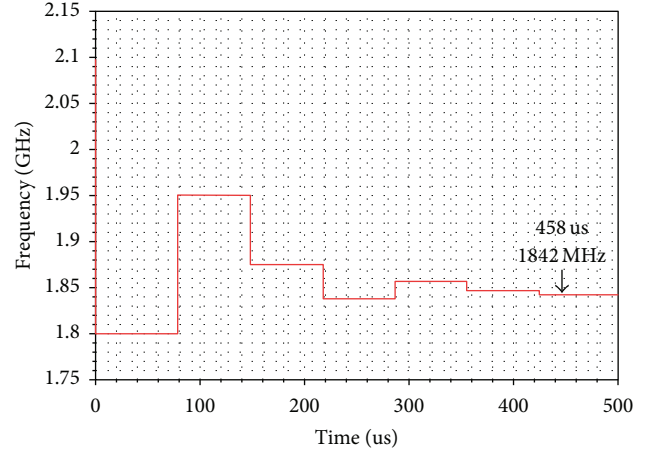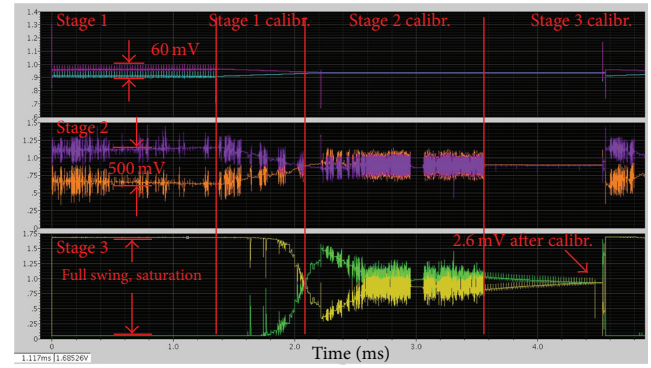
approximately 2.6 mV. Table 2 gives the calibration results for each stage.

Tables 3 and 4 present the frequency synthesizer's performance summary with comparison and the DCOC circuit's performance summary with comparison. Though the proposed calibration circuit takes longer to reach a result, no extra prescaler is needed; thus, this structure saves power and area. The DCOC achieves a prominent increase in accuracy for its gain-based calibration method. The summarized data

TABLE 2: Measured DC offset before and after calibration.

Measure position	Before calibration (mV)	After calibration (mV)
PGA1 Input	3	N.A.
PGA1 output	60	N.A.
PGA2 output	502	N.A.
PGA3 output	>1800	2.6

TABLE 3: Frequency synthesizer performance summary and comparison.

	[11]	This work
Technology	$0.5\,\mu m$ SiGe CMOS	$0.18\,\mu m$ CMOS
VCO frequency range (GHz)	1.15–1.75	1.5–2.1
Current (mA)	19.5	1.2
Calibration resolution (Hz)	5 M	1 M
Phase noise	−129 dBc/Hz at 400 KHz −139 dBc/Hz at 3 MHz	−126.3 dBc/Hz at 400 KHz −137 dBc/Hz at 3 MHz
Calibration time (μs)	150	450

TABLE 4: DCOC circuit performance summary and comparison.

	[12]	This work
Technology	$0.18\,\mu m$ CMOS	$0.18\,\mu m$ CMOS
Bandwidth (MHz)	11/22	2
Gain range (dB)	−6~58	0~60
Gain step (dB)	2	1
Current consumption (mA)	6.12	2.1
DC offset after calibration (mV)	100	3.5
Gain-based calibration	No	Yes

reveals that the proposed calibration techniques are fully suitable for the multiband multimode transceiver.

5. Conclusions

In this paper, we present two digital calibration and compensation techniques to adjust the VCO's tuning curves in the frequency synthesizer and eliminate the DC offset voltage in the intermediate frequency pathway. Based on these proposed methods, a multiband transceiver is designed and fabricated in $0.18\,\mu m$ CMOS with 1.8 V voltage supply. Experimental results show that with 24 MHz system clock, the frequency synthesizer calibration can be completed within $450\,\mu s$ to a resolution of 1 MHz; intermediate frequency pathway can achieve a DC offset voltage of less than 3.5 mV for 0 to 60 dB gain, with each calibration process taking only 1.28 ms time. The active area of the autocalibrated frequency synthesizer occupies an area of $0.29\,mm^2$, and the DC offset cancellation circuits occupy $0.38\,mm^2$. The frequency synthesizer calibration block consumes 1.2 mA current and the DCOC circuit consumes 2.1 mA current. The proposed techniques and corresponding circuits are proved to be costefficient while maintaining high performance, that is, suitable for multiband and multimode transceiver integration.

References

[1] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 555–558, May 1998.

[2] A. Aktas and M. Ismail, "CMOS PLL calibration techniques," *IEEE Circuits and Devices Magazine*, vol. 20, no. 5, pp. 6–11, 2004.

[3] W. B. Wilson, U. K. Moon, K. R. Lakshmikumar, and L. Dai, "CMOS self-calibrating frequency synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1437–1444, 2000.

[4] J. Lee, K. Kim, J. Lee, T. Jang, and S. Cho, "A 480-MHz to 1-GHz sub-picosecond clock generator with a fast and accurate automatic frequency calibration in $0.13\,\mu m$ CMOS," in *Proceedings of the IEEE Asian Solid-State Circuits Conference*, pp. 67–70, November 2007.

[5] M. Kondou, A. Matsuda, H. Yamazaki, and O. Kobayashi, "A 0.3 mm2 90-to-770 MHz fractional-N synthesizer for a digital TV tuner," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC '10)*, pp. 248–249, February 2010.

[6] J. Shin and H. C. Shin, "A 1. 9-3. 8 GHz fractional-N Σ-Δ PLL frequency synthesizer with fast auto-calibration of loop bandwidth and VCO frequency," *IEEE Journal of Solid-State Conference*, vol. 47, pp. 1–8, 2012.

[7] H. Y. Shih, C. N. Kuo, W. H. Chen, T. Y. Yang, and K. C. Juang, "A 250 MHz 14 dB-NF 73 dB-gain 82 dB-DR analog baseband chain with digital-assisted DC-offset calibration for ultra-wideband," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 338–350, 2010.

[8] Y. Wang, B. Afshar, T. Y. Cheng, V. Gaudet, and A. M. Niknejad, "A 2.5 mW inductorless wideband VGA with dual feedback DC-offset correction in 90 nm CMOS technology," in *Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC '08)*, pp. 91–94, June 2008.

[9] Y. Zheng, J. Yan, and Y. P. Xu, "A CMOS VGA with DC offset cancellation for direct-conversion receivers," *IEEE Transactions on Circuits and Systems I*, vol. 56, no. 1, pp. 103–113, 2009.

[10] L. Zhang, H. Jiang, and F. Li, "DC offset calibration method for zero-IF receiver removing the PGA-gain-correla ted offset residue," *AEU-International Journal of Electronics and Communications*, vol. 67, no. 7, pp. 578–584, 2013.

[11] H. I. Lee, J. K. Cho, K. S. Lee et al., "A Σ-Δ fractional-N frequency synthesizer using a wide-band integrated VCO and a fast AFC technique for GSM/GPRS/WCDMA applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1164–1169, 2004.

[12] Z. S. Cheng and J. C. Bor, "A CMOS variable gain amplifier with DC offset calibration loop for wireless communications," in *Proceedings of the International Symposium on VLSI Design, Automation and Test (VLSI-DAT '06)*, pp. 29–32, April 2007.