

## Research Article

# Fabricating Pinhole-Free YSZ Sub-Microthin Films by Magnetron Sputtering for Micro-SOFCs

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Received 2 September 2010; Revised 19 October 2010; Accepted 2 November 2010

Academic Editor: Boniface Kokoh

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Submicron thin yttria stabilized zirconia (YSZ) films were prepared on a variety of substrates with different surface morphologies by magnetron sputtering followed by thermal oxidation. Pinholes were observed in the films deposited on nanoporous alumina substrates. Initial dense Y/Zr films developed nanocracks after thermal oxidation on smooth Si wafer substrates. At optimal sputtering and oxidation conditions, smooth and crack/pore-free films were achieved on Si wafer substrates. The thin YSZ films exhibited fully ionic conduction with ionic conductivities, and activation energy corroborated well with the values from commercial YSZ plates. The thin YSZ films can be utilized in Solid Oxide Fuel Cells (SOFCs) for intermediate temperature operations.

## 1. Introduction

Yttria stabilized zirconia (YSZ), an oxide ion conductor, has been the primary electrolyte in Solid Oxide Fuel Cells (SOFCs) because of its mechanical strength and chemical stability. Practically, the area-specific resistance (ASR) from the YSZ electrolyte needs to be less than  $0.1 \text{ ohm} \cdot \text{cm}^2$  to ensure high-energy efficiency. However, the minimum thickness of YSZ that can be mass produced for SOFCs is in the range of tens of micrometers. The large thickness, low oxide-ion conductivity, and high conduction activation energy (around 1.0 eV) result in large ASR of the YSZ electrolyte at low temperatures. As a consequence, traditional YSZ-based SOFCs require high operating temperatures (above  $800^\circ\text{C}$ ) which limit the choice of sealing materials and create numerous problems such as corrosion and performance degradation. Lowering SOFCs operating temperature is in highly demand, particularly for potential applications in transportation and portable electronics [1–4]. When the reaction kinetics at both cathode and anode are facile, reducing the YSZ thickness is critical. For instance, the decrease of the YSZ thickness from  $10 \mu\text{m}$  to  $400 \text{ nm}$  can reduce the operating temperature from  $800^\circ\text{C}$  to  $450^\circ\text{C}$ .

Recently, there is growing interest to fabricate state-of-the-art electrolyte sub-microthin films for SOFCs capable of operating at intermediate temperatures [5–9].

The major challenges to successfully employ sub-microthin electrolytes are to ensure the films fully dense and pinhole-free. Various morphological substrates and deposition approaches have been investigated to fabricate YSZ thin films. The minimum thickness YSZ films directly deposited on porous Ni-YSZ anode was around 2–5 micrometer, restricted by the microsize pores in the anode substrate [10, 11]. Dense YSZ thin films were constantly achieved by using pulse laser deposition (PLD) and atomic layer deposition (ALD) on dense smooth substrates, like Si or  $\text{Al}_2\text{O}_3$  wafer [8, 12, 13]. However, PLD can hardly produce homogeneous thin films in large area, and ALD is relatively expensive from the practical point of view.

Sputtering is one of the widely used and relatively low cost thin film deposition approaches. By adjusting deposition parameters, for example, gas pressure, deposition power, substrate temperature, and sputtering time, different morphologies including fully dense and highly porous films can be achieved [14]. Park deposited YSZ thin films onto anodized nanoporous alumina substrates followed by oxidation at temperature of  $500^\circ\text{C}$  [15]. However, the measured

conductivity values were two-order magnitude lower than the values from commercial YSZ plate. Additionally, the minimum thickness of YSZ films in the SOFC configuration was 670 nm to achieve open circuit voltage (OCV) of 0.83 V, lower than the theoretical value. The low OCV value indicated the existence of gas leakage through the thin film. Recently, Huang et al. [7] demonstrated a working ultrathin SOFCs, which consisted of the 50 nm thick YSZ films directly deposited by radio frequency (RF) sputtering on Si substrate. Huang et al. also reported increased conductivities in ultrathin gadolinia-doped ceria deposited by magnetron sputtering followed by thermal oxidation [16]. RF-sputtering renders directly deposit oxide films from the corresponding ceramic targets. Magnetron sputtering, however, requires an electronic conducting target which can only deposit metallic films directly. Thermal oxidation process is necessary to obtain oxide films. The disadvantages of RF-sputtering relative to magnetron-sputter include (1) the deposition rate is very low, (2) metal-rich films tend to form, (3) ceramic targets (the brittle and poor thermal conducting) are susceptible to thermal stress crack at high power, and (4) the RF power supplies are expensive. Hence, RF-sputtering, though common in laboratory research, has seen limited industrial application [14].

Presented in this report is a series comparison of morphological results of YSZ thin films deposited via DC magnetron sputtering. Three different substrates, that are, nanoporous alumina, nonporous rough-surfaced alumina plate, and nonporous smooth-surfaced Silicon wafer, were selected. Anodized nanoporous alumina substrate, having vertical channels completely through the membrane, may lead to its functions as both the gas flow channel and the structural supporter for micro SOFCs [15]. Nonporous substrates like alumina or silicon wafer can serve as microfuel cell supporter after back etching [7–9]. The influences of the substrates and processing conditions on the quality of YSZ thin films were discussed. Ionic conductivities of the thin films deposited on nonporous alumina substrate were analyzed based on electrochemical impedance spectroscopy.

## 2. Experimental Aspects

**2.1. Thin Film Preparation and Morphology Imaging.** The YSZ thin films were deposited by using the DC magnetron sputtering approach. A 16:84 Y-Zr alloy plate which had a purity of 99.9% was used as a DC sputtering target (Kurt J. Lesker). The target was 5.08 cm (2 inch) in diameter and 0.32 cm (0.125 inch) in thickness. The distance between the target and the substrate was 10 cm. The substrate materials selected for film deposition were anodized nanoporous alumina (Whatman), nonporous polycrystalline alumina plate (Kyocera), and nonporous Silicon wafer (Si). On the Si wafer, a 500 nm thick silicon nitride layer was grown by chemical vapor deposition prior to YSZ thin film deposition. This silicon nitride layer served two functions: (i) a buffer layer to prevent Si diffusion into YSZ thin films during heat treatment and (ii) a blocking layer for wet-etching Si during fabrication of micro-SOFCs by MEMS technology [7–9].

The DC sputtering was performed at room temperature, and sputtering power was set at 200 watts. Argon pressure and deposition time were varied to control the porosities and thicknesses of the films. To achieve the “dense Y/Zr film” noted in this paper, 0.5 Pa argon pressure was used, and the deposition rate was estimated at 5 nm/s. To achieve the “porous Y/Zr films”, argon pressure was adjusted to 2 Pa and the deposition rate decreased to 2 nm/s. The Y/Zr films were then oxidized in a box furnace at the setting temperatures for 5 hours in air to form oxide film (referred to as YSZ films in this paper). Traditional micrometer thick YSZ plates were usually manufactured at high temperatures in the range of 1000–1400°C. It is necessary, however, to keep the processing temperatures of YSZ thin films low in consideration of the chemical compatibility with the substrate and control of stresses induced by thermal expansion. In this research, two oxidation temperatures, that are 800°C and 1200°C, were selected to compare the ionic conduction performances of the YSZ thin films. The surface and cross-section morphologies of the thin films before and after thermal oxidation were imaged using scanning electron microscope (FEI and JEOL).

**2.2. Electrochemical Characterization.** To perform conductivity characterizations, a 200 nm thick platinum layer was patterned on top of the Y/Zr and/or the YSZ films on dense alumina substrate. The dense Pt electrode patterns were deposited via DC-sputtering at 1 Pa, 100 W, and room temperature with the aid of a shadow mask. The Pt electrode pads are 0.5 cm long and 0.4 cm wide, and the spacing between two electrode pads was 0.2 cm. For impedance measurements, the deposited films with Pt electrode patterns were connected through Pt wires to an electrochemical analysis system (Gamry) and placed in a temperature controlled tube furnace (Carbolite). Electrochemical impedance spectra (EIS) were recorded in air at 50°C intervals with the selected temperature range after thermal equilibrium was achieved (2–3 hours). The AC amplitude was 50 mV, and the frequency was swept between 1 Hz and 0.5 MHz. The EIS results were analyzed using Z-plot software based on complex nonlinear least squares fitting [17].

## 3. Results and Discussion

**3.1. Influences of Substrates on Morphologies of the As-Deposited Y/Zr Thin Films.** Figure 1 showed a series of SEM images comparing the three bare substrates and the top and cross-sectional view of the as-sputtered Y/Zr thin films on these substrates. All the films were deposited at the same parameters, that are room temperature, 200 W, 0.5 Pa, and 80 s. The atomic ratio of Y/Zr in the as-deposited and later thermally oxidized thin films were confirmed to be 0.19 on average based on EDX analyses equipped in SEM microscope, which was consistent with the target composition (16/84). The oxygen over metal (sum of Y and Zr) ratio is in the range of 1.90 to 1.95, which is close to the theoretical value in 8 mol% Yttria stabilized zirconia; the compositional formulae of which is  $Y_{0.16}Zr_{0.84}O_{1.92}$ .

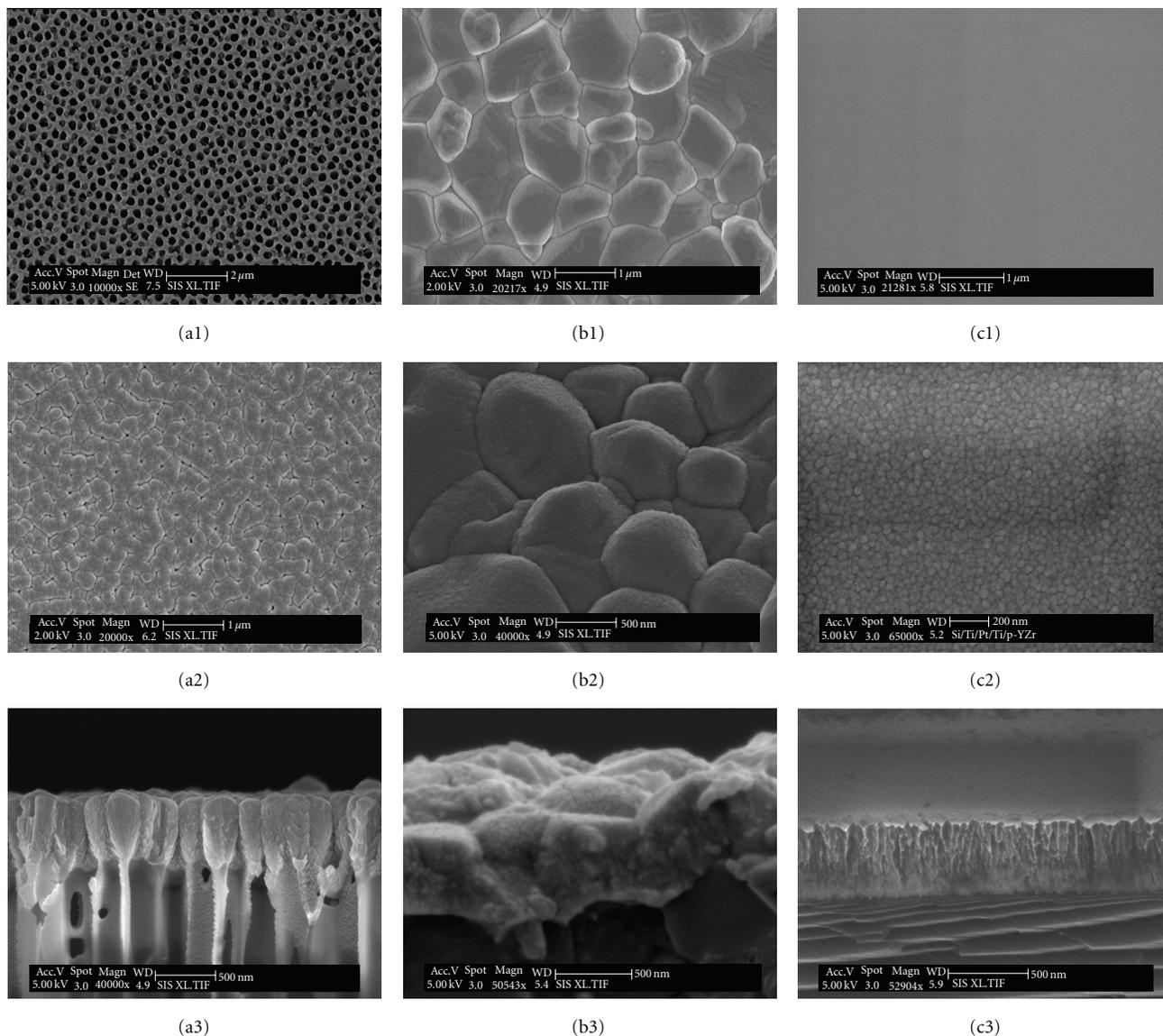


FIGURE 1: SEM images of the top-view substrates (a1) nanoporous anodized alumina, (b1) nonporous alumina plate, (c1) smooth single crystal Si wafer with 500 nm thick silicon nitride layer, top-view (a2, b2, c2) and cross-view (a3, b3, c3) of the as-deposit Y/Zr films. The deposition conditions are 200 W, 0.5 Pa, and 80 s at room temperature.

As can be seen from Figure 1(a1), the porous anodized alumina substrate had an average pore diameter of 200 nm with the wall thickness in the range of 20 nm to 50 nm. Figure 1(a2) was the top-view image of Y/Zr films deposited on the porous substrate. The image revealed apparent pinholes throughout the imaging area. Figure 1(a3) showed the cross-section image of the Y/Zr film, which has an average thickness of 370 nm under the deposition condition. In the process of sputtering, the initial Y/Zr particles were only deposited on the narrow walls of the substrate's pores. These particles became seeds for the following Y/Zr particles such that thin films developed and grew on channels in three dimensions. As a result, the pores gradually shrank into the tulip-shaped films that were observed in Figure 1(a3). However, the pores yet entirely disappeared in the 370 nm

thick film. Later a microfuel cell consisting of 100 nm thick Pt, 370 nm YSZ, and 100 nm thick Platinum, was fabricated on the anodized alumina substrate via DC sputtering followed by oxidation at 800°C for 5 hours. The fuel cell was then subjected to performance evaluation by using hydrogen as a fuel and air as the oxidant. Only 0.2 V was obtained at the open circuit condition. The low open circuit voltage (OCV) resulted from the existing pinholes in the YSZ electrolyte thin film leading to significant gas cross-over. The morphological observations and OCV results suggested that 370 nm thin YSZ electrolyte films grown on the porous alumina substrates were unacceptably for micro-SOFCs.

Following investigations, therefore, were focused on YSZ thin films deposited on nonporous substrates, that are polycrystalline alumina plate and Si wafer. The nonporous

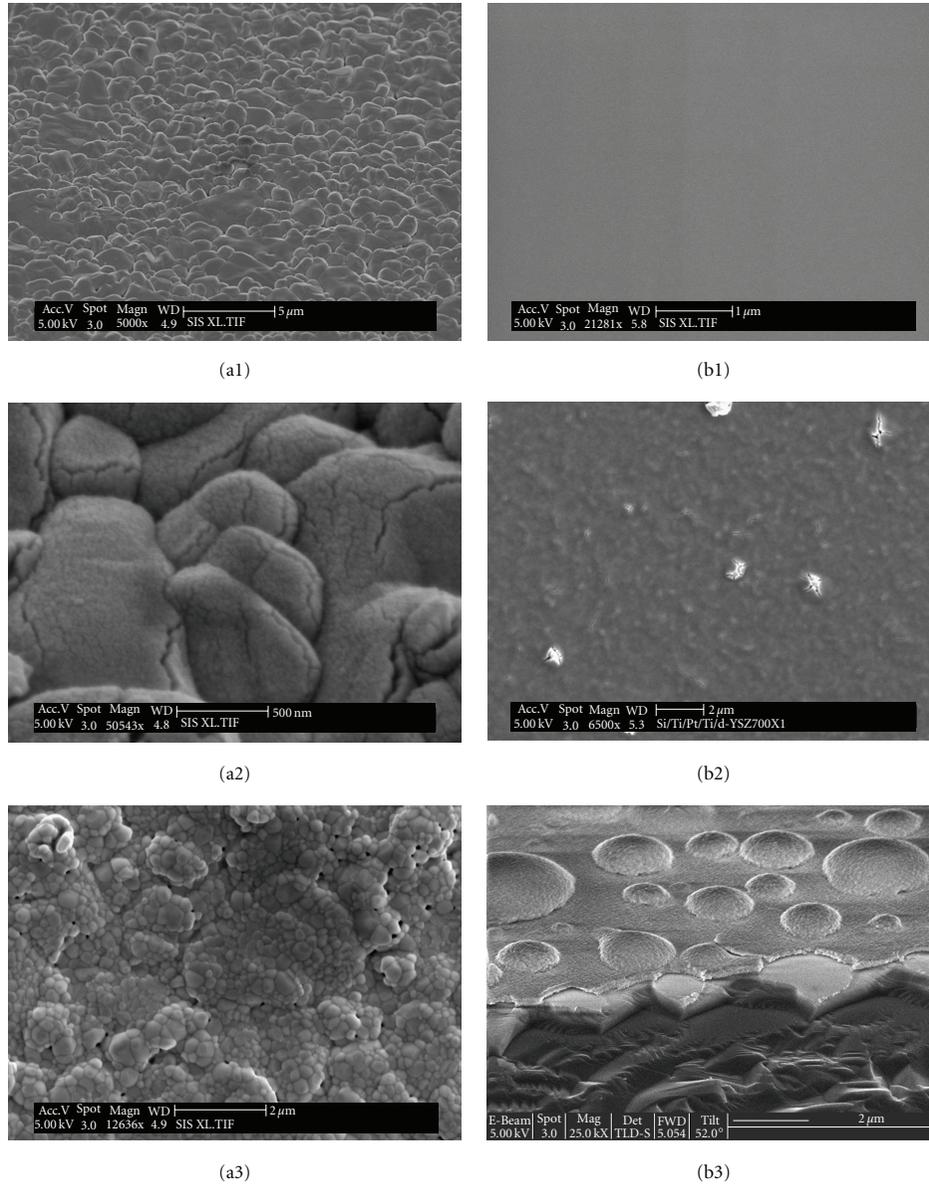


FIGURE 2: SEM images of different thin films deposited on dense polycrystalline alumina plate (a series) and on silicon wafer (b series). (a1, b1) as-sputtered, (a2, b2) annealed at 800°C, and (a3, b3) annealed at 1200°C.

alumina plate was made up of alumina grains in the size range of 500 nm to 1  $\mu\text{m}$ , as can be seen in Figure 1(b1). The as-deposited Y/Zr film fully covered the alumina surface with the same morphological pattern as the substrate (Figure 1(b2)). No pinholes were visible but the film was grainy and uneven. The average grain size of Y/Zr was approximately 20 nm. The thickness of the Y/Zr film was in the range of 370–380 nm (Figure 1(b3)). On the Si wafer, the deposited Y/Zr film was much more smooth and homogenous (Figures 1(c1)–1(c3)) in comparison to the films on polycrystalline alumina substrate. No pinholes were visible from top view and cross-section view. The thickness of the film was 380 nm. Clearly, the deposition rate was close to 5 nm/s at the experimental setting conditions, independent of the substrate morphologies.

**3.2. Influence of Oxidation Temperatures on Film Morphology.** Oxidation temperatures had profound impacts on the film morphologies of YSZ films. SEM images of the thin films before and after thermally annealing at 800°C and 1200°C were compared in Figure 2. The films were deposited on the nonporous alumina substrate and on silicon wafer. At oxidation temperature of 800°C, nanocracks were generated in the film (Figure 2(a2)) from the dense and pinhole/crack-free as-sputtered films (Figure 2(a1)). After being oxidized at 1200°C for 5 hrs, the grain size increased around ten times, that is, from 10–30 nm to 100–300 nm. Simultaneously, nanopinholes with average diameter of 100 nm were generated in films on alumina substrate, especially in the vicinity of grain boundary regions (Figure 2(a3)). Similar phenomena were observed in the films made on Si wafer

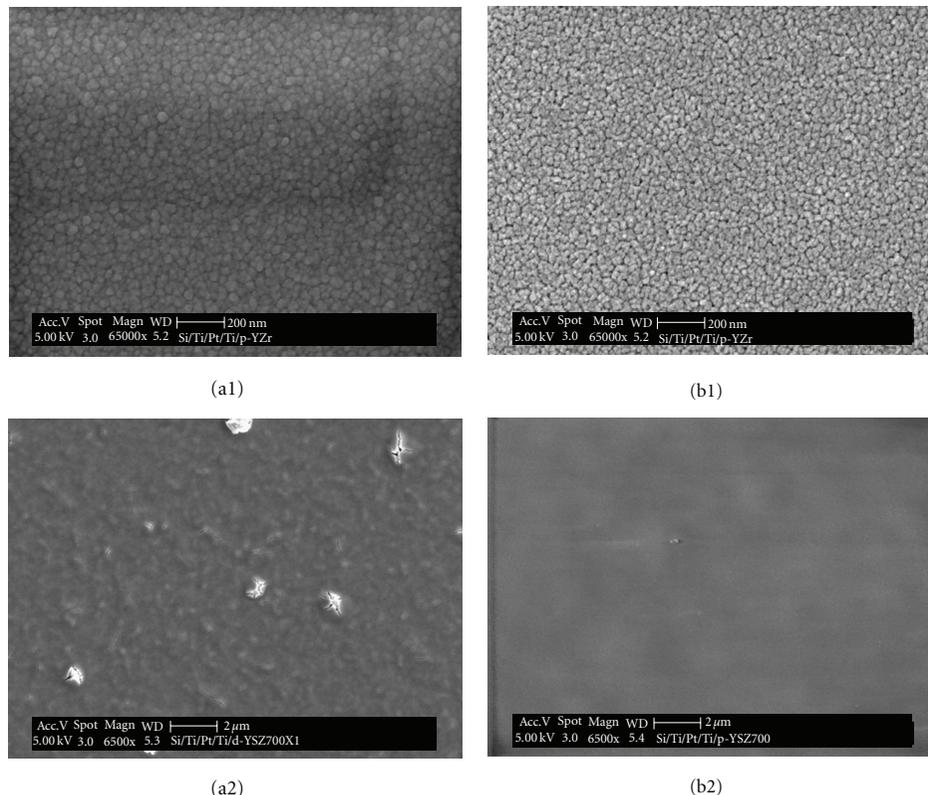


FIGURE 3: SEM images of (a1) dense Y/Zr film deposited at 0.5 Pa; (b1) less dense Y/Zr thin films deposited at 2 Pa; (a2) YSZ thin films oxidized from (a); (b2) YSZ thin films oxidized from (b). The substrate is Si wafer. Oxidation condition is 800°C for 5 hrs.

films. Compared to those on polycrystalline alumina plate, cracking and pore generation on Si wafer were more severe because the films were denser prior to oxidation (see Figures 2(b2) and 2(b3)). Many spherical bubbles were generated and detached from Si surface after 1200°C oxidation. The observed dramatic morphological changes were attributed to the expansion of closed packed crystal structure of the pure metals to the fluorite crystal structure of zirconium oxide as a consequence of oxidation.

These observations led to experiments on developing “as deposited” Y/Zr thin films with less density in Si wafer substrate to accommodate volume expansion after oxidation. A series of experiments were conducted to tailor the density of the Y/Zr films via adjusting sputtering pressure. It was found that increasing sputtering pressures increased the porosity of the “as sputtered” films. Figure 3 showed SEM images of the as-deposited Y/Zr films as well as the oxidized YSZ thin films. Apparently, Y/Zr thin film deposited at 2 Pa was more porous (Figure 3(b1)) than that deposited at 0.5 Pa. After oxidation at 800°C for 5 hrs, pinhole free as well as crack-free YSZ thin films were achieved on smooth Si wafer (Figure 3(b2)).

**3.3. Ionic Conductivities of Oxidized YSZ Thin Films.** The conductivities were derived from electrochemical impedance spectra obtained in the planar configuration, as sketched in Figure 4(a). According to electrochemical impedance theory [17], the highest frequency (hf) impedance arcs in

Nyquist plot (imaginary-part impedance  $Z''$  versus real-part impedance  $Z'$  obtained from frequency sweep) are associated with conduction processes in thin films between the two platinum electrodes. In YSZ polycrystalline specimens, oxide ions can conduct in bulk grains and grain boundaries. Correspondingly, there will be two arcs in the frequency range of a few to hundreds of kHz in Nyquist plot. A circuit, as shown in Figure 4(b), is equivalent to the two conducting processes, which will not be discussed extensively here. Small differences in characteristic frequencies for bulk and grain boundary conduction may result in overlap of the two arcs. Figure 4(c) exhibited a typical Nyquist plot recorded at 350°C on the 380 nm thick YSZ thin film samples deposited on the nonporous polycrystalline alumina substrate and oxidized at 800°C for 5 hrs. The electrochemical impedance spectra were fitted using Z-view software based on nonlinear least square method and the equivalent circuit. Both bulk conductivity ( $R_c$ ) and grain boundary conductivity ( $R_{gb}$ ) were retrieved from the fitted results. Conductivity at each temperature point was then calculated from the total electrolyte resistance ( $R_e = R_b + R_{gb}$ ). It is noteworthy that upon increasing temperature, the grain and grain boundary arcs overlap more significantly and hence rather difficult to separate. At temperature above 500°C, we used the overall resistance directly without separation of grain and grain boundary part.

The Y/Zr film deposited on the nonporous alumina plate was subjected to in situ conductivity analyses in air upon

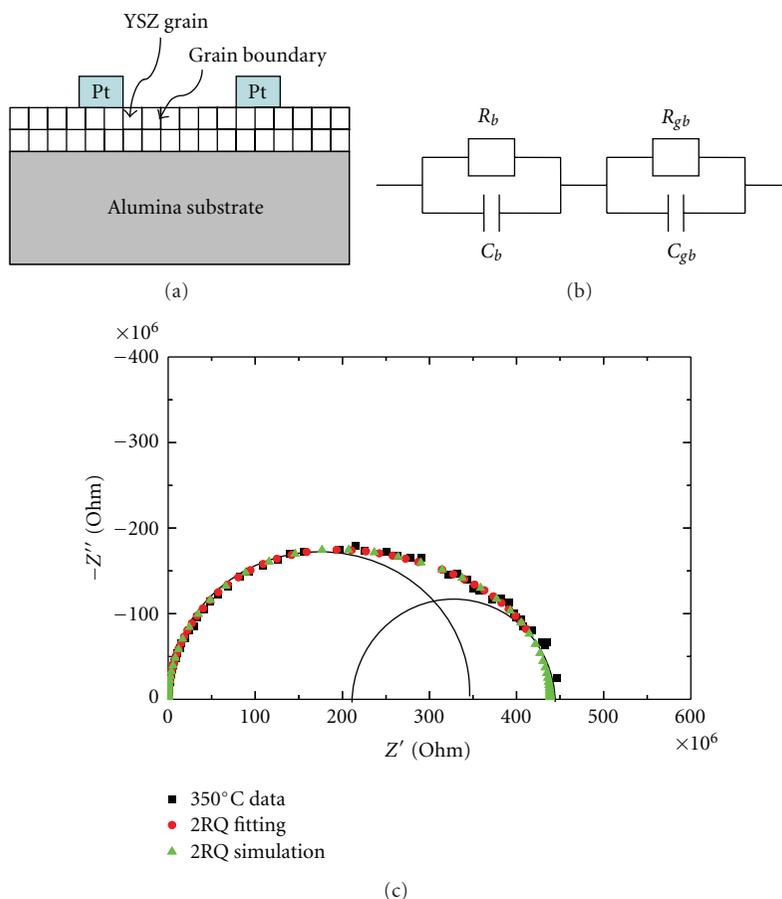


FIGURE 4: (a) Schematics of the specimen for conductivity measurement. (b) Equivalent circuit corresponding bulk and grain boundary conduction in polycrystalline ionic conductors. Q: constant phase element. (c) Typical Nyquist plot recorded at 350°C on 380 nm thick YSZ thin film specimen after being oxidized at 800°C for 5 hrs.

increasing temperature. The logarithmic conductivities as a function of thermal oxidation temperatures are shown in Figure 5(a). To reach thermal equilibrium, electrochemical impedance spectra were recorded after 2 hours at each setting temperature. The EIS data were in situ collected in the temperature range between 50°C and 700°C. The results showed that below 250°C, the conductivities were in the range of  $10^3$ – $10^4$  S/cm and then slightly decreased upon increasing temperature. The activation energy value was calculated, based on Nernst equation, less than 0.01 eV. This low activation energy and high conductivities suggested dominant electronic conduction in Y/Zr films. Essentially, no oxidation of the Y/Zr films occurred at temperatures below 250°C. As the oxidizing temperature was increased to 260°C, conductivity values decreased significantly. At oxidizing temperature of 270°C, the conductivity dropped off even more dramatically to  $10^{-5}$  S/cm. This observation suggested that oxidation of Y/Zr to YSZ began at the temperatures around 260–270°C. However, 270°C was insufficient to completely oxidize the interior sections of the Y/Zr films because of the slow oxygen diffusion. In the range from 270°C to 300°C, decrease of conductivities continued. Electronic percolation paths were disconnected due to the increase of the oxide

phase, leading to dramatic conductivity decrease. Increasing temperatures beyond 350°C resulted in a gradual increase in conductivities. Activation energy of the conductivity in the temperature range of 400–700°C was 1.06 eV. Ex situ XRD analyses confirmed fluoride structure of the thin films after oxidation at 400°C.

To ensure fully oxidized and elimination of electronic contribution, the Ex situ conductivity analyses were performed on YSZ thin films after oxidization at 800°C and 1200°C for 5 hrs, as shown in Figure 5(b). The conductivities as well as activation energies of the YSZ thin films were compared with the reference 8% YSZ electrolyte plate purchased from the Japanese Fine Ceramics, as well as previously reported values associated with ionic conductivity of 8% YSZ [7–9, 18–21]. The ionic conductivities of YSZ thin film oxidized at 1200°C were close to the reference data, while the values from YSZ thin film oxidized at 800°C were relatively lower. The slight difference in conductivities was probably associated with the Y and Zr distribution variation in the oxide films. High annealing temperatures like 1200°C allow sufficient Y diffusion across the thin film leading to a better compositional homogeneity.

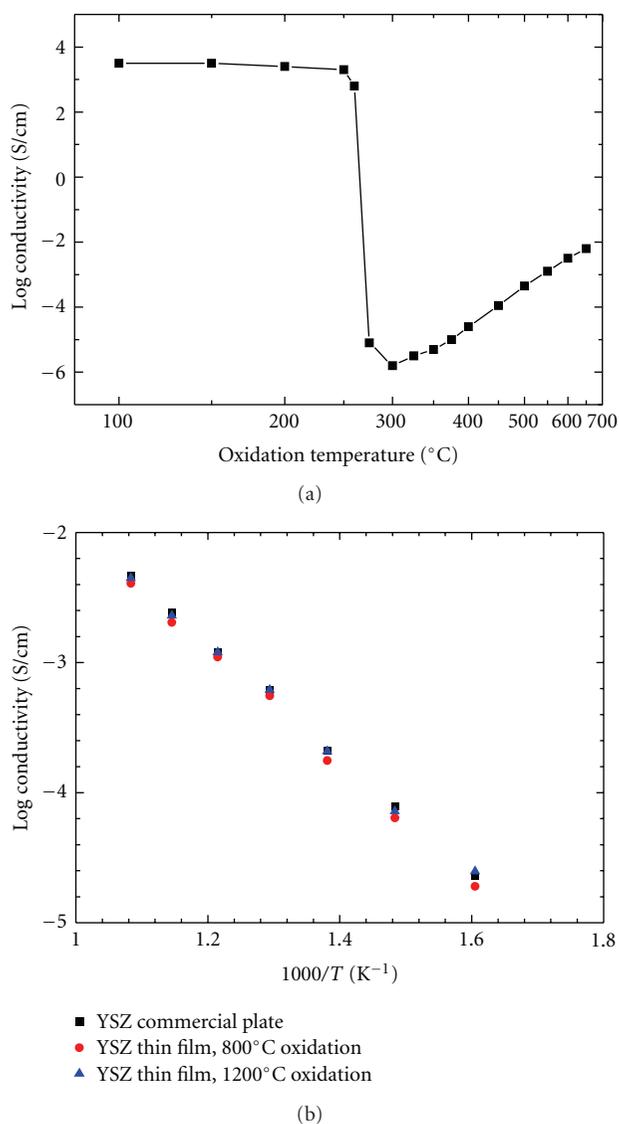


FIGURE 5: (a). In situ conductivities in logarithmic scale changes with thermal oxidation temperature. (b) Logarithmic conductivities versus reciprocal temperatures from YSZ thin films achieved at different oxidation temperatures, that are 800°C and 1200°C, in comparison with 8YSZ commercial plate.

#### 4. Summary

YSZ thin films were prepared on three substrates with different morphologies via DC-sputtering followed by thermal oxidation. Porous anodized alumina substrates result in sub-microthick films with nanopinhole, rendering unacceptable gas leakage for micro-SOFCs. Thermal oxidation will cause significant volume expansion. In consideration of this impact, pinhole/crack-free YSZ thin films can be achieved by appropriately controlling the porosity of the initial as-deposited Y/Zr films. The thin films exhibited fully ionic conduction after oxidation at high temperatures, for example, 800°C and 1200°C, with ionic conductivities and activation energy values well corroborated with commercial

YSZ plates. The sub-microthin YSZ films deposited on Si wafer (with silicon nitride passivation layer) by DC magnetron-sputtering can potentially be utilized in thin-film and micro-SOFCs for intermediate temperature operations.

#### Acknowledgment

The author would like to thank Professor F. B. Prinz at the Department of Mechanical Engineering, Stanford University. Part of this research was conducted at his laboratory.

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