Hindawi Publishing Corporation
International Journal of Microwave Science and Technology
Volume 2013, Article ID 275289, 5 pages
http://dx.doi.org/10.1155/2013/275289

Research Article

Systematic Design Methodology of a Wideband Multibit Continuous-Time Delta-Sigma Modulator

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Received 14 November 2012; Accepted 5 February 2013

Academic Editor: Ahmed Allam

Systematic design of a low power, wideband and multi-bit continuous-time delta-sigma modulator (CTDSM) is presented. The design methodology is illustrated with a 640 MS/s, 20 MHz signal bandwidth 4th order 2-bit CTDMS implemented in 0.18 μm CMOS technology. The implemented design achieves a peak SNDR of 65.7 dB and a high dynamic range of 70 dB while consuming only 19.7 mW from 1.8 V supply. The design achieves a FoM of 0.31 pJ/conv. Direct path compensation is employed for one clock excess loop delay compensation. In the feedforward topology, capacitive summation using the last opamp eliminates extra summation opamp.

1. Introduction

Delta-sigma modulators embed low-resolution analog-to-digital converter in a feedback loop. The use of feedback and high oversampling pushes the quantization noise out of the band of interest and thereby provides a high in-band resolution. Delta-sigma modulator is well suitable for a high-resolution data conversion because a moderate accuracy of passive components is required. Recently, continuous-time delta-sigma modulator has brought tremendous attention because of its exceptional features such as inherent antialiasing filter (AAF), relaxed gain-bandwidth requirement on active elements resulting in a low-power consumption compared to its counterpart discrete-time delta-sigma modulator [1, 2]. Low-power consumption is the key for a CTDSM.

In [3], the design methodology for a multibit modulator with two-step quantizer is presented. However, the optimization of the peak SNR and the maximum stable amplitude is not taken into consideration. Also, excess loop delay compensation is for more than one clock, where, to achieve higher resolution, higher bit quantizer should be used. These all increase the design methodology complexity and are not simple to adopt for designers. To keep the design simple and the insight intact, we implement one-step quantizer with excess loop delay compensation for one clock. In [4], the optimal design methodology of a higher-order continuous-time wideband delta-sigma modulator is presented. However, this methodology requires summation amplifier and hence consumes higher power. In our approach, the summation amplifier is eliminated by using capacitive summation with last integrator's amplifier and this makes design simpler and saves significant power. Also, in [4] SNR and phase margin are optimized which could be replaced to simpler way to optimize the peak SNR and the maximum stable amplitude which are more obvious parameters.

Recent development in wireless communication standard demands a wideband and high-resolution data converters. To achieve a high SNR over a wideband, a higher clock rate, that is, a higher oversampling ratio (OSR), is desired. However, OSR is limited by the clock rate due to technology limitations and power consumption. Fortunately, the SNR

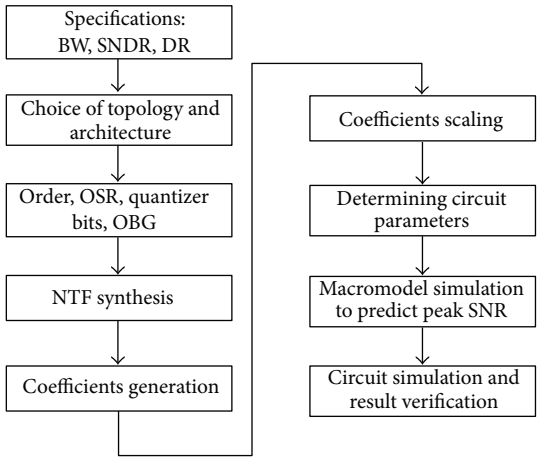

Figure 1: Flow chart of the design methodology.

degradation due to lower OSR can be compensated by a multi-bit quantizer.

We present a systematic methodology to design a wideband and high-resolution modulator at low power cost. To illustrate the methodology, we aim to design a continuous-time delta-sigma modulator which has signal bandwidth of 20 MHz and requires 10-11-bit resolution suitable for WLAN. Section 2 discusses the high-level synthesis. In Section 3, we present simple circuit implementation of the modulator. Section 4 presents the results and discussion and finally Section 5 concludes the paper.

2. High-Level Synthesis

In this section, we describe the design methodology in accordance with the flow chart in Figure 1 to synthesize a high-level wideband multi-bit continuous-time delta-sigma modulator in MATLAB to meet the specification for WLAN.

2.1. Choice of Topology and Architecture. A single-loop topology is preferred to a MASH topology to reduce the circuit complexity. To implement the loop filter, a feedforward (FF) topology is preferred to a feedback (FB). A FF topology has several advantages over a FB topology. Firstly, FF uses only one feedback DAC (without any compensation for excess loop delay (ELD)) in the main loop which results in smaller silicon area and better matching of coefficients. However, in the case of FB, multiple DACs equal to the order of the modulator are needed which increase the chip area and mismatch is a major concern [5]. Secondly, the integrating resistor in both the FF and the FB topologies is determined by the noise and distortion requirement. However, in a FF topology, the second and further resistors can be made larger. In a FF topology the first opamp is the fastest while in a FB topology, the first opamp is the slowest. Thus the capacitor size can be reduced in the second and higher integrators with increased resistor value which significantly reduces the silicon area [6]. Also, the necessity for scaling and also the requirements on integrator dynamics are much more relaxed which results in increase in power efficiency of FF topology compared to that of FB topology [1]. However, in general FF topology requires extra summation amplifier which could be eliminated by implementing capacitive as shown in Figure 4 and explained in Section 2.3 [7]. Thus a single-loop FF DSM is the most suitable choice for a high dynamic range and a low-power design.

2.2. Noise Transfer Function (NTF) Synthesis. Noise transfer function synthesis is critical for delta-sigma modulator design as it guides the overall performance and the stability of modulator. Before NTF can be synthesized, order of the modulator, oversampling ratio, quantizer's bit and out-of-band gain must be determined.

2.2.1. Oversampling Ratio (OSR). Among all these, oversampling is the most important driving factor as it is directed by the technology node and power consumption. In principle, increasing OSR by 2 times results in a 15 dB improvement in SNR. However, OSR or clock rate is limited by CMOS technology and the power consumption. To design a wideband modulator with 20 MHz signal bandwidth, an OSR of 16 results in a clock rate (f_s) of 640 MS/s which is high enough to design analog circuits in 0.18 um CMOS technology. Thus we need to design a comparator which can perform comparison at 640 MS/s and opamp which can have GBW higher than 640 MHz for integration to support sampling at 640 MS/s. Since these are pretty high-performance components, we limit the oversampling ratio to 16.

2.2.2. Modulator's Order. Higher-order modulator improves the SNR; however, it increases the circuit complexity and deteriorates the stability. Since we target a wide-signal band of 20 MHz, a higher-order modulator is essential and therefore we simulate the modulator for third, fourth, and fifth order. From simulation we find that a good choice of the modulator order is 4 for a wide bandwidth (20 MHz) and ideally produces a SNDR of 70 dB which is approximately 8 dB higher than the required 62 dB for 10-bit resolution. This 8 dB margin is kept to counter the loss due to circuit nonidealities. This is why 4th-order modulator is chosen for implementation.

2.2.3. Quantizer's Bit. A multi-bit quantizer has several advantages over a single-bit quantizer [1, 2] and compensates well the SNR limitation due to lower OSR. Firstly, a multibit quantizer reduces in-band quantization noise by 6 dB and allows more aggressive NTF with higher out-of-band gain (OBG) resulting in further significant drop in in-band quantization noise. Secondly, the amplitude of the noise in a multi-bit quantizer is much lower compared to that in a single-bit quantizer. Hence the slew rate requirement on the loop filter opamp is greatly relaxed to allow low-power opamp design. Thirdly, a multi-bit feedback DAC is less sensitive to clock jitter [8]. For low power, reduced circuit complexity, and to keep peak SNR well above 60 dB, a 2-bit quantizer is chosen.

2.2.4. Out-of-Band Gain (OBG). As a rule of thumb, the OBG for a single bit quantizer is 1.5 to ensure the stability

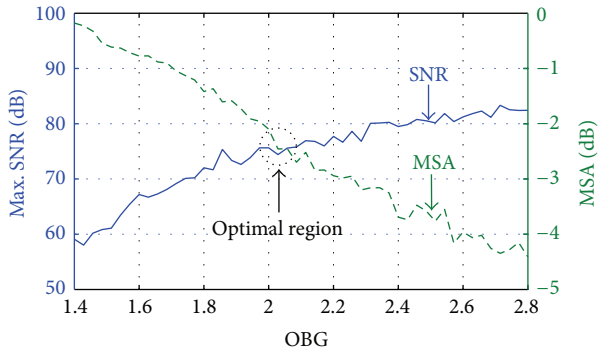

Figure 2: SNR and MSA versus the out-of-band gain (OBG) of the NTF for 4th-order 2-bit DSM.

[9]. However, in case of a multi-bit quantizer, the OBG can be increased to reduce the in-band noise and thereby improve the SNR. A 4th-order, 2-bit modulator is extensively simulated for various OBG to determine the maximum SNR and the maximum stable amplitude (MSA). Considering the tradeoff between the SNDR and the maximum stable amplitude (MSA), as depicted in Figure 2, the optimum OBG is chosen to be 2.

Now with all parameters in hand, the NTF is determined using the function *synthesizeNTF* from [10]. A 4th-order, 2-bit modulator with OSR of 16 results in a peak SNDR of 70 dB over a signal bandwidth of 20 MHz.

2.2.5. Excess Loop Delay (ELD) Compensation. The finite regenerative time of a flash converter and the digital logic delay time in the feedback add extra delay, called excess loop delay (ELD), in the loop and effectively increase the order of the modulator. For a modulator of order 2 or above, it needs to be compensated to ensure the stability and maintain a high SNR. One of the efficient methods to compensate ELD is coefficient tuning by adding a direct path between the DAC output and the flash input [1]. Though the compensation time could be any, from the circuit design and operation point of view, it is better to compensate for half a clock or integral multiple of half a clock. To use a single clock, one clock delay compensation is used which helps to relax the requirement on analog building blocks, opamp and comparator.

2.3. Coefficients Generation and RC Parameters. The function *synthesizeNTF* returns discrete-time (DT) coefficients of a modulator which must be translated into continuous-time (CT) coefficients. To reduce the clock jitter sensitivity, NRZ DAC pulse is preferred to other DAC pulse shapes. With NRZ DAC and one clock compensation for excess loop delay, the discrete-time coefficients are converted into the continuous time using the function *realizeNTF_ct* available in [10]. The obtained coefficients result in integrator's output which have much higher swing for modern low supply voltage like 1.8 V and direct implementation would result in large clipping and hence large distortion. Also, the output of one integrator is input to the next integrator and therefore large swing will demand high-input swing for opamp which costs high power.

Table 1: Scaled coefficients.

a_0	1.34
a_1	4.25
a_2	4.92
a_3	3.39
a_4	2.76
b_1	0.4
c_1	0.4
c_2	0.4
c_3	0.4
c_4	0.1
g_1	0.11
g_2	0.29

Therefore, the scaling is done to ensure that the output swings of all integrators are well below the maximum allowed voltage (in our case 1.8 V) such that they accommodate the saturation voltage of the output stages of opamps and they do not distort the signals. The resulting coefficients are tabulated in Table 1 for the modulator block diagram in Figure 3.

Figure 4 shows the block diagram of the loop filter. For simplicity, the diagram is shown single-ended; however, the actual circuit implementation is done fully differential. The fourth integrator is used to integrate with R_4C_4 and opamp and the same opamp is used to sum all the feedforward voltages with a_0C_4, a_1C_4, a_2C_4, and a_3C_4 along with C_4 [7]. The coefficients a_1, a_2, and a_3 are realized with the capacitive sum while the coefficient a_4 is embedded in the integration with R_4C_4. This helps to completely eliminate the summation opamp and thereby saves a significant amount of power. Delta-sigma

$$R_1 = \frac{V_{\text{in}}^2/2}{32kTf_B * 3*2^{2B-1}} \tag{1}$$

modulator is a thermal-noise-limited system and the resistor at the input of an active RC integrator contributes the majority of noise. So in a thermal-noise-limited modulator, the resistance value is calculated using (1) [1]. Here R_1 is the resistance at the input of the first integrator, V_{in} is the input signal voltage, k is Boltzmann constant, T is the temperature, f_B is the frequency bandwidth, and B is the effective number of bits. The determined coefficients are translated into "R" and "C" values with the thermal noise constraint as per (1) and keeping the capacitor values such that the feedforward capacitors values are not too large as it loads the last integrating opamp. The determined first resistance value is only 10.93 kΩ and the capacitance is 1.78 pF. The stability and performance of a continuous-time delta-sigma modulator are strongly dependent on process variation as it changes the coefficients drastically. To mitigate the effect, coefficient tuning is desirable. Since resistors are connected either between input and input to the first opamp or between output of one opamp and input of next opamp, it is imperative that tuning using capacitance will be much easier

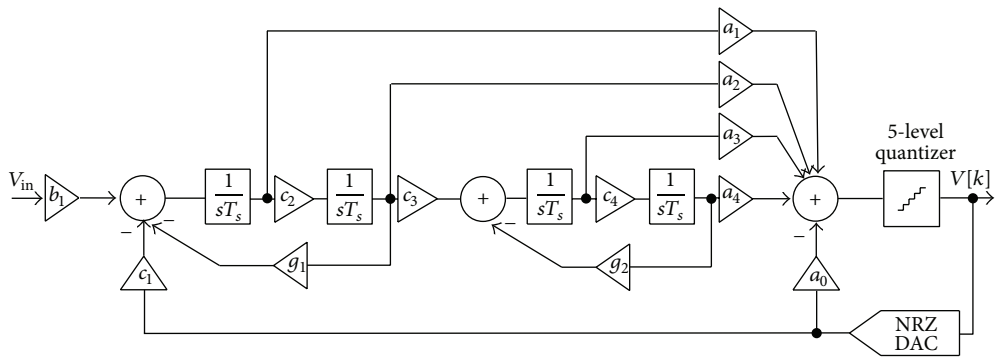

Figure 3: The block diagram of a 4th-order FF modulator with direct path for excess loop delay compensation.

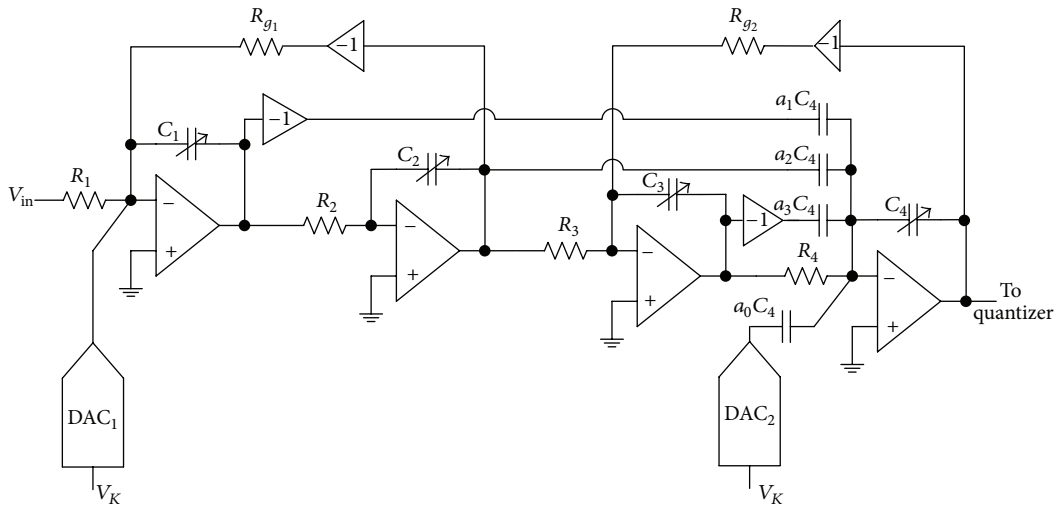

Figure 4: The block diagram of a 4th-order CIFF with direct path for excess loop delay compensation.

and effective to implement. Therefore, to combat process variation, capacitive tuning (C_1 to C_4) is implemented.

To predict the SNR, the behavioral simulation of the modulator is done with macro model of building blocks using the components from *analogLib* and *ahdlLib* of cadence. To include all the noises, thermal and circuit, transient noise is enabled while simulating the design. A 16384-point Hann window PSD predicts a SNDR of 69.7 dB for a tone at 1.0547 MHz.

3. Circuit Implementation

In this section, we describe the transistor level circuit designs of the building blocks used in the modulator.

3.1. Opamp. A generic two-stage miller-compensated opamp is used for a high-speed and a wide output swing. To mitigate input-referred flicker noise, long length input transistors are used. To keep the design simple and, power consumption low only one common mode feedback (CMFB) loop is used to maintain the output at V_{cm}. The opamp draws a total current of 2.2 mA, including the CMFB and biasing, from a supply of 1.8 V. The designed opamp has GBW of $1.56 f_s$.

3.2. Comparator. A preamp stage with a gain of 10 is used as input stage. A regenerative circuit follows the preamp stage and finally SR-latch is used to output the decision. Separate references for differential input are used to avoid the coupling between the two differential inputs. The comparator settles its output within 120 ps.

3.3. Feedback DAC. Feedback DAC is designed in two parts. First part is a d-flip-flop [11] which is used to retime the output of the quantizer. In the second part, a current steering DAC is used for fast response. This DFF and the quantizer effectively introduce a delay of one clock between the input of the flash converter and the output of the feedback DAC. The cascade current source in the DAC cell is used to achieve a high-output resistance. The output impedance of the current DAC is 70 kΩ.

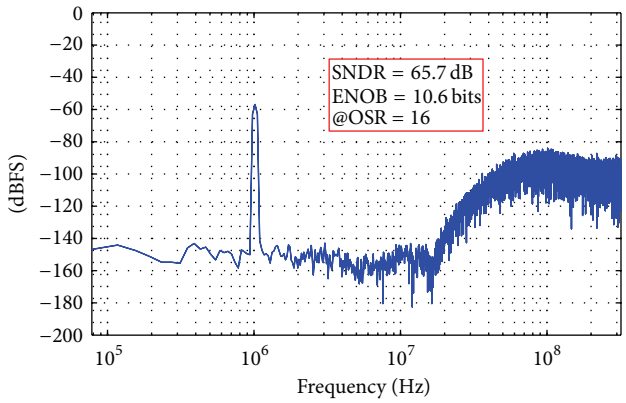

FIGURE 5: Output Spectrum of the modulator.

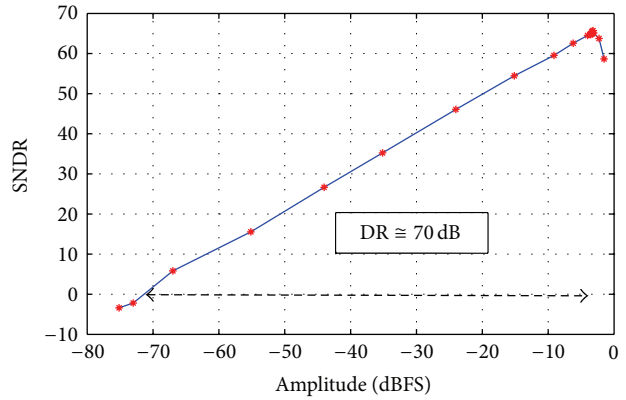

FIGURE 6: Amplitude versus SNDR of the modulator.

4. Results and Discussion

To illustrate the design methodology, a 4th-order 2-bit continuous-time delta-sigma modulator is designed in 0.18 μm CMOS technology. The implemented modulator is tested with a single tone at 1.0547 MHz. A 16384-point Hann window PSD is produced to ensure the sufficient accuracy. The resulted spectrum is shown in Figure 5. From Figure 5, it is determined that the peak SNDR is 65.7 dB over a bandwidth of 20 MHz. Figure 6 has the plot of SNR versus amplitude which gives a high dynamic range of 70 dB. The design consumes overall power of 19.7 mW to achieve a figure of merit (FoM) of 0.31 pJ/conv.

5. Conclusion

A systematic design methodology of a continuous-time delta-sigma modulator is described. A 640 MS/s, 20 MHz signal bandwidth 4th-order 2-bit continuous-time delta-sigma modulator is implemented in 0.18 μm CMOS technology to illustrate the design methodology. The CT coefficients are systematically computed compensating for excess loop delay. The designed modulator has a high SNDR of 65.7 dB and a high dynamic range of 70 dB for a signal band of 20 MHz. This modulator is well suited for WLAN applications. The modulator consumes 19.7 mW power from a 1.8 V supply to achieve FoM of 0.31 pJ/conv.

Acknowledgments

This work was partly supported by a grant of the Regional Innovation Cluster Program (Global Type 2nd Stage) from the Ministry of Education, Culture, Sports, Science and Technology (MEXT) and a Grant-in-Aid for Scientific Research (B) from JSPS, KAKENHI (Grant no. 23360159). This work was also partly supported by a grant of the Knowledge Cluster Initiative implemented by Ministry of Education, Culture, Sports, Science and Technology (MEXT), KAKENHI (B), and KIBAN (B) and the VLSI Design and Education Center (VDEC), The University of Tokyo in collaboration with CADENCE Corporation and Agilent Corporation.

References

[1] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion, Fundamentals, Performance Limits and Robust Implementations*, Springer, Berlin, Germany, 2006.

[2] J. A. Cherry and W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High Speed A/D Conversion Theory, Practice and Fundamental Performance Limits*, Kluwer Academic, New York, NY, USA, 2002.

[3] S. Balagopal, R. M. R. Koppula, and V. Saxena, "Systematic design of multi-bit continuous-time delta-sigma modulators using two-step quantizer," in *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS '11)*, pp. 1–4, August 2011.

[4] Y. Ke, S. Radiom, H. R. Rezaee, G. Vandenbosch, J. Craninckx, and G. Gielen, "Optimal design methodology for high-order continuous-time wideband Delta-Sigma converters," in *Proceedings of the 14th IEEE International Conference on Electronics, Circuits and Systems (ICECS '07)*, pp. 743–746, Marrakech, Morocco, December 2007.

[5] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press, Piscataway, NJ, USA, 2005.

[6] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time ΔΣ ADC for audio applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 351–360, 2008.

[7] S. Pavan, "Excess loop delay compensation in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II*, vol. 55, no. 11, pp. 1119–1123, 2008.

[8] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II*, vol. 46, no. 6, pp. 661–676, 1999.

[9] W. Lee, *A novel higher-order interpolative modulator topology for high resolution oversampling A/D converters [M.S. thesis]*, Massachusetts Institute of Technology, Cambridge, Mass, USA, 1987.

[10] R. Schreier, "The Delta-Sigma Toolbox Version 7. 1," http://www.mathworks.com/matlabcentral/fileexchange/19.

[11] M. J. Park, *A 4th order continuous-time ΔΣ ADC with VCO-based integrator and quantizer [Ph.D. thesis]*, Massachusetts Institute of Technology, Cambridge, Mass, USA, 2009.