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Research Article

CMOS Ultra-Wideband Low Noise Amplifier Design

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This paper presents the design of ultra-wideband low noise amplifier (UWB LNA). The proposed UWB LNA whose bandwidth extends from 2.5 GHz to 16 GHz is designed using a symmetric 3D RF integrated inductor. This UWB LNA has a gain of 11 ± 1.0 dB and a NF less than 3.3 dB. Good input and output impedance matching and good isolation are achieved over the operating frequency band. The proposed UWB LNA is driven from a 1.8 V supply. The UWB LNA is designed and simulated in standard TSMC 0.18 μm CMOS technology process.

1. Introduction

CMOS technology is one of the most prevailing technologies used for the implementation of radio frequency integrated circuits (RFICs) due to its reduced cost and its compatibility with silicon-based system on chip [1]. The use of ultra-wideband (UWB) frequency range (3.1–10.6 GHz) for commercial applications was approved in February 2002 by the Federal Communications Commission. Low cost, reduced power consumption, and transmission of data at high rates are the advantages of UWB technology. UWB technology has many applications such as wireless sensor and personal area networks, ground penetrating radars, and medical applications [2].

Low noise amplifier is considered the backbone of the UWB front-end RF receiver. It is responsible for signal reception and amplification over the UWB frequency range. LNA has many desired design specifications such as low and flat noise figure, high and flat power gain, good input and output wide impedance matching, high reverse isolation, and reduced DC power consumption [1, 3].

Nowadays one of the most suitable configurations suggested for LNA implementation is current reuse cascaded amplifier. This LNA configuration can attain low DC power consumption, high flattened gain, minimized NF, and excellent reverse isolation while achieving wide input and output impedance matching [1–3].

Radio frequency integrated inductors play a significant role in radio frequency integrated circuits (RFICs) implementation. Design, development, and performance improvement of RF integrated inductors represent a challenging work. Achieving high integration level and cost minimization of RFICs are obstructed because of the difficulties facing the RF integrated inductors designers which are related to obtaining high quality factors [4–6].

In this paper, the implementation of LNAs using 3D integrated inductors will be investigated. A symmetric 3D structure is proposed as a new structure of integrated inductors for RFICs.

This paper discusses the design procedure of current reuse cascaded UWB LNA and its bandwidth expansion. In addition, the employment of suggested symmetric 3D RF integrated inductor will be demonstrated. This paper is organized as follows. Section 2 introduces the suggested UWB LNA circuit. Section 3 gives simulation results and discussion. Conclusion is driven in Section 4.

2. Circuit Description

As shown in Figure 1, the proposed UWB LNA is a current reuse cascaded core based on a common source topology with a shunt resistive feedback technique implemented over the input stage.

This current reuse cascaded amplifier achieved good wideband input impedance matching through the use of source degeneration input matching technique. Figure 2 shows the small signal equivalent circuit of this LNA input stage. The input port of this UWB LNA is desired to match source impedance R_s at resonance frequency ω_o. This matching circuit bandwidth is defined through the quality factors of source degeneration and gain-peaking inductors (L_s and L_g) where the input impedance is given by

$$\begin{aligned} Z_{\text{in}} &= j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{\text{gs}}} + \omega_T L_s \\ &= j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{\text{gs}}} + R_s, \end{aligned} \tag{1}$$

where Z_{in} is the UWB LNA input impedance and ω_T is the current-gain cut-off frequency, where $\omega_T = g_m/C_{\text{gs}}$ and g_m and C_{gs} are the input stage transconductance and gate-source capacitance, respectively. V_s represents the RF signal source. R_s is the output impedance of V_s.

Although the shunt resistive feedback loop leads to LNA noise performance degradation [7], it is widely used in recently proposed LNAs due to its superior wideband characteristics. Shunt capacitive-resistive feedback technique is employed to widen the input-matching bandwidth and increase the LNA stability.

Shunt-peaked amplifiers are known to have wide gain bandwidth and high low frequency power gain [8]. To have a high flattened gain of the proposed UWB LNA, shunt-peaking technique is used. In addition the gate-peaking technique is used to enhance the LNA gain at high frequencies. Besides the shunt- and gate-peaking techniques, the shunt resistive feedback loop is used in gain flattening [2, 8]. The LNA approximate gain is given by

$$\begin{aligned} A &\cong \frac{V_{\text{out}}}{V_s} \\ &\cong \frac{g_{m1} g_{m2}\left[R_L // \left(R_{d2} + SL_{d2}\right)\right]\left[SL_{d1}\right]}{2 \cdot SC_{\text{gs1}}\left[S\left(L_{s1} + L_{g1}\right) + 1/SC_{\text{gs1}}\right]}. \end{aligned} \tag{2}$$

Ultra-wideband applications require good noise performance in addition to high and flat gain. Low noise design techniques which are suitable for narrowband applications cannot be used for wideband applications. Main contribution of cascaded matched stages noise figure is due to first stage [9]. The reduction of noise figure of input stage will lead to the reduction of the overall noise figure of the proposed design. Optimization and control of factors affecting the NF will improve this UWB LNA noise performance. An equivalent circuit of the input stage for noise factor calculation is shown in Figure 3 [1].

An estimated value of the noise figure (NF = 10 $\log_{10}$ f) of this topology is given in [1] where f is the noise factor of the UWB LNA. The noise factor f can be given by

$$\begin{aligned} f = 1 &+ \frac{R_g + R_{\text{lg}} + R_{\text{ss}} + R_{\text{ls}}}{R_s} + \frac{\delta\alpha\omega^2 C_{\text{gs1}}^2 R_s}{5g_{m1}} \\ &+ \frac{R_{\text{FB}}\left(\left(L_{g1} + L_{s1}\right)C_{\text{gs1}}\right)^2}{R_s\left(g_{m1}R_{\text{FB}} - 1\right)^2} \\ &\cdot \left| s^2 + s\left(\frac{\omega_{o,\text{rfbn}}}{Q_{\text{rfbn}}}\right) + \omega_{o,\text{rfbn}}^2 \right|^2 \\ &+ \frac{\gamma g_{m1}\left(R_{\text{FB}} + R_s\right)^2\left(\left(L_{g1} + L_{s1}\right)C_{\text{gs1}}\right)^2}{\alpha R_s\left(g_{m1}R_{\text{FB}} - 1\right)^2} \\ &\cdot \left| s^2 + s\left(\frac{\omega_{o,\text{dn}}}{Q_{\text{dn}}}\right) + \omega_{o,\text{dn}}^2 \right|^2, \end{aligned} \tag{3}$$

$$f = 1 + \frac{R_g + R_{\text{lg}} + R_{\text{ss}} + R_{\text{ls}}}{R_s} + f_{\text{gn}} + f_{\text{rfbn}} + f_{\text{dn}}, \tag{4}$$

where

$$\begin{aligned} \omega_{o,\text{rfbn}} &= \sqrt{\frac{1 + g_{m1}R_s}{\left(L_{g1} + L_{s1}\right)C_{\text{gs1}}}}, \\ Q_{\text{rfbn}} &= \frac{1}{R_s + \omega_{T1}L_{s1}} \cdot \sqrt{\frac{\left(1 + g_{m1}R_s\right)\left(L_{g1} + L_{s1}\right)}{C_{\text{gs1}}}}, \\ \omega_{o,\text{rfbn}} &= \sqrt{\frac{1}{\left(L_{g1} + L_{s1}\right)C_{\text{gs1}}}}, \\ Q_{\text{dn}} &= \frac{1}{\left(R_s \mid\mid R_{\text{FB}}\right) + \omega_{T1}L_{s1}} \cdot \sqrt{\frac{\left(L_{g1} + L_{s1}\right)}{C_{\text{gs1}}}}, \end{aligned} \tag{5}$$

where f_{gn}, f_{dn}, and f_{rfbn} are gate, drain, and feedback resistor noise factors, respectively and α, δ, and γ are constants equal to 0.85, 4.1, and 2.21, respectively.

It is clear from (4) that, to reduce the noise figure, high quality factors of L_{s1} and L_{g1} are desired. It can also be noted that the noise factor is inversely proportional to feedback resistor R_f. In other words, weak feedback topology decreases the noise factor value while strong feedback implementation degrades the noise performance of the suggested UWB LNA.

In addition, the noise factor formula given by (4) states that the noise figure is also inversely proportional to the transconductance of the input stage (g_{m1}). This goes along with the known fact that noise performance trades off with power consumption.

For output matching, the series resonance of the shunt peaking technique is used to match the proposed UWB LNA to the load impedance R_L while the series drain resistance R_{d2} is used to extend the output matching bandwidth.

This proposed UWB LNA (LNA1) has an operating bandwidth of 3.1–10.6 GHz. The proposed LNA2 whose schematic

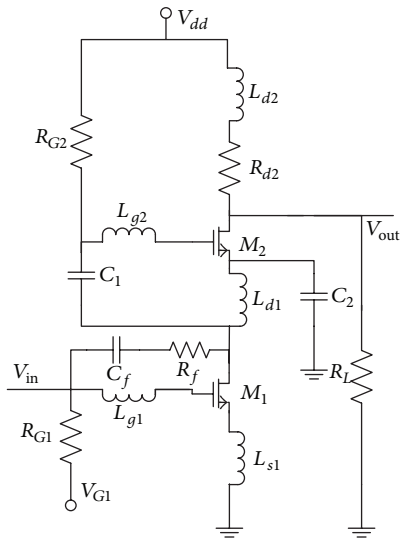

Figure 1: Current reuse UWB LNA (LNA1).

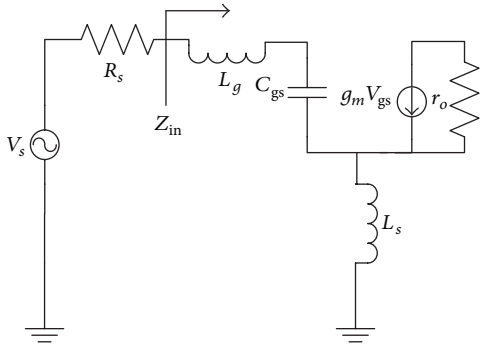

Figure 2: Input stage small signal equivalent circuit.

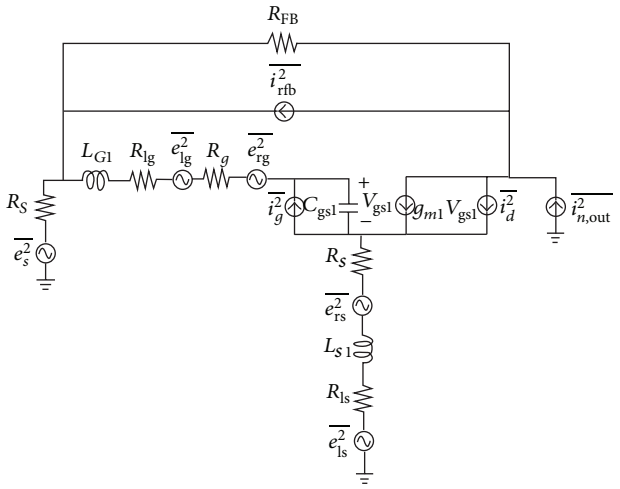

Figure 3: Equivalent circuit of the fisrt stage for noise calculation [1].

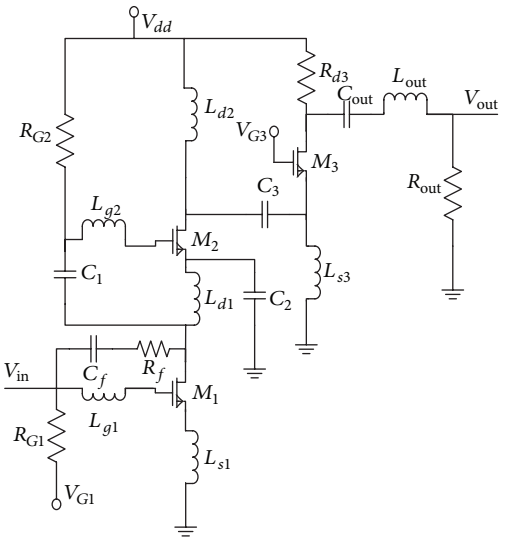

Figure 4: Schematic circuit of LNA2.

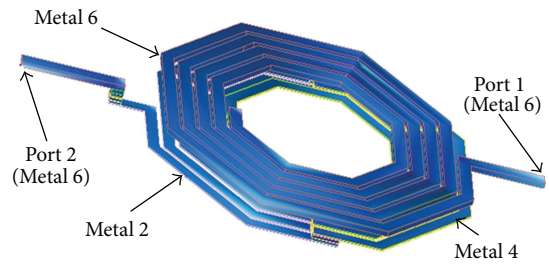

Figure 5: 3D view of the symmetric 3D proposed structure.

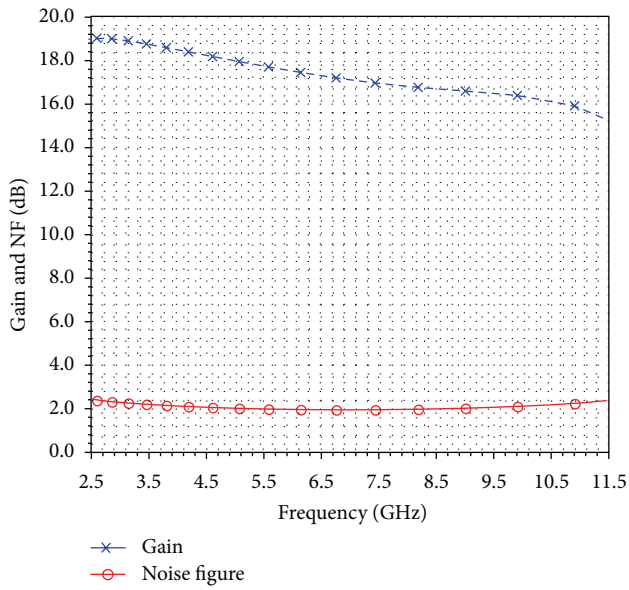

Figure 6: S_{21} (dB) and NF (dB) of LNA1.

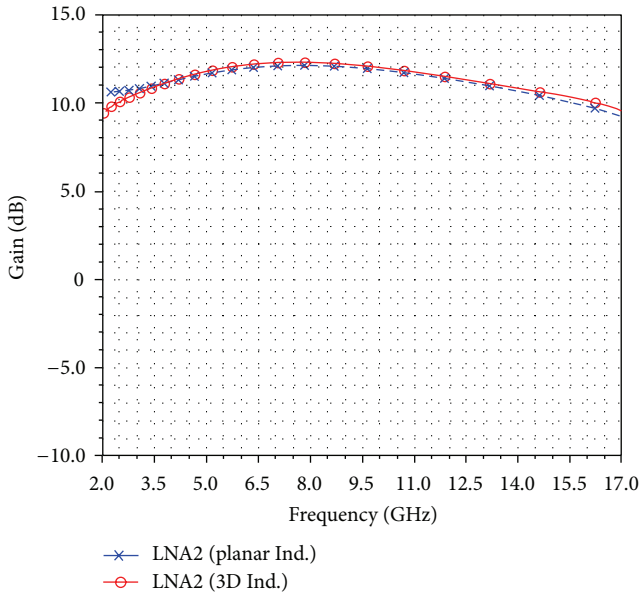

Figure 7: S_{21} (dB) of LNA2.

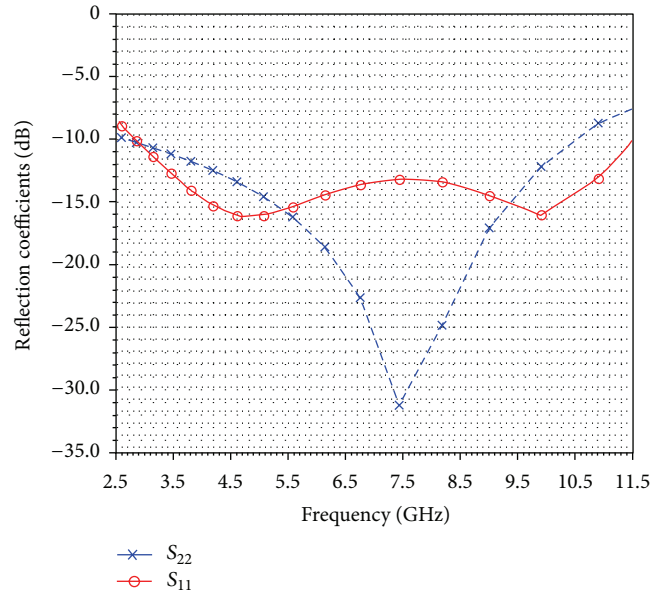

Figure 9: S_{11} (dB) and S_{22} (dB) of LNA1.

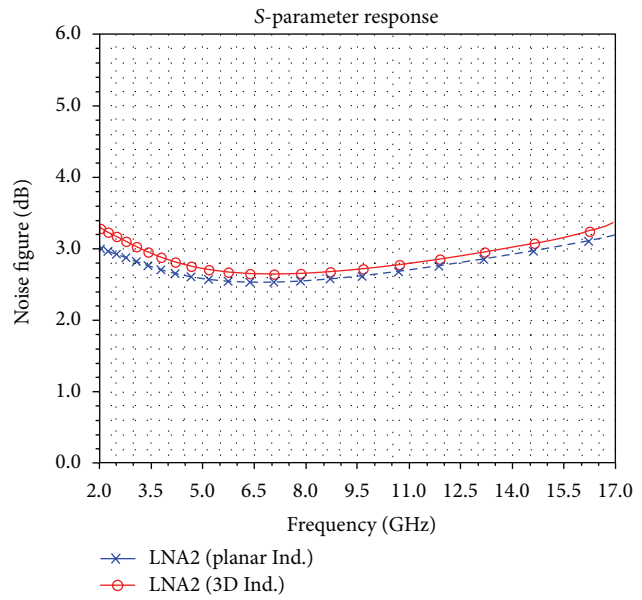

Figure 8: NF (dB) of LNA2.

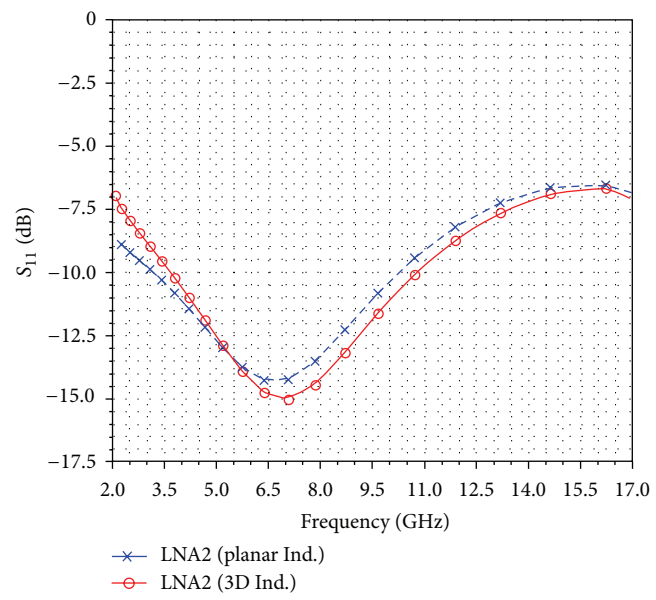

Figure 10: S_{11} (dB) of LNA2.

circuit is shown in Figure 4 is an extended version of LNA1. It has a wider operating band of frequency which extends from 2.5 GHz to 16 GHz.

Input impedance match has a special importance and consideration especially in wideband sensitive circuits design. Input impedance matching bandwidth is broadened by the use of a weaker shunt capacitive-resistive feedback loop which mainly leads to quality factor reduction of the input matching circuit. Weakness of shunt feedback strength not only reduces the input reflection coefficient over this wide bandwidth but it also reduces the input side injected thermal noise which decreases the proposed LNA2 noise figure indicating the enhanced noise performance of the suggested design.

Shunt-peaking technique increases the low frequency gain and hence decreases the gain flatness while having a wide operating bandwidth. In spite of shunt-peaking drawbacks, it mainly facilitates LNA output impedance to load matching. LNA2 bandwidth extension and gain flatness over its operating band of frequency are achieved through the removal of shunt peaking. Moreover the control of gate peaking is used to enhance the current reuse amplifier core gain.

For wideband output impedance matching, a unity common gate (CG) matching topology in addition to series

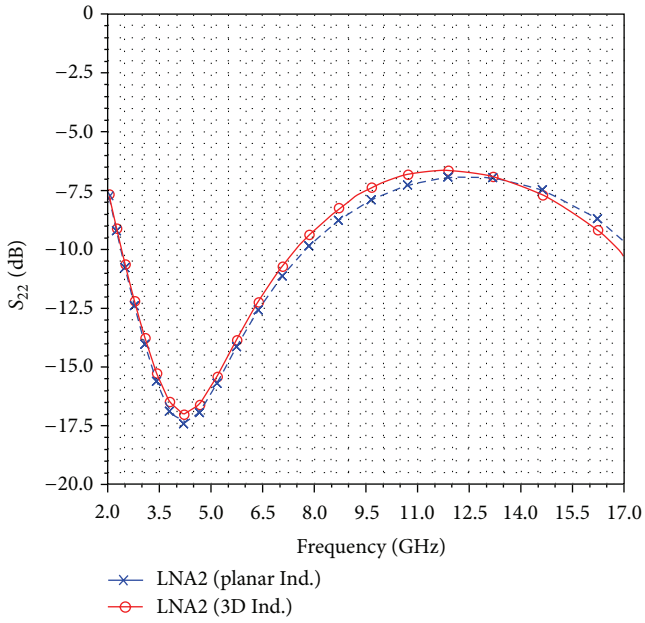

FIGURE 11: S_{22} (dB) of LNA2.

resonance circuit consisting of capacitor C_{out} and inductor L_{out} is used to match the LNA2 output impedance to its load (succeeding RF stage). The resistive termination R_{out} is used to control the load-output impedance match bandwidth.

A planar RF on-chip spiral inductor (L_{d1}) having an inductance of 14.5 nH and a maximum quality factor of 8.0 is needed as a load of the input CS stage to improve the current reuse stages matching. This RF integrated inductor occupies an area of 428 μm × 425 μm which represents a considerable part of the UWB LNA total die area.

One of the well-known difficulties facing the development of RFICs is inductors large area relative to other passive and active components. This area problem becomes more severe with the recent intensive shrinking of active devices and competitive reduction of fabrication cost [10].

Inductors quality factor (Q) reduction is another limiting factor of RFICs performance enhancement. The reduction of inductor Q factor is due to ohmic and substrate losses. Ohmic losses can be decreased by using a high conductive metal for inductor implementation. On the other hand placing a high resistive layer underneath the inductor can minimize the substrate losses. Lately optimized 3D structures and implementations of RF integrated inductors are suggested to overcome all of these limitations and improve the RF integrated inductors performance [4, 5].

For LNA2 circuit area reduction and RF inductor characteristics improvement, a symmetric 3D structure for RF integrated inductor implementation is suggested to replace the planar RF integrated inductor (L_{d1}). Similar to the design of planar RF inductor, 3D metallic structure layout should be drawn on a substrate to design and test a 3D integrated inductor [11]. 3D RF inductors structures are mainly consisting of serially connected different metal layers spirals having the same current flow direction. This 3D structure inductance is dependent on these different spirals inductances and the positive mutual coupling they have [11].

For 1P6 M CMOS technology which has six different metal layers, the proposed symmetric 3D RF integrated inductor has a complete spiral inductor on the highest metal layer ($M6$) . Half of the lower spiral is implemented using fourth metal layer ($M4$) to increase its inductance value due to the increased mutual coupling. The second metal layer ($M2$) which is distant from the top metal layer is employed to implement the lower spiral other half to reduce the parasitic components of that 3D metal structure and increase its quality factor. The suggested symmetric 3D inductor has an inductance of 14.5 nH, a quality factor of 8.5, and an area of 185 μm × 165 μm. 80% of planar inductor area is saved through this symmetric 3D structure while achieving the same inductance value and higher quality factor. Figure 5 shows a 3D view of the proposed symmetric RF integrated inductor.

3. Simulation Results and Discussion

The proposed UWB LNA (LNA1 and LNA2) circuits are designed in TSMC CMOS 0.18 μm technology process using Agilent Advanced Design System (ADS). Electromagnetic simulation is verified by the post-layout simulation results which are obtained using the Cadence design environment. The suggested symmetric 3D structure is designed and tested using Momentum simulation software and verified using Cadence design environment. The LNAs simulation results are given below.

3.1. Power Gain and Noise Figure. LNA1 has a gain of 17 ± 1.5 dB as shown in Figure 6. It also has a noise figure less than 2.3 dB over its operating band of frequency (3.1–10.6 GHz).

S_{21}(dB) of LNA2 is higher than 10 dB with a maximum value of 12 dB over the desired band of frequency (2.5–16 GHz). This high and flat gain is due to the use of inductive gain-peaking technique in addition to the control of the unity gain current cut-off frequencies of LNA2. Figure 7 shows that the proposed LNA2 employing the symmetric 3D RF integrated inductor achieves a gain of 11 ± 1.0 dB.

The proposed UWB LNA2 has an enhanced LNA noise performance. LNA2 NF ranges from 2.5 dB to 3.3 dB over the operating bandwidth (2.5–16 GHz). This NF reduction is accomplished due to the optimization of the LNA noise factor given by (4) and the use of weak shunt capacitive-resistive feedback implemented over the input stage. LNA2 achieves a NF less than 3.3 dB over the operating band of frequency as shown in Figure 8.

3.2. Input and Output Impedance Matching. LNA1 input and output ports have good matching conditions to its source and load, respectively. Simulation results of input and output reflection coefficients of LNA1 are shown in Figure 9. LNA1 has S_{11} and S_{22} less than −11 dB and −10 dB, respectively, over the UWB range of frequencies.

The proposed UWB LNA2 achieves good input impedance matching as shown in Figure 10. Good impedance

Table 1: Proposed UWB LNA performance summery in comparison to recently published UWB LNAs.

Reference	BW (GHz)	Gain (dB)	NF (dB)	S_{11} (dB)	S_{22} (dB)
This work (LNA2)*	**2.5~16**	**11 ± 1.0**	**<3.3**	**<−7**	**<−7.25**
This work (LNA1)*	**3.1~10.6**	**17 ± 1.5**	**<2.3**	**<−11**	**<−10**
LNA-1 [1]	1.7~5.9	11.2 ± 2.3	<4.7	<−11.8	<−12.7
LNA-2 [1]	1.5~11.7	12.2 ± 0.6	<4.8	<−8.6	<−10
[2]	3~10.6	15	<4.4	<−7	NA
[12]	3.1~10.6	10.8 ± 1.7	<6	<−10	<−9.3
[13]	1~5	12.7 ± 0.2	<3.5	<−8	NA

*Post-layout simulation results.

match between LNA2 and its source is obtained using the series-resonant input matching technique. The input return loss (S_{11}) is less than −7.0 dB over this wide range of frequency (2.5–16 GHz).

Figure 11 shows that better output impedance matching is obtained using the planar integrated inductor while simulating LNA2. Good output impedance matching of LNA2 over its operating band of frequency (2.5–16 GHz) is accomplished due to the optimization of the CG output matching stage with the aid of the output LC resonant circuit. R_{out} termination is used to widen the matching bandwidth. The output return loss (S_{22}) shown in Figure 11 is less than −7.25 dB for LNA2 using the planar inductor while it is less than −6.0 dB for LNA2 employing the proposed 3D inductor over the desired frequency band (2.5–16 GHz).

3.3. DC Power, Reverse Isolation, and Stability. LNA1 and LNA2 consume DC power of 12.8 mW and 20 mW, respectively, from a 1.8 V power source. The increased DC consumption of LNA2 is due to having enough driving bias for the CG output match stage.

Both of the proposed UWB LNA1 and LNA2 have a reverse isolation factor (S_{12}) less than −28 dB over each design bandwidth. The proposed UWB LNAs (LNA1 and LNA2) are unconditionally stable over their bandwidths.

Table 1 shows a summary of the proposed UWB LNAs performance in comparison to other recently published UWB LNAs implemented in 0.18 μm CMOS technology.

4. Conclusion

In this paper, two different UWB LNAs were presented. LNA1 has high gain, minimized noise figure, and good impedance match over the UWB range of frequencies. LNA2 has a wide range of operating frequency (2.5 GHz–16 GHz). UWB LNA2 consists of a current reuse cascaded amplifier with shunt resistive feedback followed by a CG output stage with resistive termination. LNA2 input stage use series-resonant impedance matching technique and employs a symmetric 3D RF integrated inductor as a load. The post-layout simulation results of LNA1 and LNA2 demonstrate the performance improvement achieved through theses designs. The next step is to implement these UWB LNAs to have a comparison between post-layout simulation results and measured results.

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