

## Research Article

# An Inductorless Cascaded Phase-Locked Loop with Pulse Injection Locking Technique in 90 nm CMOS

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An inductorless phase-locked loop with subharmonic pulse injection locking was realized (PLL area:  $0.11 \text{ mm}^2$ ) by adopting 90 nm Si CMOS technology. The proposed circuit is configured with two cascaded PLLs; one of them is a reference PLL that generates reference signals to the other one from low-frequency external reference signals. The other is a main PLL that generates high-frequency output signals. A high-frequency half-integral subharmonic locking technique was used to decrease the phase noise characteristics. For a 50 MHz input reference signal, without injection locking, the 1 MHz offset phase noise was  $-88 \text{ dBc/Hz}$  at a PLL output frequency of 7.2 GHz ( $= 144 \times 50 \text{ MHz}$ ); with injection locking, the noise was  $-101 \text{ dBc/Hz}$  (spur level:  $-31 \text{ dBc}$ ; power consumption from a 1.0 V power supply: 25 mW).

## 1. Introduction

Conventional multistandard wireless mobile terminals contain multiple RFICs. To reduce production costs, one-chip wideband RF LSI systems are desired. A great effort is being made to develop wideband and/or multiband RF solutions using highly scaled advanced CMOS processes. The use of such processes is beneficial to *A/D* and *D/A* converters and digital baseband circuits. However, it is very difficult to reduce the scale of RF/analog circuit blocks, especially power amplifiers and oscillator circuits, including voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs), because of the presence of inductors that do not scale with advancements in technology.

In designing VCOs which generate signals in RF systems, ring-type VCOs (ring VCOs) are more attractive than LC-resonant-type VCOs (LC VCOs) in terms of their small area and wide frequency tuning range since they do not use large passive devices. However, they have poor phase noise with relatively high power consumption. Nevertheless, low-phase-noise ring VCO is still a possibility if some noise-suppression mechanism is applied. One of available options would be injection locking.

In the early days, Adler [1] and many other authors studied the behavior of VCOs with injection locking. Also,

there are numerous papers published in reference to VCOs with injection locking in order to achieve phase locking and high performances. Moreover, recently, PLLs with an injection-locked frequency divider and frequency multiplier, and a clock and data recovery circuit (CDR) were presented.

This paper describes a study on a ring-VCO-based PLL with pulse injection locking as a potential solution to realize a scalable inductorless PLL, which can generate wideband frequency signal with low supply voltage. Usually, the frequency range utilized consumer RF applications, such as wireless LAN *a/b/g/n*, Bluetooth, and digital TV (DTV), is very wide and spreading from 400 MHz to 6 GHz. Table 1 shows target performance of the proposed PLL. Generally, in RF systems using high transmitting power, a frequency synthesizer should generate higher-frequency signals up to 12 GHz to avoid injection pulling from a power amplifier. Then, some methods, such as using frequency dividers and mixers, are applied to widen frequency range [2, 3].

In addition, the proposed PLL is augmented with high-frequency half-integral subharmonic locking in order to improve its phase-noise performance. In Section 2, brief features of the proposed PLL are explained. In Section 2.1, high-frequency half-integral subharmonic locking is shown as a method of reducing phase noise. Also, the proposed

TABLE 1: Target performance.

VCO	Ring
Frequency range	6–12 GHz
Phase noise at 1 MHz offset	−100 dBc/Hz
CMOS process	90 nm
Supply voltage	1.0 V

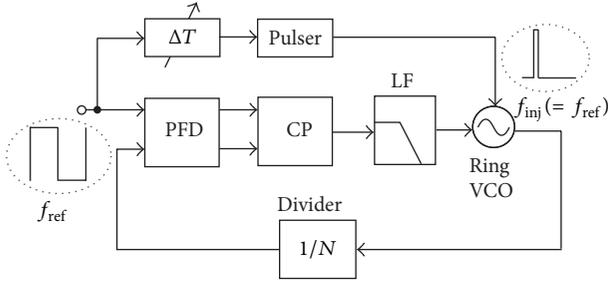


FIGURE 1: Injection-locked PLL with pulse injection.

cascaded PLL (CPLL) that can achieve injection locking at high frequencies from low-frequency reference is presented. Detailed circuit designs, such as a VCO and a charge pump which are able to realize wide-band operation, and the measurement results obtained from an implementation in 90 nm CMOS process are presented in Sections 3 and 4, respectively. Finally, we conclude this work in Section 5.

## 2. Injection Locking in Frequency Synthesizers

Figure 1 shows an injection-locked PLL (ILPLL). The PLL is based on a ring VCO that is able to generate high-frequency outputs across wide frequency range, as well as  $I/Q$  outputs. The PLL also consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a variable delay unit ( $\Delta T$ ), and a pulsar.

PLLs that use ring type VCOs are required to have a wide loop bandwidth of the phase-locked loop for lowering their poor phase noise characteristics. However, there is a trade-off between the loop bandwidth and the stability of PLLs. In general, the loop bandwidth ( $\omega_{-3\text{dB}}$ ) must be narrower than  $\omega_{\text{ref}}/20 \sim \omega_{\text{ref}}/10$ , where  $\omega_{\text{ref}}$  is the reference-signal frequency [4]. Consequently, there is a limitation on lowering the phase noise in ring-VCO-based charge-pump PLLs (CP PLLs). Figure 2 shows phase noise characteristics of the PLL. In this case, the charge-pump noise of the PLL is assumed to be small enough and can be neglected. In Figure 2, phase noise is suppressed up to the loop bandwidth ( $\omega_{-3\text{dB}}$ ) by the noise filtering of the loop. On the other hand, pulse injection locking is effective to reduce phase noise of ring VCOs since ring VCOs have a wider lock range with injection locking than that of LC VCOs because of their low quality factors. In designing subharmonically injection-locked oscillators (ILOs),  $N$  times frequency-multiplied signals as to the reference frequency

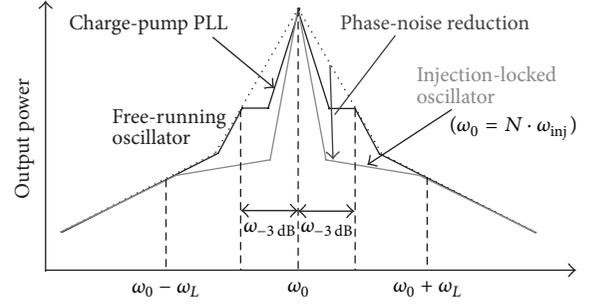


FIGURE 2: Phase-noise reduction with a charge-pump PLL and injection locking.

can be achieved. The lock range is decided by the power of  $N$ th superharmonics of the reference signal as follows [1, 5]:

$$\omega_L = \frac{\omega_{\text{out}}}{2Q} \cdot \sqrt{\frac{P_{\text{inj}N}}{P_0}}, \quad (1)$$

where  $Q$  represents the open-loop quality factor of an oscillator (calculated by using the open-loop transfer function of the oscillator [6]),  $\omega_{\text{out}}$  is the output frequency of the oscillator under injection locked condition,  $P_{\text{inj}N}$  is the  $N$ th harmonic power of the reference signal, and  $P_0$  is the free-running output power of the oscillator.  $P_{\text{inj}N}$  is approximately given by

$$P_{\text{inj}N} \propto \left\{ A \cdot D \frac{\sin(\pi D \cdot N)}{\pi D \cdot N} \right\}^2, \quad (2)$$

where  $A$  is the pulse amplitude,  $D$  is the duty cycle of pulses ( $D = \Delta T/T$ ,  $\Delta T$ : pulse width,  $T$ : period of pulses). From (1) and (2), the lock range  $\omega_L$  can be rewritten as follows:

$$\omega_L \propto \frac{\omega_{\text{inj}}}{2Q} \cdot \frac{|\sin(\pi D \cdot N)|}{\sqrt{P_0}}, \quad (3)$$

where  $\omega_{\text{inj}}$  ( $= \omega_0/N$ ) is the injection-signal frequency [7].

The overall ILO output phase noise is obtained by adding the noise contributions in an ILO. Assuming that  $S_{\text{ILO}}(\omega)$ ,  $S_{\text{REF}}(\omega)$ , and  $S_{\text{VCO}}(\omega)$  are phase noise power functions of an injection-locked VCO, a reference signal, and a free-running VCO, respectively, the phase noise of an ILO,  $S_{\text{ILO}}(\omega)$ , simply can be expressed as

$$\begin{aligned} S_{\text{ILO}}(\omega) &= S_{\text{REF},M}(\omega) \cdot |H_{\text{LPF}}(j\omega)|^2 + S_{\text{VCO}}(\omega) \cdot |H_{\text{HPF}}(j\omega)|^2 \\ &= M^2 \cdot S_{\text{REF}}(\omega) \cdot \frac{1}{1 + (\omega/\omega_L)^2} + S_{\text{VCO}}(\omega) \cdot \frac{(\omega/\omega_L)^2}{1 + (\omega/\omega_L)^2}, \end{aligned} \quad (4)$$

where  $S_{\text{REF},M}$  is the normalized phase noise power function with respect to the output frequency of  $f_{\text{out}}$ , and  $M$  means the ratio between the output frequency ( $f_{\text{out}}$ ) and the input frequency ( $f_{\text{inj}}$ ).  $H_{\text{LPF}}(j\omega)$  and  $H_{\text{HPF}}(j\omega)$  are low-pass and

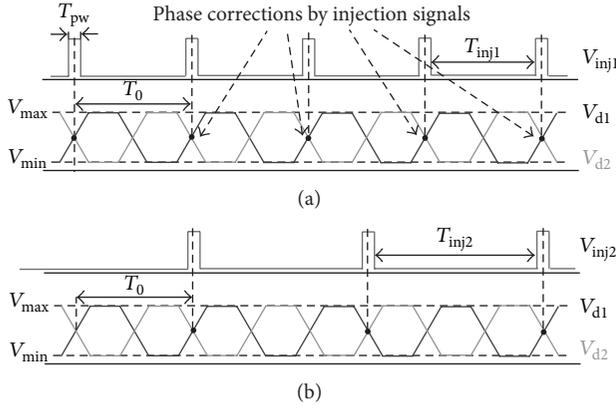


FIGURE 3: Voltage and current waveforms at differential output nodes of a VCO; (a) integral subharmonic locking ( $f_0 = f_{inj}$ ), (b) half-integral subharmonic locking ( $f_0 = 1.5f_{inj}$ ).

high-pass transfer functions, respectively [8]. Supposed that  $H_{HPF}(j\omega)$  and  $H_{LPF}(j\omega)$  have the first-order transfer functions and they have the same cutoff frequency of  $\omega_L$ , the simple equation of (4) would be achieved [5, 9, 10].

In the proposed PLL, there are two kinds of phase locking mechanism: one is a phase-locked loop, and the other is pulse injection locking. In general, either of them is enough for phase locking. However, those two mechanisms are combined to get a wide frequency range operation with a low-phase-noise performance. The phase-locked loop, which uses a charge pump for controlling the oscillation frequency, is implemented to ensure correct frequency locking over the entire VCO tuning range. The final phase locking is done by injection locking to reference signal [11–13].

**2.1. High-Frequency Half-Integral Subharmonic Locking Topology for Noise Reduction.** A paper on half-integral subharmonic injection locking based on the use of a ring VCO has been presented [8]. A differential VCO can be easily designed to lock to half-integral subharmonics by giving its necessary symmetry properties. Suppose that a VCO consists of differential circuits and has a certain symmetry. As a method to achieve injection locking, a direct injection technique is applied, which uses nMOS switches that short the differential outputs for phase corrections. Figure 3 shows differential waveforms ( $V_{d1}$ ,  $V_{d2}$ ) of the VCO in the case of both integral ( $f_0 = f_{inj}$ ) and half-integral subharmonic locking ( $f_0 = 1.5f_{inj}$ ). The two output nodes are shorted when the injection signal ( $V_{inj1}$ ,  $V_{inj2}$ ) is input into the nMOS switches. Phase corrections may occur at the time and the jitter is reduced. Generally, there are two points of time during the period of the output signal when two output nodes can be shorted because of topological symmetry as shown in Figure 3. Consequently, the differential VCO is capable of both integral and also half-integral subharmonic locking.

One advantage of using half-integral subharmonic locking is to be able to use high-frequency reference signal and can make the locking range of injection locking,  $\omega_L$  wide as shown in (1). Figure 2 and Equation (4) also show that

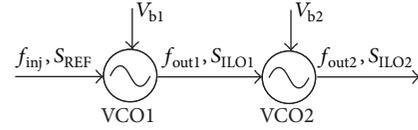


FIGURE 4: Concept of the cascaded ILOs.

the phase noise of the reference signal mainly affects the output phase noise at low offset frequencies and that the phase noise of the PLL becomes dominant as the offset frequency approaches the edge of the locking range [11]. Therefore, it will improve phase noise characteristics to the edge of the locking range to use high-frequency reference signals.

## 2.2. High-Frequency Signal Generation with Cascaded ILOs.

As shown in (3), the lock range is proportional to the input frequency of  $\omega_{inj}$ . However, narrower pulses are required to achieve smaller  $D$  with increasing the multiplication ratio ( $N$ ). Unfortunately, it is difficult to achieve sufficiently narrow pulses even with the use of nm-scale CMOS processes since the reference inputs also have certain jitter and parasitic components of the pulser limit the pulse width. In other words, there is limitation to generate high-frequency (over 5 GHz) injection-locked signals with low-frequency reference such as XTALs.

One solution is to employ cascaded oscillators [11], which make each multiplication ratio ( $N$ ) smaller by using two multiplication processes. Figure 4 shows the concept of the cascaded ILOs. Firstly, the input signal, which has sufficiently high-power superharmonics, is injected into VCO1. Then,  $M_1$  multiplied frequency signal ( $f_{out1} = M_1 \cdot f_{inj}$ ) of the reference frequency can be achieved by tuning the VCO1 oscillation frequency properly. In this case, the output phase noise of VCO1 with injection locking can be expressed as follows:

$$S_{ILO1}(\omega) = M_1^2 \cdot S_{REF}(\omega) \cdot \frac{1}{1 + (\omega/\omega_{L1})^2} + S_{VCO1}(\omega) \cdot \frac{(\omega/\omega_{L1})^2}{1 + (\omega/\omega_{L1})^2}, \quad (5)$$

where  $\omega_{L1}$  is the lock range that is proportional to the input frequency ( $f_{inj}$ ) and can be calculated from (3).

The output signal of VCO1 is injected into VCO2 and locked to the output of VCO1 with the same process occurred in VCO1. Also, the output phase noise of VCO2 with injection locking can be expressed as follows:

$$S_{ILO2}(\omega) = M_2^2 \cdot S_{ILO1}(\omega) \cdot \frac{1}{1 + (\omega/\omega_{L2})^2} + S_{VCO2}(\omega) \cdot \frac{(\omega/\omega_{L2})^2}{1 + (\omega/\omega_{L2})^2} \quad (6)$$

$$\approx M_2^2 \cdot \frac{1}{1 + (\omega/\omega_{L2})^2} \cdot S_{ILO1}(\omega), \quad (7)$$

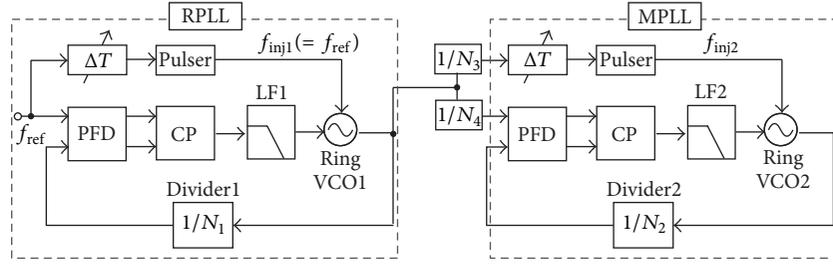


FIGURE 5: Proposed cascaded injection-locked PLL (CPLL) with pulse injection.

TABLE 2: Dividers ratio in Figure 5.

$N_1$	$N_2$	$N_3$	$N_4$
32	24, 36	1, 8	4, 8

where  $M_2$  is the ratio between the output frequency of VCO2 ( $f_{out2}$ ) and input frequency ( $f_{out1}$ ) and  $\omega_{L2}$  is the lock range of VCO2. When the offset frequency of  $\omega$  is sufficiently lower than  $\omega_{L2}$  (i.e.,  $\omega \ll \omega_{L2}$ ), (7) is held. In other words, sufficiently wide lock range makes it possible to neglect the secondary VCO phase noise up to the lock range in cascaded ILOs.

### 3. Proposed Injection-Locked PLL Topology

Figure 5 shows the configuration of the proposed PLL that enables the use of half-integral subharmonic locking, which was proposed in our previous work [13]. The proposed PLL consists of two injection-locked PLLs. A reference PLL, namely, RPLL generates reference signals to a main PLL, namely, MPLL from low-frequency external reference signals. In this topology, when we choose divider ratios (Table 2), respectively as,  $N_2 = 36$ ,  $N_3 = 1$ , and  $N_4 = 8$ , the ratio between the reference signal to MPLL and the output frequency of MPLL may be 4.5 and high-frequency half-integral subharmonic locking can be applied. Variable time delay cells  $\Delta T$ s are implemented to control the time when injection signals are input because phase corrections can occur easily when differential output nodes are shorted in the direct injection locking scheme (Figure 3).

**3.1. Main PLL.** Figure 6(a) shows the topology of the proposed delay cell that composes a ring VCO [13]. The delay cell contains an inverter latch as a negative conductance circuit that generates delay by positive feedback in order to satisfy the oscillation condition [14]. To tune the VCO output frequency widely, variable pMOS resistive loads are used. However, in the commonly used delay cells with pMOS resistive loads, the range of control voltage is limited from 0 V to the pMOS threshold voltage. In the proposed delay cell, a pMOS transistor is added into which the subcontrol voltage ( $V_{bn}$ ) is input in order to make the range of sensitive voltages identical to the rail-to-rail voltage range (0 V to  $V_{DD}$ ). For this purpose, the bias level shifted by about  $V_{DD}/2$ ,  $V_{bn}$ , is input to the added pMOS transistor. As a result,

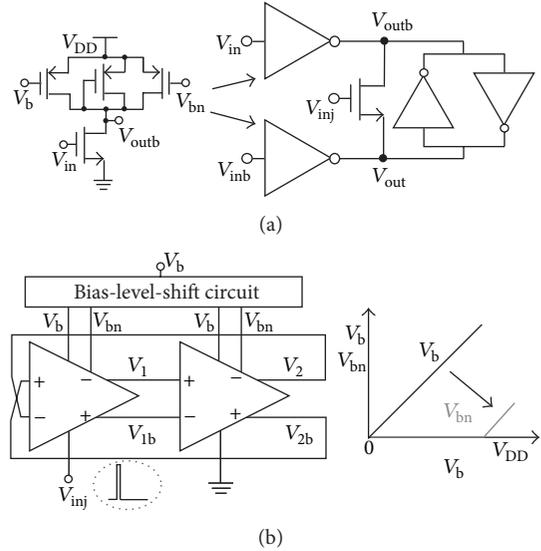


FIGURE 6: (a) Proposed differential delay cell, (b) two-stage differential VCO of MPLL with a bias-level-shift circuit.

the total equivalent resistance of the two pMOS transistors in parallel changes almost linearly versus the main control voltage,  $V_b$ . Consequently, the VCO output frequency can be tuned linearly across the wide tuning range [12, 13]. An nMOS switches are connected at the nodes between the differential nodes to achieve injection locking [15].

The proposed ring VCO is shown in Figure 6(b). It is based on a two-stage pseudo differential ring oscillator. Pulses which are generated by the on-chip pulser are injected into the left delay cell in the form of rail-to-rail pulses for injection locking. To maintain topological symmetry, an nMOS switch biased to 0 V is also applied in the right-side delay cell. We achieved the VCO tuning range of 6.02 GHz to 11.1 GHz across the rail-to-rail control voltage from the postlayout simulation of the VCO core with output buffers (90 nm CMOS process,  $V_{DD} = 1.0$  V).

A tristate phase/frequency detector (PFD) is implemented, which consists of two D-flip flops, delay-path inverters, and an AND logic. The PFD detects phase and frequency difference between the reference signal and the divided VCO output and generates output pulses of  $V_{UP}$  and  $V_{DN}$  which are input into the charge pump to reduce the difference.

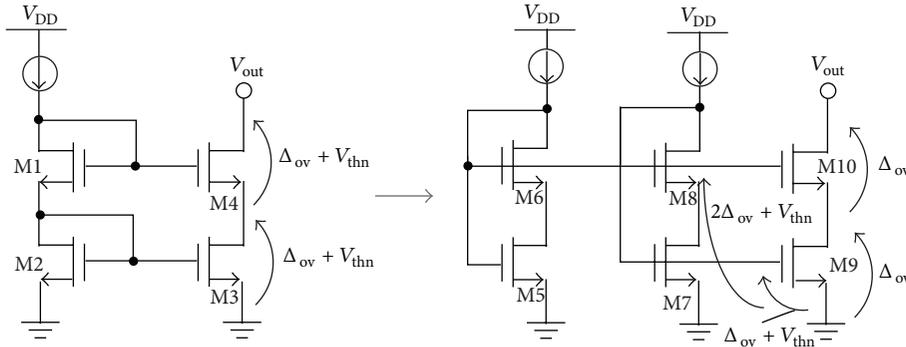


FIGURE 7: Sooch cascode current mirror circuit.

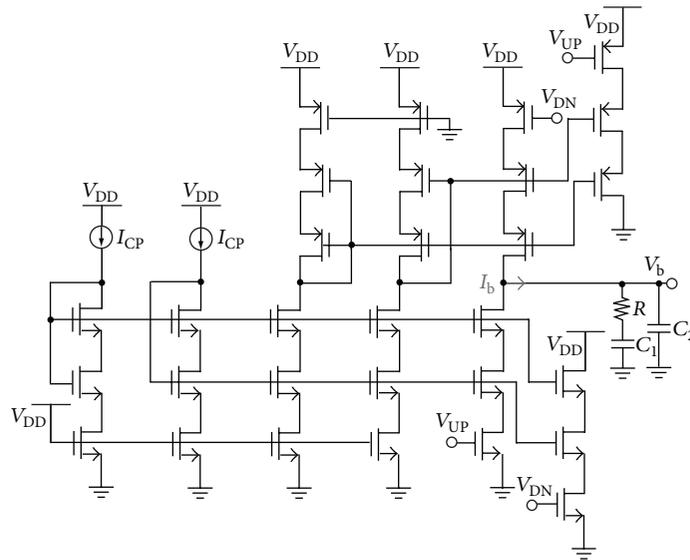


FIGURE 8: Proposed charge-pump (CP) circuit and loop filter (LF).

Figure 7 shows an implemented current mirror circuit to generate stable constant current from the charge pump. Usually, stacked current mirrors design can obtain better DC headroom and linearity with longer channel lengths as shown in the left side of Figure 7. In this case, DC headroom of the output voltage ( $V_{out}$ ) is expressed as  $2(\Delta_{ov} + V_{thn})$ , where  $\Delta_{ov}$  is the overdrive voltage of MOS transistors (M3, M4), and  $V_{thn}$  is an nMOS threshold voltage. In the case of Sooch cascode current mirror as shown in the right side of Figure 7, the MOS transistor, M5, is forced to operate in the triode region. The DC headroom can be reduced as  $2\Delta_{ov}$  since MOS transistors operate in the saturation region except for M5 [16]. Consequently, low voltage operation can be achieved.

Proposed current switching charge pump (CP) that employs Sooch cascode current mirror is shown in Figure 8. Dummy switches are also implemented to maintain the balance between PFD outputs. Two external current sources ranged from  $10 \mu A$  to  $150 \mu A$  are used.

Figure 9 shows postlayout simulation results of the proposed charge pump, when  $I_{CP} = 20 \mu A$  (90 nm CMOS process, 1.0 V supply). It shows that the charge pump can generate quite constant output current across the wide range

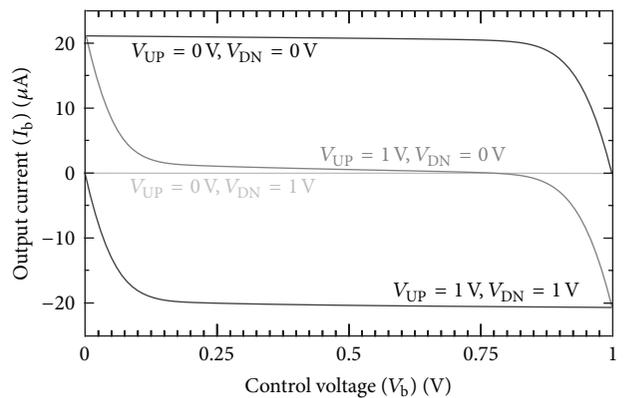


FIGURE 9: Charge-pump output current versus the control voltage ( $V_b$ ), when  $I_{CP} = 20 \mu A$ .

of the output voltage ( $V_b$ ). When  $V_{UP} = 1 V$  and  $V_{DN} = 0 V$ , the result shows current mismatch between the up and down output currents as a function of the output voltage ( $V_b$ ). The percentage mismatch error for  $0.48 V \leq V_b \leq 0.81 V$  is less

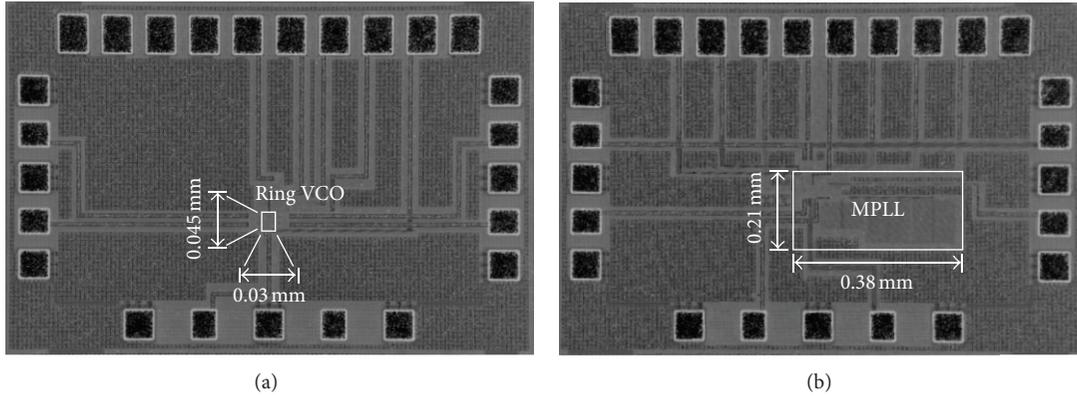


FIGURE 10: Chip micrographs; (a) proposed VCO and (b) proposed PLL.

than 2% and increases to less than 5% for  $0.21 \text{ V} \leq V_b \leq 0.85 \text{ V}$ .

A second-order lag-lead filter that consists of a register and two capacitors is implemented as a loop filter (LF) of the loop to suppress the charge-pump ripple. ( $R = 16 \text{ k}\Omega$ ,  $C_1 = 41 \text{ pF}$ ,  $C_2 = 12 \text{ pF}$ ). In this case, on-chip MIM capacitors were used.

The frequency divider consists of differential pseudo-nMOS latches to minimize chip area and achieve low power consumption [17]. The frequency divider chain consists of three divide-by-2 circuits and one divide-by-2/3 circuit. As a result, it can divide by 24 and 36 in the loop (i.e., divider ratio  $N_1 = 24, 36$ ).

The loop dynamic characteristics are designed to have the unity-gain bandwidth of 2.8 MHz and phase margin of  $16^\circ$  (VCO gain: 5 GHz/V,  $I_{CP} = 20 \mu\text{A}$ , divider ratio  $N_1 = 24$ ). When the divider ratio  $N_1$  equals to 36, the unity-gain bandwidth of 2.2 MHz and phase margin of  $19^\circ$  are achieved. The PLL has poor phase margin that is related to the low damping factor and the slow settling time, because final phase locking is done not only by the phase-locked loop but also by injection locking. Injection locking that is applied into a phase-locked loop helps the phase margin to be improved [21]. In this case, large capacitance of  $C_2$  is required to suppress the reference spur level due to the control voltage ripple. A loop bandwidth of the PLL is designed to be small enough compared to the lock range of injection locking to avoid the interference between two phase locking but can still achieve frequency locking.

To achieve subharmonic locking, an AND-based pulser is used, which is able to tune the pulse width below 40 ps by the analog control. Also, a variable time-delay unit ( $\Delta T$ ) which consists of inverters and tristate inverters was applied to match the zero-crossing points of differential VCO outputs to the pulses for effective injection locking.

**3.2. Reference PLL.** The proposed ring VCO used in RPLL is based on a four-stage pseudo differential ring oscillator. The same delay cell shown in MPLL (Figure 6(a)) is applied to widen frequency tuning range linearly. Also, long-gate channel MOS transistors are equipped in the delay cell to decrease VCO oscillation frequencies and reduce flicker noise

characteristics as a reference signal into MPLL. Pulses which are generated by the on-chip pulser are injected into the left delay cell in the form of rail-to-rail pulses for injection locking. To maintain topological symmetry, an nMOS switch biased to 0 V is also applied in the other delay cells. We achieved the VCO tuning range of 0.805 GHz to 2.85 GHz across the rail-to-rail control voltage from the postlayout simulation of the VCO core with output buffers (90 nm CMOS process,  $V_{DD} = 1.0 \text{ V}$ ).

The tristate PFD and CP presented in Figure 8 are implemented in RPLL. With postlayout simulation results of the charge pump (90 nm CMOS process, 1.0 V supply), the percentage mismatch error ( $I_{CP} = 100 \mu\text{A}$ ) for  $0.32 \text{ V} \leq V_b \leq 0.70 \text{ V}$  is less than 2% and increases to less than 5% for  $0.24 \text{ V} \leq V_b \leq 0.76 \text{ V}$  ( $V_{UP} = 1 \text{ V}$ ,  $V_{DN} = 0 \text{ V}$ ).

As a loop filter (LF), a second-order lag-lead filter is implemented. The filter consists of a register ( $R = 16 \text{ k}\Omega$ ), and two on-chip capacitors ( $C_1 = 41 \text{ pF}$ ,  $C_2 = 1 \text{ pF}$ ). The frequency divider chain in RPLL consists of five divide-by-2 circuits. As a result, it can divide by 32 (i.e., divider ratio  $N_2 = 32$ ). Finally, the AND-based pulser and the variable time-delay unit ( $\Delta T$ ) were implemented for effective injection locking. In RPLL, an injection frequency of  $f_{inj1}$  is same to a reference frequency of  $f_{ref}$ .

## 4. Measurement Results

**4.1. Main PLL (MPLL).** Figures 10(a) and 10(b) show chip micrograph of the differential ring VCO and a PLL, respectively. To clear the effectiveness of the proposed PLL, the VCO cell used in the PLL was also fabricated. They were fabricated by a 90 nm Si CMOS process. The area of the ring VCO core is  $0.030 \times 0.045 \text{ mm}^2$  including the bias-level-shift circuit and the pulser. The PLL circuit occupies an area of  $0.38 \times 0.21 \text{ mm}^2$ . They were measured in 1.0 V supply condition. Also, the PLL circuit was measured using  $20 \mu\text{A}$ -current-sources ( $I_{CP}$ ) into the charge pump.

During free-running operation, the frequency tuning range of the VCO was from 6.35 GHz to 11.5 GHz as shown in Figure 11. It was measured by using an Agilent Technologies E5052B signal source analyzer. It also shows that the VCO

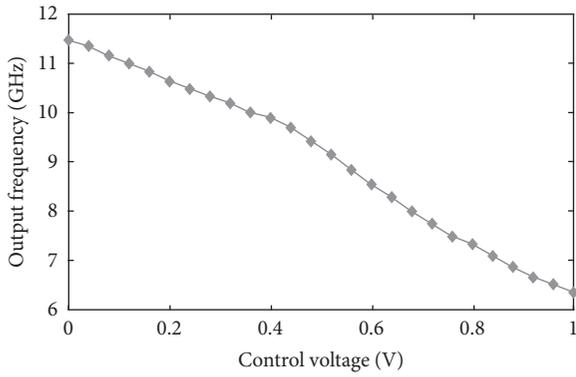


FIGURE 11: Measured frequency tuning range of the VCO.

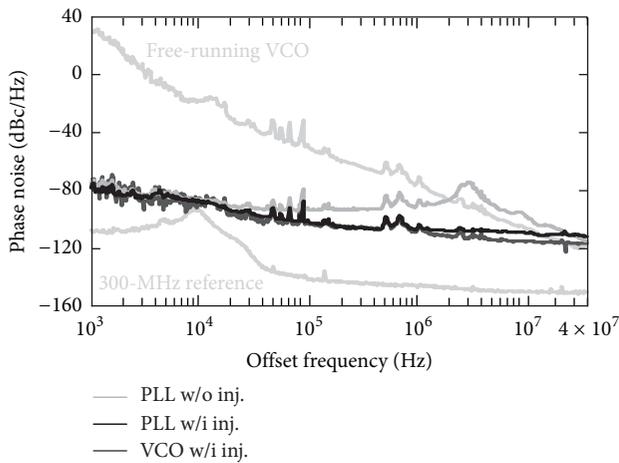


FIGURE 12: Measured phase noise characteristics at 7.2 GHz from the VCO and PLL output without and with injection locking.

output frequency could be tuned quite linearly versus the rail-to-rail control voltage ( $V_b$ ) due to the bias-level-shift circuit. When the VCO output frequency ( $f_0$ ) is 7.18 GHz, the total power consumption of the VCO (with the bias-level-shift circuit and pulser) was 8.4 mW.

Phase noise characteristics of the VCO and PLL at  $f_0 \approx f_{out} = 7.2$  GHz without and with injection locking are shown in Figure 12 as measured by the signal source analyzer. In addition to them, phase noise characteristics of the 300 MHz reference signal are shown in Figures 12 and 14. A 1 MHz-offset phase noise of  $-75.8$  dBc/Hz was generated in the free-running VCO. With injection locking, a 1 MHz offset phase noise of  $-108$  dBc/Hz was generated, which was improved by 32 dB compared to the former. On the other hand, a 1 MHz-offset phase noise of  $-91.3$  dBc/Hz was generated in the PLL when the PLL was only locked by the phase-locked loop. Due to the poor phase margin, gain peaking at the offset frequency of about 3 MHz was observed. With injection locking, a 1 MHz offset phase noise of  $-107$  dBc/Hz was generated, which was improved by 16 dB compared to the former.

Figure 13 shows calculated phase noise characteristics by using (4) and the measurement phase noise of the free-running VCO and the reference signal as shown in Figure 12.

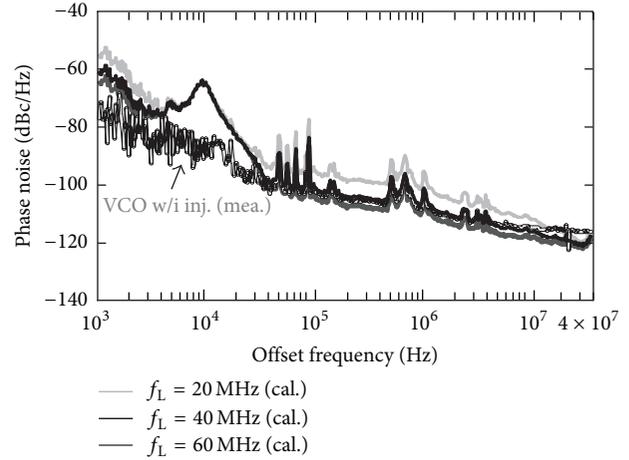


FIGURE 13: Calculated phase noise by using (4) and measure phase noise characteristics as shown in Figure 12.

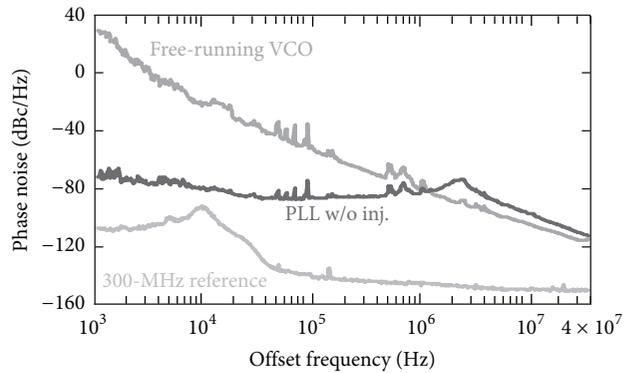


FIGURE 14: Measured phase noise characteristics at 10.8 GHz from the VCO and PLL output without injection locking.

The results show that wider lock range makes lower phase noise characteristics within the lock range. From the calculated result of  $f_L = \omega_L/2\pi = 40$  MHz, (4) is well matched to the measurement results except the offset-frequency region up to about 30 kHz. It is because that flicker noise model as expressed in [5] is not included for simplicity and certain spurs occurred at the offset frequency of about 10 KHz were measured.

Phase noise characteristics of the VCO and PLL at  $f_0 \approx f_{out} = 10.8$  GHz are shown in Figure 14. A 1 MHz offset phase noise of  $-79.5$  dBc/Hz and  $-83.7$  dBc/Hz were generated in the free-running VCO and the PLL, respectively. Phase noise reduction with injection locking could not be achieved since it was difficult to generate effective injection pulses with sufficient power for achieving the injection-locked condition at that high output frequency.

4.2. Cascaded PLL. Figure 15 shows a chip micrograph of the proposed CPLL. It was fabricated by a 90 nm Si CMOS process. It includes both RPLL and MPLL that occupy an area of  $0.11$  mm<sup>2</sup>. It was measured in 1.0 V supply condition. Also, the PLL circuit was measured using 100  $\mu$ A current

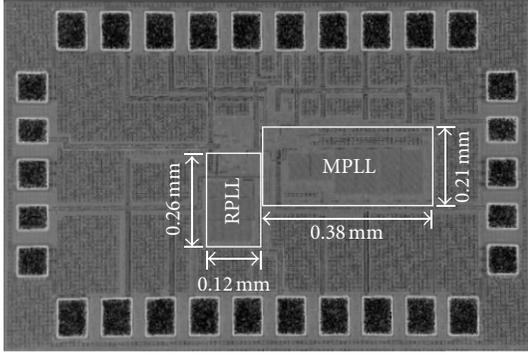


FIGURE 15: A chip micrograph of the proposed cascaded PLL.

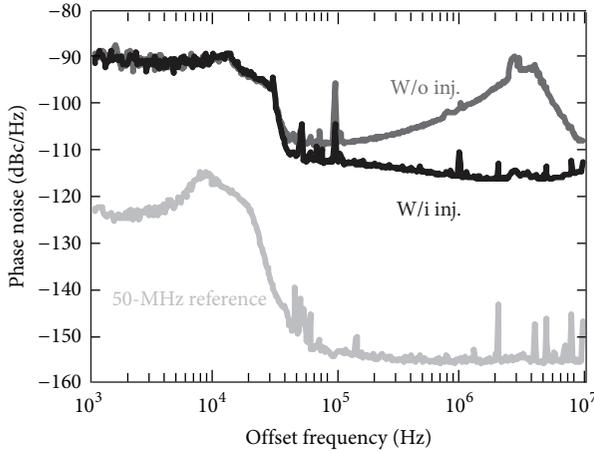


FIGURE 16: Measured phase noise characteristics of RPLL output at 1.6 GHz.

sources into RPLL charge pump and  $20 \mu\text{A}$  current-sources into MPLL charge pump. RPLL was locked to reference signals of 50 MHz which were generated by the pulse pattern generator.

Figure 16 shows the phase noise characteristics at  $f_{\text{rout}} = 1.6 \text{ GHz}$  ( $= 32 \times 50 \text{ MHz}$ ) as measured by an Agilent Technologies E5052A signal source analyzer. Without injection locking, a 1 MHz-offset phase noise of  $-100 \text{ dBc/Hz}$  was generated in RPLL. Due to the poor phase margin, gain peaking at the offset frequency of about 4 MHz was observed. With injection locking, the measured phase noise was  $-116 \text{ dBc/Hz}$  at an offset of 1 MHz. It shows a 16-dB phase-noise reduction with injection locking. Also, phase noise characteristics of the external reference signal are shown Figure 16. At 10 KHz and 1 MHz offset, the phase noise of the reference signal were  $-117$  and  $-155 \text{ dBc/Hz}$ , respectively.

Figure 17 shows the phase noise characteristics at  $f_{\text{mout}} = 7.2 \text{ GHz}$  ( $= 144 \times 50 \text{ MHz}$ ). 0.2 GHz injection signals were injected when  $N_2$ ,  $N_3$ , and  $N_4$  are corresponding to 36, 8, and 8, respectively. Also, 1.6 GHz injection signals were injected when  $N_2$ ,  $N_3$ , and  $N_4$  are corresponding to 36, 1, and 8, respectively. Without injection into MPLL, a 1 MHz offset phase noise of  $-88 \text{ dBc/Hz}$  was generated in the PLL. With integral subharmonic injection locking ( $f_{\text{mout}} = 36 \times$

TABLE 3: Performance summary at  $f_{\text{out}} = 7.2 \text{ GHz}$ .

This work	MPLL VCO	MPLL	CPLL	
$f_{\text{out}}$ [GHz]		7.2		
$f_{\text{ref}}$ [MHz]	—	300	50	
$f_{\text{inj}}$ [MHz]	300	300	200	1600
$f_{\text{out}}/f_{\text{inj}}$	24	24	36	4.5
$L(\Delta f) _{\Delta f=1 \text{ MHz}}$ [dBc/Hz]	-108	-107	-99	-101
Power consumption [mW]	8.4	14	25	
Area [ $\text{mm}^2$ ]	0.0014	0.080	0.11	

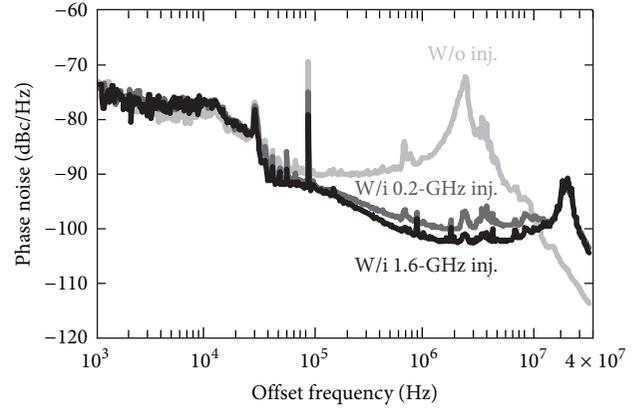


FIGURE 17: Measured phase noise characteristics of CPLL output at 7.2 GHz.

$f_{\text{inj}2}$ ,  $f_{\text{inj}2} = 0.2 \text{ GHz}$ ), the measured phase noise was  $-99 \text{ dBc/Hz}$  at an offset of 1 MHz. With high-frequency half-integral subharmonic locking ( $f_{\text{mout}} = 4.5 \times f_{\text{inj}2}$ ,  $f_{\text{inj}2} = 1.6 \text{ GHz}$ ), we successfully achieved 2 dB lower phase noise at 1 MHz offset than the former. A 4 MHz offset phase noise was improved by 4 dB in the latter case, compared with the former. The results show that high-frequency reference injections can widen the injection lock range. However, there was a spur around the offset frequency of 25 MHz owing to the RPLL spur level, and the spur limited the lock range widening with high-frequency signal injections.

Usually, spurs are induced by periodic phase shift due to injection locking. The spur level can be expressed as follows:

$$\sqrt{\frac{P_{\text{spur}, \omega_{\text{inj}}}}{P_0}} \approx \frac{\omega_0}{2Q\omega_{\text{inj}}} \cdot \sqrt{\frac{P_{\text{inj}N}}{P_{\text{osc}}}} = \frac{\omega_L}{\omega_{\text{inj}}}, \quad (8)$$

where  $P_{\text{spur}, \omega_{\text{inj}}}$  represents the spur levels occurred by the reference signal at  $f_0 \pm f_{\text{inj}}$ , and  $P_0$  is the injection-locked output power of the oscillator [22]. As shown in this equation, the spur level would be reduced lowering the lock range with the same reference frequency, however, which is undesirable to reduce phase noise characteristics.

Calculated phase noise characteristics by using (6) and measure phase noise characteristics, as shown in Figures 12 and 16, are shown in Figure 18. In this case, the lock range was supposed to be proportional to the input frequency and the coefficient was 0.14, which was expected in Figure 13. In

TABLE 4: Performance comparison of PLLs.

Reference	CMOS Technology	$f_0$ [GHz]	$N = f_0/f_{ref}$	$L_{in-band}$ [dBc/Hz]	$L_{normalized}^*$ [dBc/Hz <sup>2</sup> ]	Power [mW]	Area [mm <sup>2</sup> ]	VCO
This work	90 nm	1.6	32	-116	-223	11 (sim.)	0.031	Ring
		7.2	144	-101	-221	25	0.11	
		9.6	192	-93	-216	27		
[11]	90 nm	20	20	-113	-229	38	0.46	LC
[18]	90 nm	9.24	35	-97	-212	56	0.09	Ring
[19]	0.18 $\mu$ m	8.98	17	-110	-222	58	0.77	LC
[20]	0.18 $\mu$ m	8.45	32	-98	-212	117	5.5	LC

\*Normalized in-band phase noise =  $L_{in-band} - 20\log N - 10\log f_{ref}$ .

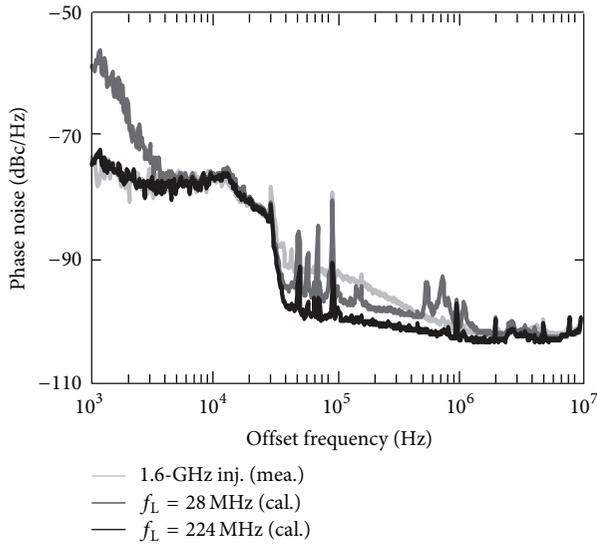


FIGURE 18: Calculated phase noise by using (6) and measuring phase noise characteristics as shown in Figures 12 and 16.

the results, phase noise characteristics especially at the offset frequency of 500 kHz, 700 kHz, and lower than 5 kHz due to the secondary VCO (VCO2) would be reduced by using high-frequency injection signals ( $f_{inj} = 1.6$  GHz,  $f_L = 224$  MHz). In Figure 18, measured phase noise characteristics from the offset frequency of 30 kHz to 1 MHz were degraded compared with calculated results due to induced noise from the MPLL loop.

Figure 19 shows the phase noise characteristics at  $f_{mout} = 9.6$  GHz ( $= 192 \times 50$  MHz). In these cases,  $N_2$ ,  $N_3$ , and  $N_4$  are corresponding to 24, 8, and 8, respectively. Without injection into MPLL, a 1 MHz offset phase noise of  $-85$  dBc/Hz was generated in the PLL. With integral subharmonic injection locking ( $f_{mout} = 48 \times f_{inj2}$ ,  $f_{inj2} = 0.2$  GHz), the measured phase noise was  $-93$  dBc/Hz at an offset of 1 MHz. In Figure 19, spur levels around the offset frequency of 25 MHz were decreased, because the phase-locking effect of injection locking was decreased.

The PLL generated reference spurs of lower than  $-31$  dBc at the output frequency of 7.2 GHz with 1.6 GHz injections, as shown in Figure 20(a). At the output frequency of 9.6 GHz with 0.2 GHz injections, reference spurs of lower than  $-27$  dBc were measured as shown in Figure 20(b).

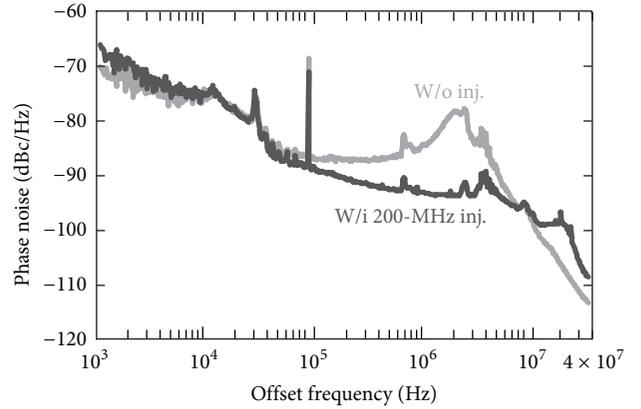


FIGURE 19: Measured phase noise characteristics of CPLL output at 9.6 GHz.

A performance summary at the output frequency of 7.2 GHz of the fabricated chips are given in Table 3, when injection locking was established. It shows that high-frequency injections are effective to reduce the phase noise because a wide injection lock range can be achieved.

A performance comparison of the PLL with other PLLs that were designed using various kinds of phase-locking methods is given in Table 4. Unfortunately, the proposed PLL cannot cover wide frequency range from 6 GHz to 12 GHz as shown in Table 1, due to the VCO tuning range and limitation of tunable divider ratio. To make a fair in-band phase noise comparison between various kinds of PLL designs, the dependency of in-band phase noise on  $f_{ref}$  and  $N$  should be normalized out [23]. Therefore, normalized in-band phase noise  $L_{normalized}$  was applied for comparison. The proposed PLL shows a relatively good  $L_{normalized}$  value. Also its area and power consumption are small and comparable to that of other circuits.

## 5. Conclusion

An inductorless PLL architecture, using the combination of a phase-locked loop, and injection locking with a ring VCO was proposed. The proposed CPLL that consists of two PLLs was designed in order to generate high-frequency output signals with low-frequency external reference signals. High-frequency half-integral subharmonic injection locking

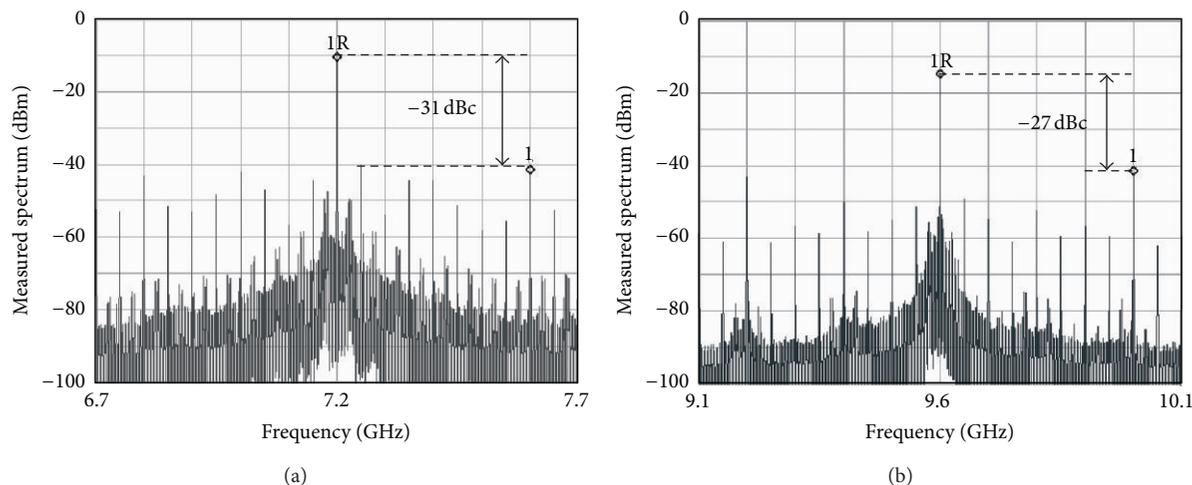


FIGURE 20: Measured frequency spectra of CPLL output (a) at 7.2 GHz and (b) at 9.6 GHz.

to improve the phase noise characteristics of the inductorless PLL was implemented.

The injection-locked PLL was fabricated by adopting 90 nm Si CMOS technology. A 1 MHz-offset phase noise of  $-101$  dBc/Hz was achieved at an output frequency of 7.2 GHz, which was improved by 25 dB compared with that of the free-running VCO. The area of this inductorless PLL was as small as  $0.11 \text{ mm}^2$  with low power consumption of 25 mW.

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## References

- [1] R. Adler, "A study of locking phenomena in oscillators," *Proceedings of the IRE*, vol. 34, pp. 351–357, 1946.
- [2] Y. Ito, H. Sugawara, K. Okada, and K. Masu, "A 0.98 to 6.6 GHz tunable wideband VCO in a 180 nm CMOS technology for reconfigurable radio transceiver," in *Proceedings of the IEEE Asian Solid-State Circuits Conference (ASSCC '06)*, pp. 359–362, November 2006.
- [3] B. Razavi, "Cognitive radio design challenges and techniques," *The IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, 2010.
- [4] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Transactions on Communications*, vol. 28, no. 11, pp. 1849–1858, 1980.
- [5] X. Zhang, X. Zhou, and A. S. Daryoush, "A theoretical and experimental study of the noise behavior of subharmonically injection locked local oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 5, pp. 895–902, 1992.
- [6] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, 1996.
- [7] S. Lee, N. Kanemaru, S. Ikeda et al., "A ring-VCO-based injection-locked frequency multiplier with novel pulse generation technique in 65 nm CMOS," *IEICE Transactions on Electronics*, vol. 95, no. 10, pp. 1589–1597, 2012.
- [8] Y. Kobayashi, S. Amakawa, N. Ishihara, and K. Masu, "A low-phase-noise injection-locked differential ring-VCO with half-integral subharmonic locking in  $0.18 \mu\text{m}$  CMOS," in *Proceedings of the 35th European Solid-State Circuits Conference (ESSCIRC '09)*, pp. 440–443, September 2009.
- [9] T. Sugiura and S. Sugimoto, "FM noise reduction of Gunn-effect oscillators by injection locking," *Proceedings of the IEEE*, vol. 57, no. 1, pp. 77–78, 1969.
- [10] M. C. Chen and C. Y. Wu, "Design and analysis of CMOS subharmonic injection-locked frequency triplers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 8, pp. 1869–1878, 2008.
- [11] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *The IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, 2009.
- [12] S. Y. Lee, S. Amakawa, N. Ishihara, and K. Masu, "Low-phase-noise wide-frequency-range ring-VCO-based scalable PLL with subharmonic injection locking in  $0.18 \mu\text{m}$  CMOS," in *Proceedings of the IEEE MTT-S International Microwave Symposium Digest (MTT '10)*, pp. 1178–1181, May 2010.
- [13] S. Y. Lee, S. Amakawa, N. Ishihara, and K. Masu, "High-frequency half-integral subharmonic locked ring-VCO-based scalable PLL in 90 nm CMOS," in *Proceedings of the IEEE Asia-Pacific Microwave Conference (APMC '10)*, pp. 586–589, December 2010.
- [14] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, NY, USA, 2001.
- [15] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1170–1174, 2004.
- [16] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, New York, NY, USA, 4th edition, 2001.
- [17] T. Sekiguchi, S. Amakawa, N. Ishihara, and K. Masu, "Inductorless 8.9 mW 25 Gb/s 1:4 DEMUX and 4 mW 13 Gb/s 4:1 MUX in 90 nm CMOS," *Journal of Semiconductor Technology and Science*, vol. 10, no. 3, pp. 176–184, 2010.

- [18] H. Kodama, H. Okada, H. Ishikawa, and A. Tanaka, "Wide lock-range, low phase-noise PLL using interpolative ring-VCO with coarse frequency tuning and frequency linearization," in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC '07)*, pp. 349–352, September 2007.
- [19] G. Y. Tak, S. B. Hyun, T. Y. Kang, B. G. Choi, and S. S. Park, "A 6.3–9 GHz CMOS fast settling PLL for MB-OFDM UWB applications," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 8, pp. 1671–1679, 2005.
- [20] T. Y. Lu and W. Z. Chen, "A 3-to-10GHz 14-band CMOS frequency synthesizer with spurs reduction for MB-OFDM UWB system," in *Proceedings of the IEEE International Solid-State Circuits Conference—Digest of Technical Papers (ISSCC '08)*, pp. 126–601, February 2008.
- [21] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, 2002.
- [22] M. M. Izad and C. Heng, "A pulse shaping technique for spur suppression in injection-locked synthesizers," *The IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 652–664, 2012.
- [23] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A 2.2 GHz 7.6 mW sub-sampling PLL with  $-126$  dBc/Hz in-band phase noise and 0.15 psrms jitter in  $0.18 \mu\text{m}$  CMOS," in *Proceedings of the IEEE International Solid-State Circuits Conference—Digest of Technical Papers (ISSCC '09)*, pp. 392–393, 393a, February 2009.



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