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Research Article

Ultrathin Oxide Passivation Layer by Rapid Thermal Oxidation for the Silicon Heterojunction Solar Cell Applications

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It is difficult to deposit extremely thin a-Si:H layer in heterojunction with intrinsic thin layer (HIT) solar cell due to thermal damage and tough process control. This study aims to understand oxide passivation mechanism of silicon surface using rapid thermal oxidation (RTO) process by examining surface effective lifetime and surface recombination velocity. The presence of thin insulating a-Si:H layer is the key to get high V_{oc} by lowering the leakage current (I_0) which improves the efficiency of HIT solar cell. The ultrathin thermal passivation silicon oxide (SiO_2) layer was deposited by RTO system in the temperature range 500–950°C for 2 to 6 minutes. The thickness of the silicon oxide layer was affected by RTO annealing temperature and treatment time. The best value of surface recombination velocity was recorded for the sample treated at a temperature of 850°C for 6 minutes at O_2 flow rate of 3 Lpm. A surface recombination velocity below 25 cm/s was obtained for the silicon oxide layer of 4 nm thickness. This ultrathin SiO_2 layer was employed for the fabrication of HIT solar cell structure instead of a-Si:H, (i) layer and the passivation and tunneling effects of the silicon oxide layer were exploited. The photocurrent was decreased with the increase of illumination intensity and SiO_2 thickness.

1. Introduction

The surface passivation effect is one of the most important characteristics in the fabrication of solar cells [1, 2]. The decrease in quality of surface passivation limits the efficiency of solar cell due to increase of surface recombination velocity (S_{eff}). An increase in surface recombination reduces the generation of electron hole pair (EHP). The quality of the silicon wafer is also a decisive factor to get high-efficiency solar cell. One of the typical features that decide the quality of a wafer is its diffusion length. The diffusion length of a wafer can be correlated with its diffusivity and surface passivation. The typical passivation layers used are SiO_2 and silicon nitride (SiN_x) thin films. The passivated emitter, rear locally diffused (PERL) cell and heterojunction with intrinsic thin layer (HIT) solar cell recorded an efficiency of 23% and 24.7%, respectively [1, 2]. The PERL cell utilized SiO_2 as the passivation layer whereas a-Si:H(i) is used as passivated layer in HIT solar cell to obtain an efficiency of over 20%. S. De Wolf et al. [3] indicated that a-Si:H layer is thermally unstable. However, SiO_2 will be an appropriate passivation layer for the solar cell fabrication due to its thermal stability and low interface defect density (D_{it}) [4]. The oxidized n-type silicon has a much better surface passivation properties than p-type silicon due to the small hall capture cross-section ($\sigma_n/\sigma_p \approx 1000$ at mid gap) [5] and optimized thermal oxide interface state densities of the order of 10^9 to 10^{10} $\text{cm}^{-2}\,\text{eV}^{-1}$ range [5, 6]. Two different mechanisms leading to good passivation are (i) the reduction of interface defect states and (ii) the field effect passivation, that is, the high reduction of one type of carrier by the incorporation of fixed charges Q_f in the passivation layer [7]. A reduction of interface state together with the field effect passivation is more effectively expected to attain for thermally grown SiO_2 layers [8, 9].

This thermal oxide growth could be achieved by two different methods. One is by the normal conventional furnace process (CFO) and the other is by the rapid thermal oxidation (RTO) process. The CFO process has

few disadvantages such as low throughput, high process cost, and high thermal budget. On the other hand RTO process is driven by the necessity to reduce the overall thermal budget associated with device fabrication and in particular to maintain the desired device electrical properties [10].

In this study, we used a thermal oxide process (RTO process) for the growth of the SiO_2 as a passivation layer for the HIT solar cell application and discussed SiO_2 layer's passivation property.

2. Experimental Method

2.1. Thermal Oxide Passivation Process. The n-type polished crystalline (100) silicon substrates having a resistivity of 2-3 Ω-cm were used for this study. The resistivity of the silicon substrate has a decisive effect on the growth rate of SiO_2. The substrates were cut into 20 cm^2 pieces and were ultrasonically cleaned in sequence by dipping in acetone, isopropyl alcohol, and deionized (DI) water for 10 minutes. The native oxide layer was removed by dipping the substrate in 2% HF for 2 minutes. Rapid thermal oxidation technique using infrared (IR) lamp was utilized to oxidize the silicon substrates. The oxygen flow rate and temperature were varied in the range of 1–8 Lpm and 500–950°C, respectively. Firstly, the chamber was filled with nitrogen gas. At the steady state temperature, only oxygen was passed through the chamber. Lifetime was measured by photoconductive decay (PCD, WCT-1200) model. We confirmed the surface passivation effect of SiO_2 layer and estimated the surface recombination velocity (SRV) using PCD. The thickness of the SiO_2 layer formed by RTO process was measured by Ellipsometry (VB-250, J. A. Woollam) system. The metal-oxide-semiconductor (MOS) structure was fabricated to measure the interface trap density (D_{it}). The D_{it} value of the MOS structure was calculated by *C-V* measurement (HP-4129A) at 1 MHz.

2.2. Heterojunction Fabrication Process. The HIT solar cell structure was fabricated after growing an ultrathin SiO_2 layer on the silicon substrate by the RTO process. A p-type hydrogenated amorphous silicon (a-Si:H(p)) layer was deposited as an emitter on the polished side of the n-type Czochralski (CZ) silicon substrate and n-type hydrogenated amorphous silicon (a-Si:H(n)) layer was deposited as back surface field (BSF) layer on the rear side of the n-type CZ wafer. The thickness of the SiO_2 layer was around 3 nm. The thickness of the a-Si:H(p^+) and a-Si:H(n^+) layers was kept fixed at 7 nm and 10 nm, respectively. The deposition of ITO was performed by magnetron sputtering using a metal mask that was directly placed on the a-Si:H(p) surface. The evaporation method was used to deposit Ag/Al electrodes (200 nm) on the ITO and rear side to enable a good ohmic contact. The reactive ion etching (RIE) was carried out using SF_6 gas on the top side for mesa-etching. Finally, the above sample was annealed in air, and the solar cell characteristics have been measured.

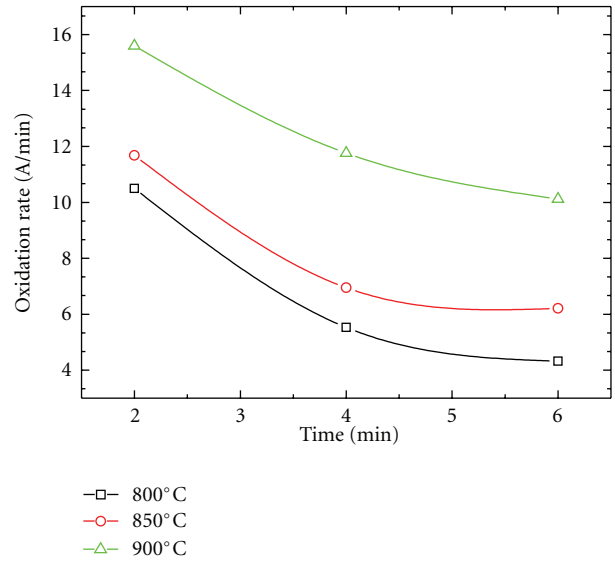

Figure 1: Oxidation rate of silicon substrate during rapid thermal annealing process at 800, 850, and 900°C with time.

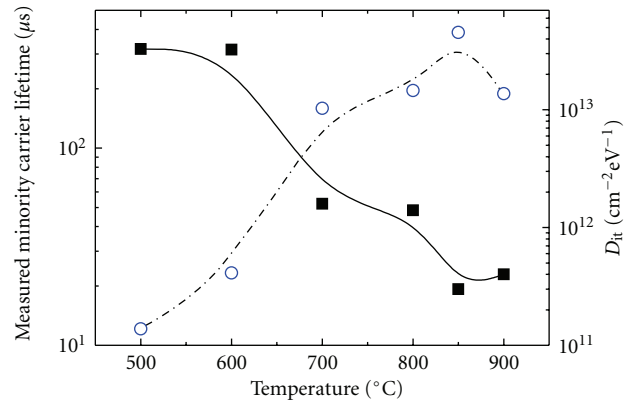

Figure 2: Variation of effective lifetime and interface trap density (D_{it}) as a function of rapid thermal annealing temperature.

3. Results and Discussion

Figure 1 depicts variations in the oxidation rate of silicon substrate during the rapid thermal annealing process at 800, 850, and 900°C as a function of time. The variation of the oxidation rate as a function of time can be explained by modifying the Deal-Grove model, which is accurate for very thin layer up to 1 nm, and proposed by Watanabe et al. [11]. Based on the Watanabe formulas, the thickness of the film as function of time can be expressed in the following form:

$$\frac{d}{dx_0}\left(\frac{dt}{dx_0}\right) = \frac{N_1}{D_0 C^*} - \frac{N_1}{2D_0^2 C^*}(A + 2x_0)\frac{dD_0}{dx_0}, \quad (1)$$

where the second term on the right side corresponds to the deviation from the linear kinetics of dt/dx_0. If $dD/dx_0 > 0$; that is, D_0 is decreased as x_0 decreases, the slope of dt/dx_0 decreases. In this case, the plot bends upward at the thin oxide region (short annealing time), as shown in our

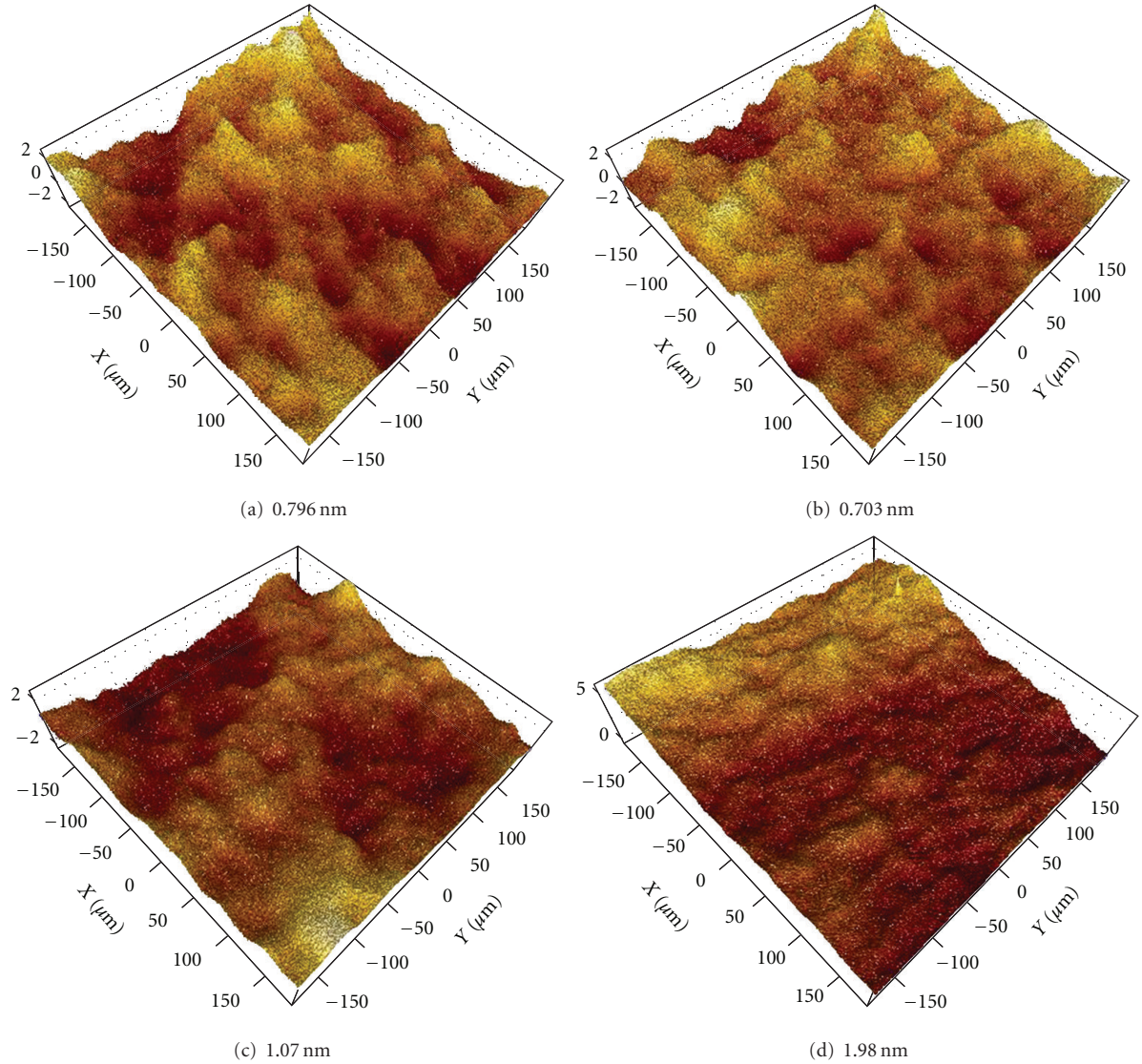

Figure 3: RMS as a function of rapid thermal annealing temperature: (a) 750, (b) 850, (c) 900, and (d) 950°C.

experiment results. Thus, it can be seen from the figure that the oxidation rate depends on the rapid thermal annealing temperature and shows a similar trend in the variation irrespective of RTO temperature. However, as the RTO temperature increased from 800 to 900°C, the SiO_2 layer formation rate was higher, as expected.

Figure 2 shows the variation in the effective lifetime and interface trap density (D_{it}) of the HIT solar cell as a function of RTA temperature. According to (1), an increase in effective life time would reduce the surface recombination velocity of the structure. When the thermal annealing temperature increased, the defect content of the surface may decrease that would reduce the surface recombination of carriers and result in an increase of effective carrier life time. The figure also shows that the effective lifetime increased when the temperature was increased from 500 to 850°C, maximum being at 850°C. As expected, the interface trap density (D_{it}) decreased with an increase of RTO annealing temperature, implying that the surface passivation quality is enhanced with an increase of temperature. The D_{it} gives a measure of the defects at the interface between Si substrate and SiO_2 layers. In order to explain the tendency of D_{it}, the surface roughness of the SiO_2/c-Si was estimated at different annealing temperatures, that is, 750, 850, 900 and 950°C, as shown in Figure 3. From Figure 3, we can deduce the average interface nanoroughness affects the interface condition (D_{it}). As the average interface nanoroughness gets bigger, however, the τ_{eff} decreased. It is also revealed that the lowest D_{it} as well as nanoroughness simultaneously can be observed. This is considered because the carriers are scattered by nanoroughness of the Si/SiO_2 interface [12]. Therefore it will become of more importance to improve the smoothness of Si/SiO_2 interface.

The illuminated current-voltage (I-V) characteristics of the device at different light intensity sources are shown in Figure 4 along with the dark I-V characteristics measured at

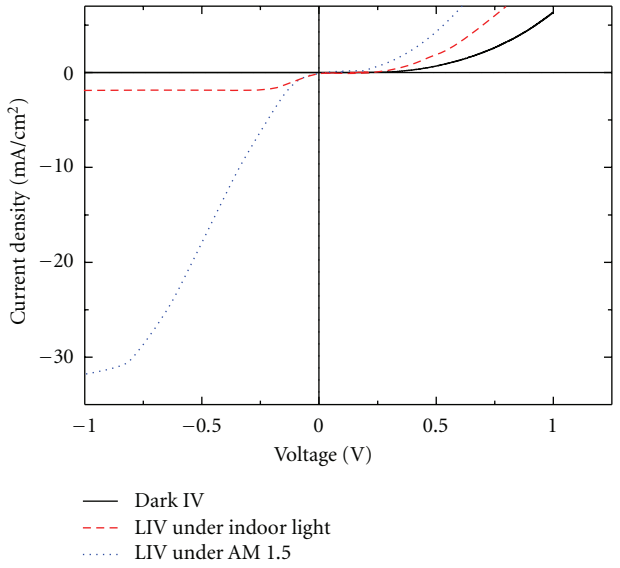

FIGURE 4: The illuminated current-voltage (I-V) characteristics of the device at different light intensity sources.

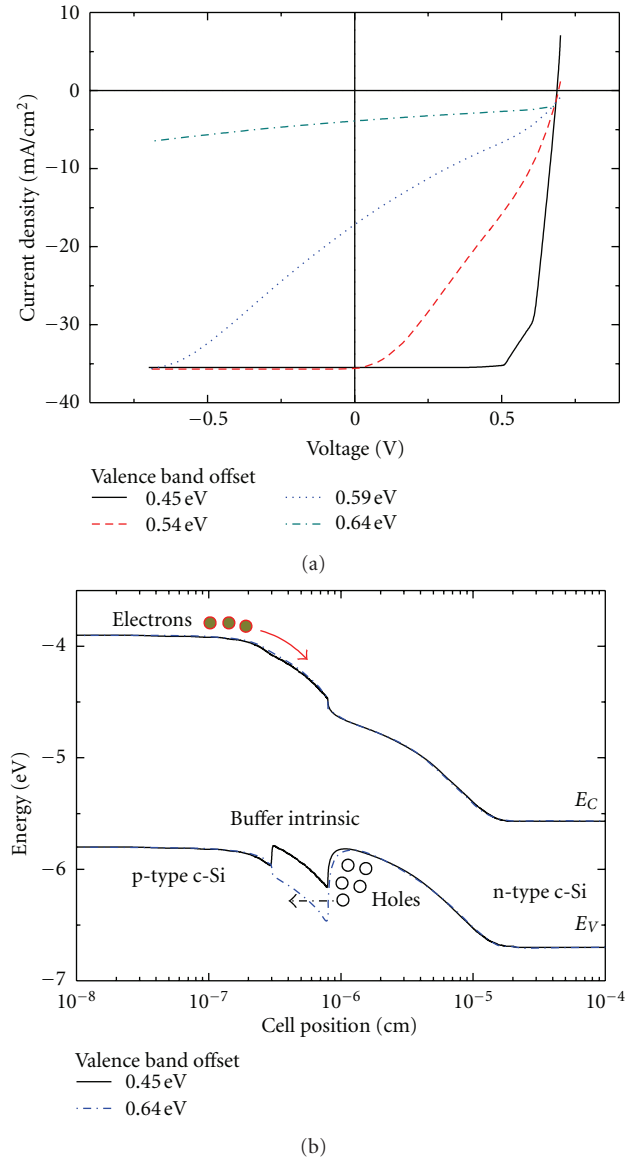

FIGURE 5: (a) Simulated I-V curve with different energy band gap of passivation layer, (b) schematic of the band diagram depend on energy band gap of passivation layer.

room temperature. It is observed from the figure that the illuminated I-V curve has been distorted (S-shaped) and the dark I-V curve retain in its original form. A change in light intensity results in changing of output current density, but does not change the shape of the photo I-V curve. We performed numerical simulation using AFORS-HET to determine the probable cause of the S-shaped I-V curve. The simulation results are shown in Figures 5(a) and 5(b). Figure 5(a) shows the change in illuminated I-V curve with increasing energy bandgap. When we increased the energy bandgap from 1.72 to 1.89 eV, the illuminated I-V shape changed toward our experimental results. Figure 5(b) shows the band diagram of the device having different valence band offset. From band diagram we may assume that higher bandgap of the buffer intrinsic oxide results in higher band offset, lowering electron affinity, and opposes the flow of the photocurrent in the device.

In order to remove the S-shaped curve in the I-V characteristics, both our simulation and van Cleef's experiment [13] suggested that (1) the energy band gap is either lower than 1.72 eV or (2) enhances the tunneling mechanism at the interface which mitigate the blocking of photo-generated free holes by a high valence band discontinuity. It is well known that SiO_2 is a wide-band-gap material (>4.0 eV) if it is grown by RTO method. Figure 6 shows the I-V characteristics of our device as a function of the intrinsic SiO_2 thickness in range of 1.0–3.4 nm. The S-shaped curve in I-V characteristics can be significantly reduced or even completely removed with the reduction of thickness. It is clear that the decrease thickness of the SiO_2 in the results in a narrow valence band spike. Then photogenerated holes are able to tunneling through the SiO_2 layer. Consequently a high accumulation of holes at the interface is prevented, and, also depletion region is prevented from spreading too much inside the emitter. At the same time, the SiO_2 layer's band gap is too high for the photoelectrons to cross the tunneling layer. When we apply wide-band-gap material to passivation layer in HIT solar cell structure, we should consider compromising condition between band gap and thickness.

4. Conclusion

The surface passivation is very important issue in amorphous and crystalline silicon solar cell applications as it highly influenced the performance of the device. Here we used ultrathin thermal passivation SiO_2 layer deposited by RTO system as a function of temperature and time for the fabrication of HIT solar cell. The high RTO annealing temperature can decrease the surface defects and reduce the

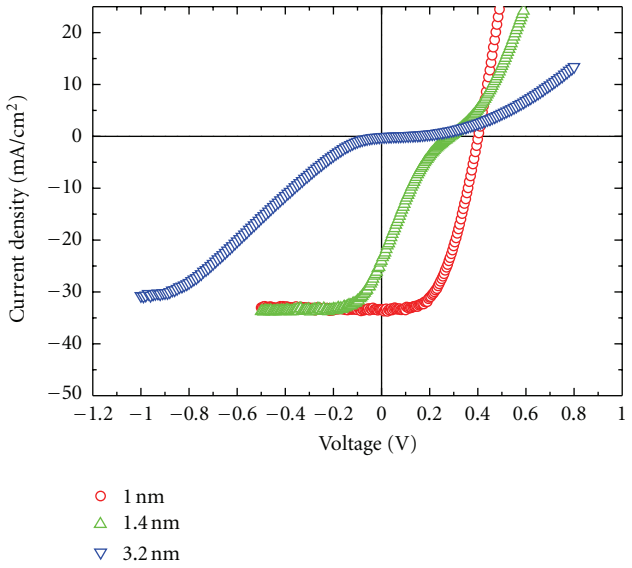

Figure 6: Variation of current density as a function of voltage of silicon oxide layer with thicknesses 1, 1.4, and 3.2 nm formed by rapid thermal annealing process.

surface recombination which caused an increase in effective life time. The SiO_2 layer deposited at a temperature of 850°C for 6 minutes gives the best values of S_{eff}, although the performance of our fabricated HIT solar cell using SiO_2 passivation layer is not better than the conventional HIT solar cell using a-Si:H(i) as a passivation layer. The bandgap is also a key factor to use SiO_2 as a passivation layer, which is yet to be tried to achieve for the upcoming experiments. The SiO_2 passivation layer can be employed in HIT solar cell by proper control of bandgap and tunnelling mechanism.

Acknowledgments

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References

[1] J. Zhao, A. Wang, and M. A. Green, "24.5% efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates," *Progress in Photovoltaics*, vol. 7, no. 6, pp. 471–474, 1999.

[2] T. Mishima, M. Taguchi, H. Sakata, and E. Maruyama, "Development status of high-efficiency HIT solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, no. 1, pp. 18–21, 2011.

[3] S. De Wolf and M. Kondo, "Boron-doped a-Si:Hc-Si interface passivation: degradation mechanism," *Applied Physics Letters*, vol. 91, no. 11, Article ID 112109, 3 pages, 2007.

[4] S. W. Glunz, "High-efficiency crystalline silicon solar cells," *Advances in Optoelectronics*, vol. 2007, Article ID 97370, pp. 1–15, 2007.

[5] A. G. Aberle, "Surface passivation of crystalline silicon solar cells: a review," *Progress in Photovoltaics*, vol. 8, no. 5, pp. 473–487, 2000.

[6] S. R. Wenham, J. Zhao, X. Dai, A. Wang, and M. A. Green, "Surface passivation in high efficiency silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 65, no. 1, pp. 377–384, 2001.

[7] A. G. Aberle, S. Glunz, and W. Warta, "Field effect passivation of high efficiency silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 29, no. 2, pp. 175–182, 1993.

[8] A. G. Aberle, S. W. Glunz, A. W. Stephens, and M. A. Green, "High-efficiency silicon solar cells: Si/SiO2 interface parameters and their impact on device performance," *Progress in Photovoltaics*, vol. 2, no. 4, pp. 265–273, 1994.

[9] W. D. Eades and R. M. Swanson, "Calculation of surface generation and recombination velocities at the Si-SiO2 interface," *Journal of Applied Physics*, vol. 58, no. 11, pp. 4267–4276, 1985.

[10] B. J. O'Sullivan, P. K. Hurley, C. Leveugle, and J. H. Das, "Si(100)-SiO_2 interface properties following rapid thermal processing," *Journal of Applied Physics*, vol. 89, no. 7, pp. 3811–3820, 2001.

[11] T. Watanabe, K. Tatsumura, and I. Ohdomari, "New linear-parabolic rate equation for thermal oxidation of silicon," *Physical Review Letters*, vol. 96, Article ID 196102, p. 4, 2006.

[12] S. De Wolf, G. Agostinelli, G. Beaucarne, and P. Vitanov, "Influence of stoichiometry of direct plasma-enhanced chemical vapor deposited SiN films and silicon substrate surface roughness on surface passivation," *Journal of Applied Physics*, vol. 97, no. 6, Article ID 063303, pp. 1–8, 2005.

[13] M. W. M. van Cleef, F. A. Rubinelli, R. Rizzoli, R. Pinghini, R. E. I. Schropp, and W. F. van der Weg, "Amorphous silicon carbide/crystalline silicon heterojunction solar cells: a comprehensive study of the photocarrier collection," *Japanese Journal of Applied Physics*, vol. 37, no. 7, pp. 3926–3932, 1998.