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Research Article

Improved Efficiency of Flexible Organic Light-Emitting Diodes by Insertion of Ultrathin SiO_2 Buffer Layers

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An ultrathin hole-injection buffer layer (HBL) using silicon dioxide (SiO_2) by electron beam evaporation in flexible organic light-emitting diode (FOLED) has been fabricated. While the current of the device at constant driving voltage decreases as increasing SiO_2 thickness. Compared to the different thicknesses of the buffer layer, the FOLED with the buffer layer of 4 nm showed the highest luminous efficiency. The atomic force microscopy (AFM) investigation of indium tin oxide (ITO)/SiO_2 topography reveals changes at the interface between SiO_2 and N,N′-bis-(1-naphthl)-diphenyl-1,1′-bipheny-4,4′-diamine (NPB), resulting in ultrathin SiO_2 layers being a clear advantage for a FOLED. However, the SiO_2 can be expected to be a good buffer layer material and thus enhance the emission performance of the FOLED.

1. Introduction

In the recent years, organic light-emitting diodes (OLED) have gained great interest in the last decade due to their potential application in efficient, large-area, and full-color displays [1–4], especially for flexible displays application [5–8]. The quantum efficiency, photons emitted per electron injected, is dependent upon the current balance between electrons and holes and therefore upon the charge injection rates at cathode and anode interfaces. Current balance is especially difficult to achieve in devices with only a single organic layer since there are no energy barriers to block carrier transit from electrode to electrode. It, therefore, becomes critical to achieve the best possible current balance by suitable choice of materials [9, 10]. The injection currents depend primarily on Schottky barrier heights at each electrode. Furthermore, corroborating evidence for the important injection rate using physical hole-injection buffer layer (HBL) deposited on the anode. Recently, few studies have reported that an ultrathin film of oxide is employed as an anode buffer layer in organic light-emitting devices to enhance the hole transport and power efficiency of OLED [11–13]. In other words, the buffer layer enhances most of the holes injected from the anode and improves the balance of the hole and electron injections. Although these studies can improve their efficiency, to accurately control the evaporation rate and the concentration of two or more materials, such as molybdenum oxide (MoO_3), zinc oxide (ZnO), and silicon dioxide (SiO_2), in the doping codeposition process is very difficult.

Among these materials, the cost of SiO_2 material is cheaper than that of the other two materials. However, if a thin insulating layer such as silicon dioxide (SiO_2) with a wide bandgap (8 eV, compared to 2.9 eV for 8-hydroxyquinoline aluminum (Alq_3)) is added between the indium tin oxide (ITO) anode and N,N′-bis-(1-naphthl)-diphenyl-1,1′-bipheny-4,4′-diamine (NPB) layer, the accumulation of holes can occur at the ITO/NPB interface; hence, the improvement

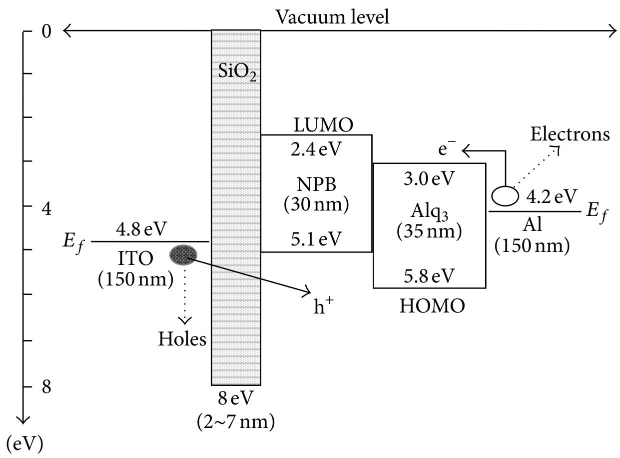


Figure 1: The schematic energy level diagram of ITO/SiO_2/NPB/Alq_3/Al.

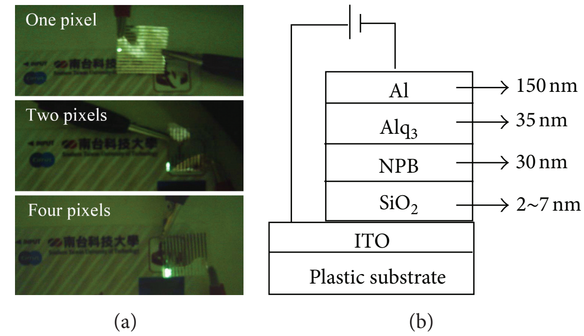


Figure 2: Photographs (a) of flexible organic light-emitting diode at an applied voltage of 6 V and schematic diagram of device configuration (b).

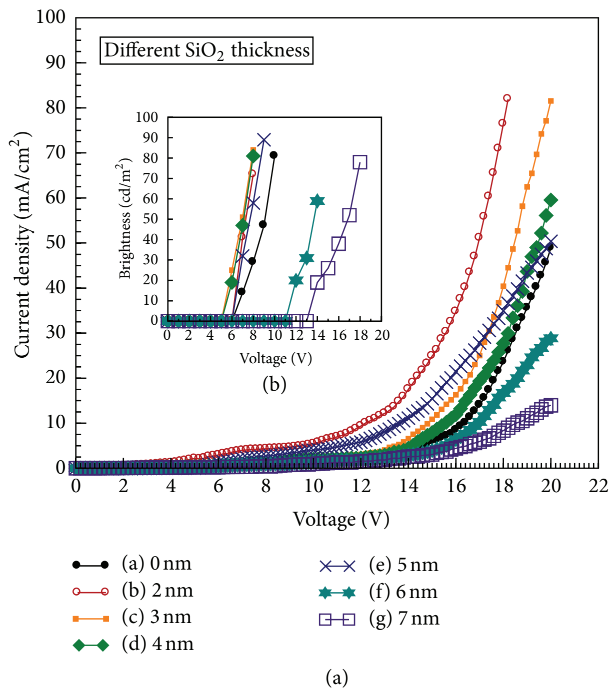


Figure 3: (a) J-V characteristics of the devices with different silicon dioxide thicknesses. (b) The inset shows the B-V characteristics of the devices.

is of current balance between the injected electrons and holes. The inserted buffer layer has not yet been studied. In this paper, a detailed investigation of an ultrathin SiO_2 layer as the HBL and the effect of SiO_2 on the device efficiency is presented.

2. Experimental

For the fabrication of flexible organic light-emitting diode (FOLED), the devices were performed on 150 nm thickness of indium tin oxide (ITO)-coated plastic substrate. The schematic energy level diagram of the FOLED with the SiO_2 layer inserted between ITO/NPB interface structures is shown in Figure 1. The sheet resistance of ITO was obtained at 50 Ω/sq. The plastic substrate used in this study is a transparent polymer named ARTON (ARTON F, JSR Co., Ltd., Japan). The ITO film is streaked with the photolithography processing via etching and is as an anode electrode. The device configuration was adopted as shown in Figure 2. The multilayer structure consists of an ITO-coated plastic substrate, ultrathin SiO_2 as an HBL, NPB as a hole-transporting layer (HTL), Alq_3 as an electron-transporting layer (ETL), and aluminum (Al) cathode electrode manufactured by shadow mask. The thickness of ITO, NPB, Alq_3, and Al was performed at 150, 30, 35, and 150 nm, respectively. The emitting area of devices is 2.25 mm^2. After the previously mentioned multilayer structure, the SiO_2 layer is fabricated by using the electron beam deposition (EBD) system. The evaporation onto the ITO-covered plastic substrate is performed in a high vacuum system with a base pressure of 1.0×10^{-6} torr. The Al was deposited by EBD system at rates of 1 nm/sec. The brightness is measured by spectrophotometer (Photo Research, PR655 SpectraScan, USA). The characterization was carried out by using the power source (Keithley Source Meter 2400, USA). The present study also presents a complementary study of the topography of the surfaces by atomic force microscopy (AFM, Burleigh, METRIS-3345, USA).

3. Results and Discussion

Figure 3(a) shows typical current density versus applied voltage (J-V) characteristics of the studied devices fabricated with different thicknesses of SiO_2 (0, 2, 3, 4, 5, 6, and 7 nm). The current density of the devices is almost zero under negative voltage. As expected, the current density decreases as the buffer layer thickness increases when the buffer layer of SiO_2 is larger than 5 nm at a constant applied voltage of 14 V. On the other hand, there is a tendency that current density increases with the decrease of the thickness of the buffer layer (2~4 nm). This suggests that the buffer layer is as a block layer and has an effect of blocking the hole in movement, leading to more balance. In other words, this barrier impedes hole injection from ITO, preventing the accumulation of excess holes in the luminance layer, thus increasing the probability of e-h^+ pair combination.

It is known that holes are the major charge carrier in FOLED, and luminous efficiency strongly depends on charge balance. Luminous intensity therefore increases with the increase of barrier height and with the thickness of the buffer layer (2~4 nm) when the applied voltage is less than 8 V. It shows that the bias voltage to obtain the same current density of 20 mA/cm^2 is obviously lowered for the FOLED with 2 nm SiO_2 buffer layer compared with the devices without SiO_2. Furthermore, the light onset voltage ($V_{L\text{-on}}$; defined as the voltage required to drive a luminance of 10 cd/m^2) of the device with SiO_2 of 4 nm is as low as 5.2 V, as shown in the inset of Figure 3(b). In other words, the $V_{L\text{-on}}$ in Figure 3(b) is estimated to be 7.1, 6.2, 5.1, 5.2, and 6.5 V for devices with buffer layer in 0 nm, 2 nm, 3 nm, 4 nm, and 5 nm, respectively. Thus, the $V_{L\text{-on}}$ of 2 nm, 3 nm, 4 nm, and 5 nm is to be lower than that of the device without buffer layer. However, there is a tendency that the $V_{L\text{-on}}$ increases with the increase of oxide thickness (2~7 nm) because a larger voltage is dropped across the oxide [14]. When the oxide layer is more than 5 nm, the effective barrier is as (1) [15]

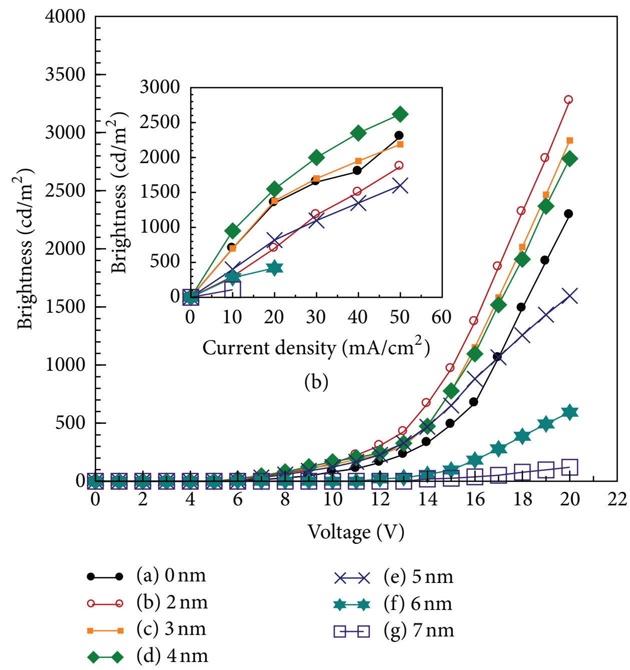
$$\Phi_B' = \Phi_B - \left(q\frac{|E_S|}{4\pi\varepsilon\varepsilon_o}\right)^{1/2} - \alpha|E_S|, \tag{1}$$

$$D_m = \left[\frac{q}{16\pi\varepsilon_o E}\right]^{1/2}, \tag{2}$$

$$\Delta\Phi = \left[\frac{qE}{4\pi\varepsilon_o}\right]^{1/2}, \tag{3}$$

where E_S is the NPB surface field and Φ_B is the potential barrier height when $E_S = 0$. The image force exerted by ITO proximity and the thermally assisted tunneling through the barrier lowers the effective barrier height. Equations (2) and (3) show the relationship between $\Delta\Phi$ and D_m, where D_m is the distance from the ITO. From the previous equation and viewpoints, there is an image force at smaller D_m which results from increasing oxide thickness and lowers considerably the barrier. In other words, the barrier height is inversely proportional to oxide thickness. With lowered barrier, there follows an excess of hole injection and accumulation. However, improved hole/electron injection balance is a consequence one may expect from the inclusion of SiO_2 ultrathin film as HBL. Besides, the electrons possess much lower mobility than holes in organic materials. This gives rise to an accumulation of excess holes at SiO_2-NPB boundary. The electron-hole pair combination is decreased, so the luminous efficiency is decreased.

Figure 4(a) shows the brightness versus applied voltage (*B-V*) characteristics of the FOLED with the SiO_2 buffer layer. In contrast with the value of only 2300 cd/m^2 without SiO_2 buffer layer, an impressive brightness of more than 3300 cd/m^2 was measured when the SiO_2 thickness was 2 nm at 20 V. Similarly, the luminous efficiency of the FOLED was increased due to the introduction of the thin SiO_2 layer (Figure 5). Figure 4(b) shows the brightness versus current



(a)

Figure 4: (a) *B-V* characteristics for the devices with different SiO_2 buffer layer thicknesses. (b) The inset shows the *B-J* characteristics of the devices.

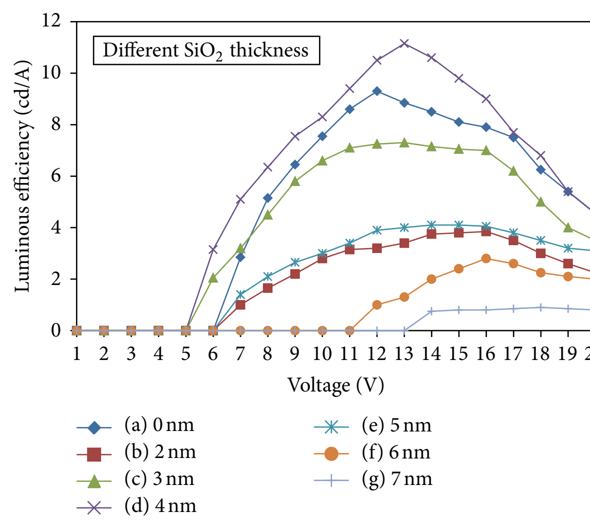


Figure 5: Luminous efficiency versus applied voltage curves of the devices with different buffer layer thicknesses.

density (*B-J*) on the SiO_2 thickness for the devices. At a given constant current density of 20 mA/cm^2, the device with buffer layer of 4 nm displayed the highest luminance of 1550 cd/m^2 among the seven samples which corresponded to a luminous efficiency of 7.6 cd/A. In contrast, the device without the SiO_2 buffer layer only shows the luminous efficiency of 6.4 cd/A at the current density of 20 mA/cm^2. Table 1 showed the luminance and efficiency characteristics for the devices with different thicknesses of SiO_2 at the

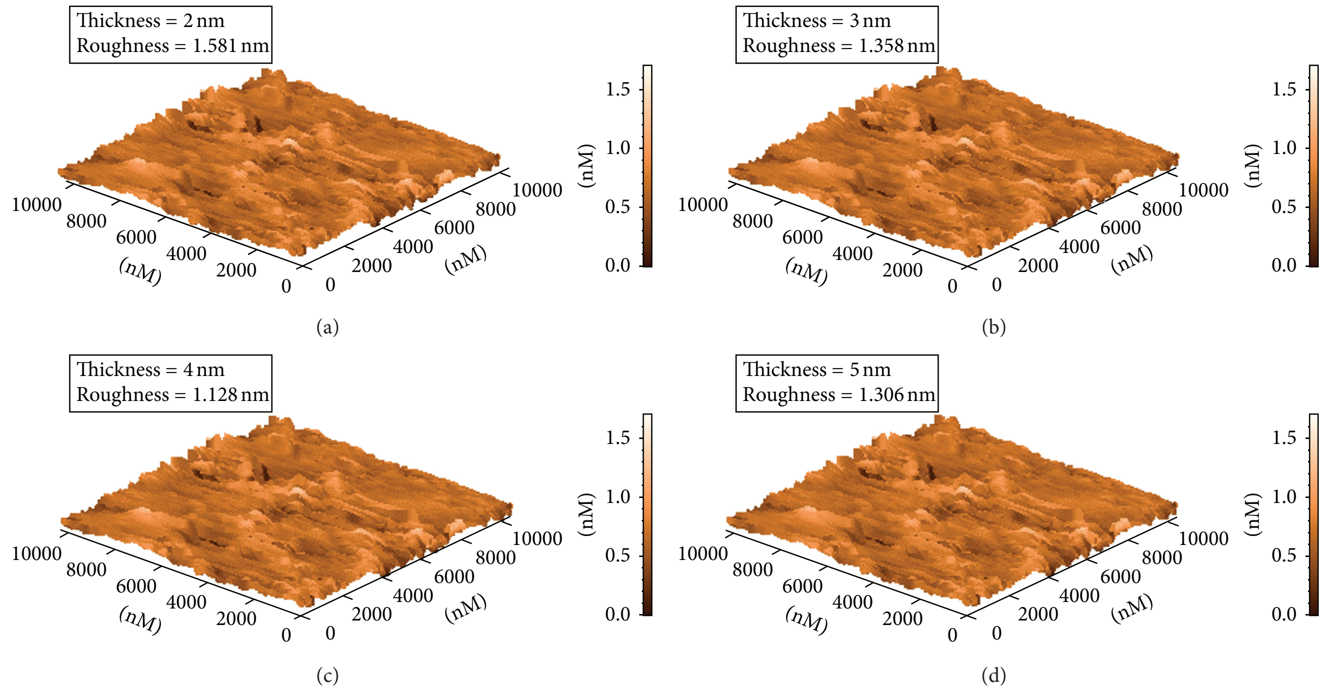


Figure 6: Images of atomic force microscopy of the ITO surface after depositing (a) 2, (b) 3, (c) 4, and (d) 5 nm SiO_2 buffer layers.

Table 1: Luminance and efficiency characteristics for the devices with different SiO_2 buffer layer thicknesses at the current density of 20 mA/cm^2.

SiO_2 thickness (nm)	Luminance (cd/m^2)	Voltage (V)	Luminous efficiency (cd/A)
0	1310	17.8	6.4
2	700	14.2	3.8
3	1380	16.8	6.5
4	1550	17.1	7.6
5	820	15.8	4.1
6	420	18.2	2.2
7	78	18	0.72

current density of 20 mA/cm^2. The voltages are obtained from Figure 3(a) at a constant current density of 20 mA/cm^2. Furthermore, the luminance and the luminous efficiency are got and corresponded from above various voltages via Figures 4(a) and 5, respectively. And then it is obvious that the efficiency of the device with buffer layer of 4 nm is better than that of the one without buffer layer. The brightness and efficiency of electroluminescent (EL) devices increased with the thickness of the SiO_2 buffer layer, but those drop after the maximum brightness and efficiency of EL devices, which can be attributed to excessively blocking the hole by the thick buffer layer. However, a good EL device should possess not only the high brightness but also the high luminous efficiency.

Shown in Figure 5 is luminous efficiency versus applied voltage curves for seven different devices, derived from the data shown in Figure 4. There is an optimization thickness of SiO_2 (4 nm) for the luminous efficiency of the devices. At a given constant voltage of 13 V, obviously the device with the 4 nm thick buffer layer was the most efficient one. In contrast, the device without the SiO_2 buffer only showed a luminous efficiency of 8.8 cd/A at the voltage of 13 V. An increase in the thickness of the SiO_2 buffer beyond 4 nm resulted in a gradual decrease in brightness and efficiency. No EL emission could be findable when the thickness of the layer exceeded 8 nm. Device performance was improved by the use of a buffer layer consisting of SiO_2. Although the exact role of the SiO_2 buffer layer in the hole-injecting transporting process is not completely clear, the enhancements in brightness and efficiency of the devices may tentatively be attributed to an improved balance of the hole and electron injections, which results in enhancements of carrier recombination efficiency. In addition, some groups believe that the deposition of an ultrathin oxide layer prior to the organic material deposition may smooth the interface and lead to a more homogeneous adhesion of the HBL to the anode [16–19].

The topography of SiO_2 on ITO was acquired *ex situ* using atomic force microscopy (AFM). Figures 6(a)–6(d) show the topographical images that present the surface root mean square (RMS) roughness for ITO and surfaces obtained after depositing SiO_2 of 2, 3, 4, 5 nm on ITO. The RMS roughness is 1.581, 1.358, 1.128, and 1.306 nm, respectively. That reveals that ITO has a relatively smooth surface. In the 2 and 3 nm thickness, the surface morphologies are island structure and small quantity of spikes; a few nanometers in height on bare ITO surfaces indicate that the grains coalesce and fill in the channel between the grain and the poor surface uniformity. In addition, there is an optimization thickness of SiO_2 (4 nm) for the low RMS roughness of surface; the structure of island

and spikes have fallen away little by little. In fact, the smooth uniformity of film surface for improving interface contact of the ultrathin SiO_2 layer with organic layer is important for the injection and transmission properties of carrier. Therefore, carrier can be easy to inject through from ITO to organic mediums when the device is properly biased.

4. Conclusions

In summary, the devices with the insertion of an ultrathin SiO_2 buffer layer between ITO and NPB showed enhanced hole-injection efficiency, higher EL efficiency, and operational stability that may be attributed to an improved current balance of the hole and electron injections, resulting mainly from the blocking of the injected holes by the buffer layer. In other words, this buffer layer improves FOLED efficiency without modifying the electrode work function or requiring additional organic layers. Various techniques, including physical and electrical characterizations, show that a smoother SiO_2 (4 nm)/NPB interface versus ultrathin SiO_2 layers is a clear advantage for a FOLED. However, the buffer layer can be to control the emission performance of the FOLED, offering further promise for innovation optoelectronic application.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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