Research Article

Single-Crystalline Silicon Solar Cell with Selective Emitter Formed by Screen Printing and Chemical Etching Method: A Feasibility Study

Yen-Po Chen, Ching-Tao Li, and Likarn Wang

Institute of Photonics Technologies, National Tsing Hua University, Hsinchu 300, Taiwan

Correspondence should be addressed to Likarn Wang; lkwang@ee.nthu.edu.tw

Received 20 January 2013; Accepted 20 October 2013

Academic Editor: Junsin Yi

Copyright © 2013 Yen-Po Chen et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

A new method for fabricating crystalline silicon solar cells with selective emitters is presented. In this method, shallow trenches corresponding to metal contact area are first formed by screen printing and chemical etching, followed by heavy doping over the whole front surface of the silicon wafer. After a polymer mask is pasted by aligned screen-printing to cover the shallow trenches, the silicon wafer is etched such that the heavy doping remains at the shallow trench area, while other areas become lightly doped. With the presented method, two screening printing steps are required for obtaining a selective emitter structure on a solar wafer. Compared with existing etch-back methods, the presented one is believed to be able to easily conform with present industrial process. Experimental results show that optical responses at the short and long wavelengths were both improved by applying the proposed selective emitter technique to fabricate solar cells with an a-Si:H film deposited on the back surface. The selective emitter cell with a-Si:H back surface deposition had improvements of 1.66 mA/cm² and 1.23% absolute in J_{sc} and conversion efficiency, respectively, compared to the reference cell that had a homogeneous emitter and no a-Si:H on the back surface.

1. Introduction

In the field of silicon wafer based solar cells, selective emitter structures are attracting attention to a great extent because of enhanced light-to-electricity conversion, especially at the short-wavelength range. The enhancement of light-to-electricity conversion results from the suppressed carrier recombination due to lowered concentration of dopant impurity at the illuminated area as well as the reduced contact resistance due to the high dopant concentration at the contact-semiconductor interface. In principle, the suppressed carrier recombination leads to increases in both the open-circuit voltage and short-circuit current, while the reduced contact resistance improves the fill factor.

Selective emitter is not a new concept. It originates during the development of work record silicon solar cells [1]. Various studies have been carried out [2–15] and notable efficiencies of cells with selective emitters utilizing industrial compatible processes have been reported [11, 13]. An industrial selective emitter processing sequence may involve the coating of

selected regions of the front of a p-type silicon substrate with a phosphorus-containing paste via screen printing [3]. At high temperature, the paste is used as a source for direct-diffusion and gas-phase outdiffusion into the substrate. Thus, the region covered with the coated layer becomes a heavily doped region by direct diffusion and the other region becomes a lightly doped region through gas-phase outdiffusion. Thus, the heavily doped region and the lightly doped region are formed simultaneously. Yet, precise control of uniform diffusion is required for obtaining target doping concentrations. An alternative process of using doped silicon ink for selective emitter formation developed by Innovalight has proved to be viable in a mass production test [4].

Another industrial selective emitter processing sequence may involve lightly doping the entire front surface of a p-type substrate with phosphorus followed by the standard antireflection application process and completed by screen printing a silver paste containing phosphorus through the front contacts [7, 8]. During the firing process, a metal front contact is formed while the phosphorus diffuses into the front surface

to form heavily doped regions in the contact regions. The advantage is that this method is compatible with common mass production technique of using silver paste to form the front contact. However, silver would diffuse into the substrate faster in the presence of phosphorus worsening the leakage current.

A third selective emitter approach will be the use of etch-back method, whereby the entire front surface of a p-type wafer will be heavily doped [10, 12, 13] followed by a masking step to mask selective regions from subsequent etch-back while the rest of the front is etched resulting in a lightly doped surface. An etch-back technology developed by Schmid's group has been recently commercialized by using an inkjet-printed wax mask for selective emitter formation [12]. The advantage of etch-back methods lies in the use of one diffusion step.

The fourth approach is to cover the front surface of a wafer with a patterned masking layer of silicon dioxide or silicon nitride through PECVD before doping [2, 5, 11]. Then, a dopant is doped into the substrate through high-temperature diffusion to form a heavily doped region and a lightly doped region at one time. The disadvantage of this method is the requirement for a mask layer, which is usually coated by a high-priced facility.

A widely used approach in the industry to date is the use of laser [14, 15] to selectively diffuse phosphorus into the substrate surface such as that used in mass produced Pluto solar cells [16]. The metal contact is then formed via a self-aligning plating process. The advantage of this technique is the avoidance of precise alignment. However, the plated metal requires a different interconnection method, not conventional used in the industry.

Despite the limitation of selective emitter in its contribution to boosting performance of commercial solar modules due to the absorption of short wavelength light by the standard EVA encapsulation material, it is still imperative to consider the selective emitter technology as new photovoltaic module encapsulation material emerges such as polydimethylsiloxane (PDMS) silicone. This appears to have better moisture proof and optical transmission properties than EVA in particular in the 300 to 500 nm wavelength range [17, 18].

In this paper, we present an alternative to the present selective emitter formation methods. In the presented method, an as-doped textured silicon substrate is first processed to obtain multiple shallow trenches which correspond to the front metal contact area on the front surface. The substrate is then doped in a high-temperature diffusion furnace to obtain a heavily doped layer with an opposite electric type to the substrate. Then the shallow trench area is covered with an acid-resistant mask layer, while the other area is not. An etch-back method with acid etching is then applied to obtain a selective emitter structure over the front surface. That is, the unmasked area becomes lightly doped, while a high dopant concentration remains at the trench area. The presented method differs from Schmid's etch-back method and any other existing etch-back method in two points. First, shallow trenches are obtained and then heavy doping is applied in the presented method, while heavy doping is

FIGURE 1: Fabrication steps for 3 groups of samples in this study.

applied first and then followed by an etch-back in Schmid's and other methods. Secondly, there are shallow trenches with a depth of several μm or more for metal contacts in the presented selective emitter structure, while no trenches are dug by using Schmid's and other methods.

2. Fabrication Method

2.1. Preparation of Reference Samples. The main steps for fabricating the selective emitter solar cells in the presented method are depicted in Figure 1. In the fabrication, $125 \times 125 \text{ mm}^2$ pseudosquare solar-grade (100) p-type Cz silicon wafers with a thickness of $\sim 180 \mu\text{m}$ and a resistivity of 1 to $3 \Omega \text{ cm}$ were cleaned through an SC1 cleaning procedure followed by a double-side alkaline texturization and were cut into pieces of $30 \times 30 \text{ mm}^2$ dimensions afterwards. These smaller pieces, named as-textured wafers here, were divided into three groups. As-textured wafers of group 1 followed a standard cell-fabrication procedure in our lab. This standard procedure contains the steps of phosphorus doping on the front side, phosphorous glass removal, deposition of anti-reflection coating (ARC) on the front side, metallization on both sides, cofiring to obtain an ohmic contact on the front surface and back surface field on the rear side, and edge isolation. This group was considered as a reference in this study. The front-side contact was screen printed with silver paste to form a finger-grid pattern with a single central busbar, while the rear side contact was screen printed with aluminum paste all over the back surface. The phosphorus doping was performed in a quartz-tube furnace in nitrogen ambient. For the reference samples, phosphorus pentoxide

wafers were used as a dopant source at the temperature of 880°C to obtain a sheet resistance of $\sim 55 \Omega/\square$ (measured by a four-point probe method). The ARC was SiNx deposited by PECVD at 300°C and has a thickness of 103 nm for obtaining the lowest average optical reflectivity. The cofiring was performed by using a high-temperature oven following these steps: (1) elevating the temperature up to 830°C; (2) slightly opening the oven door and putting the sample toward inside slowly; (3) closing the oven door and maintain at 800°C for 20 seconds; and (4) slightly opening the oven door and moving out the sample slowly from the hot zone. These steps were manually controlled in precise time mode to ensure that all samples experience cofiring under an identical condition. The cofiring temperature was increased from the room temperature up to an almost constant temperature at 800°C during a time period of 15 seconds, maintained at 800°C for 20 seconds and then decreased to the room temperature again during a 20-second time period.

The second group of as-textured wafers was also processed in the same fabrication procedure as mentioned above, except that there was a thin layer of hydrogenated amorphous silicon (denoted as a-Si:H) deposited on the rear side before metallization. This group (i.e., group 2) is denoted as a-Si:H deposited samples here. The a-Si:H layer was grown by PECVD at 285°C and had a thickness of 5 nm. The a-Si:H layer was supposed to contain many Si-H bonds as deposited, whereas a part of these bonds might break during the cofiring step resulting in hydrogen leakage. It is noted that group 2 was also used as a reference for samples of group 3 that have a selective emitter formed by the presented method. As-textured wafers of group 3 were processed following the selective emitter formation method presented below.

2.2. Selective Emitter Formation. As-textured wafers of group 3 were processed following the steps shown in Figure 2, where step (a) shows an as-textured wafer. The as-textured wafer was masked at its front surface with a patterned acid-resistant masking layer by screen printing (step (b)). A masking layer was also screen printed all over the back side of the wafer. The masking layer was a resin-based material, containing a certain proprietary binding components to resist chemical etching. The wafer was then dipped in an acid etching solution mixed with HF, HNO₃, and deionized water (step (c)). The regions covered by the masking layer on both sides of the wafer were protected against the chemical, while the regions not covered by the masking layer on the front side of the wafer were etched to a certain depth inside the wafer. The Multiple shallow trenches were thus formed at the etched regions. These shallow trench areas were prepared to be contact formation regions. After the formation of the trenches, the masking layer was removed by dipping the wafer in an ultrasonic cleaner with acetone as a solvent. Then the wafer was heavily doped to form an n⁺⁺ layer all over the front surface, as shown in step (d). A sheet resistance of $\sim 28 \Omega/\square$ was obtained at this step. Curve A of Figure 3 shows concentration-depth relation of the phosphorus doping, measured by SIMS. As can be seen from this figure, there exists a very high concentration at the front surface, leading to an expectable low contact

resistance. For regions between contacts, a part of silicon was removed, in an etch-back process, to a certain depth by again chemical etching and this resulted in a sheet resistance of $110 \Omega/\square$. In the etching-back process, an acid-resistant mask with the same type of resin-based material used for trench formation was screen printed onto the shallow trenches only, as shown in step (e), followed by a chemical etching. The chemical etching solution for this etching-back was a mixed HF/HNO₃/CH₃COOH solution of the ratio 1 : 40 : 200. Curve B of Figure 3 shows the concentration distribution inside the wafer after etching. After removing the masking layer with acetone in an ultrasonic cleaner, we obtained a selective emitter structure as shown in step (f) of Figure 2. Then, a silicon nitride ARC coating was deposited over the front surface using PECVD (see step (g), Figure 2), followed by a metallization process to obtain front contacts in the shallow trenches and a rear contact. Silver paste was screen printed into the shallow trenches in good alignment (see step (h), Figure 2), while the rear side of the wafer was screen printed with aluminum paste over the whole rear surface. In this study, the shallow trenches were 300 μm wide for fingers and 2 mm wide for the central busbar, while the front contact lines were 180 μm wide for fingers and 1.8 mm wide for the central busbar, as shown in Figure 4(d). The widths of the heavily doped areas are 2.2 mm for the busbar and 360 μm for the fingers. Cross-sectional SEM views for a 2 μm deep trench and a 15 μm deep trench both filled with silver paste are, respectively, shown in Figures 4(a) and 4(b), while a prospective view for the 15 μm deep trench is shown in Figure 4(c).

A part of these selective emitter structured wafers was processed by PECVD deposition to form a 5 nm-thick a-Si:H layer on the rear side before metallization (see step (h), Figure 2). Another part of these selective emitter structured wafers was not processed by PECVD deposition of a-Si:H for comparison. A cofiring step was afterwards applied to obtain an ohmic contact on the front and a BSF (as indicated in Figure 5) on the rear side.

2.3. Some Concerns. The presented etch-back method inevitably needs one additional alignment step for metal contact formation compared to self-aligning methods used for Pluto and buried contact cells. An alignment in printing usually needs a good enough visual image contrast. In our case, the trenched region is light blue on the dark blue background, after ARC is deposited. This visual contrast is good enough for printing when using high-resolution cameras. The advantage of the proposed method lies in the use of one diffusion step for selective emitter formation.

Another concern is on the surface reflectivity when the above etching is applied to remove high-density dopant. Original surface morphology may be changed and this may increase the optical reflectivity due to too much possible etching on the pyramids formed in the texturization process. To clarify this concern, we used the same etching condition to etch a phosphorus-doped textured wafer without forming trenches upon for 2, 4, and 12 minutes and compared the optical reflectivity with an as-textured wafer. Figure 6(a)

FIGURE 2: Fabrication steps for selective emitter solar cells in this study.

shows the measured optical reflectivities for the samples that were etched and not etched over the wavelength span from 400 nm to 1000 nm. The inset in this figure shows the difference in greater detail over the 700 to 800 nm span. It can be seen that the difference in optical reflectivity between any two samples is slight. In particular, when the sample is etched for only two minutes, which is the case for our etching back process, the increase in optical reflectivity is only $\sim 0.05\%$. After being deposited with an ARC layer, this sample shows no difference in optical reflectivity (as shown in Figure 6(b)) from the sample without etching, indicating that the above etching-back step for forming lightly doped regions is of no harm to the surface morphology as well as the optical reflectivity.

3. Experimental Results

3.1. Comparison between Homogeneous Emitter and Trenched Selective Emitter Cells. Table 1 shows the resultant sheet resistances of the lightly doped emitter and the corresponding solar cell parameters measured under the standard testing condition (i.e., AM 1.5 at 25°C) for 5 sets of selective emitter solar cells with different etching-back time periods (using Oriel/Newport SOL 3A solar simulator and Keithley 400 source meter). As the sheet resistance of the lightly doped emitter was increased from 56 to $110\ \Omega/\square$ (with the etching time period varying from 64 to 120 sec), J_{sc} increased from $35.42\ \text{mA}/\text{cm}^2$ to the maximum $36.9\ \text{mA}/\text{cm}^2$ accompanied by a slight increase in V_{oc} . As the sheet resistance was

FIGURE 3: Concentration-depth relation of the phosphorus doping, measured by SIMS, for shallow trench area (curve A) and region between contacts (curve B).

TABLE 1: Resultant sheet resistances and light-to-electricity parameters for five sets of selective emitter cells after applying different etching-back time periods.

Etching time (sec)	Sheet resistance ($\Omega/\square$)	J_{sc} (mA/cm ²)	V_{oc} (mV)	F.F. (%)	η (%)
140	159 $\pm$ 23	34.30	572.8	71.08	13.9
120	110 $\pm$ 10	36.90	589.3	77.53	16.9
100	82 $\pm$ 9	36.59	589.0	77.10	16.6
80	68 $\pm$ 5	35.90	588.8	76.67	16.2
64	56 $\pm$ 5	35.42	589.0	76.63	16.0

increased to 159 $\Omega/\square$, the built-in field at p-n junction was greatly weakened and resulted in reduced J_{sc} and V_{oc} . That also caused a reduced fill factor (F.F.) because of an increase in the emitter resistance. The best conversion efficiency η achieved among these sets of selective emitter cells was 16.9%. Two-minute time period was chosen for etching-back in forming the lightly doped region throughout this study.

The conversion efficiencies of reference cells (i.e., the cells with a homogeneous junction), selective emitter cells, and homogeneous-junction cells with 5 nm thick a-Si:H on the back surface are listed in Table 2, together with their electrical parameters. Here it is noted that the performance of selective emitter cells with a 5 nm a-Si:H film on the rear side is also shown in the table (the last row). It can be seen that the deposition of an a-Si:H layer on the rear side increased J_{sc} and V_{oc} with respect to the reference cells. A conversion efficiency of 16.2% for this type of cells was obtained. The selective emitter cell had a better J_{sc} and F.F. but a worse V_{oc} than the a-Si:H deposited cell. It is known that the selective emitter technique enhances the UV-to-visible optical response, while a-Si:H deposition improves the longer wavelength response. Our measurements of external quantum efficiency (EQE) for the three kinds of cells mentioned above confirm these characteristics. Figure 7 shows the measured EQE versus optical wavelength.

TABLE 2: Electrical parameters and conversion efficiencies measured for a reference cell (Ref.), a selective emitter cell (S.E.), a back-surface a-Si:H deposited cell (a-Si:H), and a selective-emitter cell with back-surface a-Si:H deposition (S.E. + a-Si:H).

	J_{sc} (mA/cm ²)	V_{oc} (mV)	F.F. (%)	η (%)
Ref.	35.38	589.1	76.54	16.0
S.E.	36.90	589.3	77.53	16.9
a-Si:H	35.42	602.1	76.13	16.2
S.E. + a-Si:H	37.04	602.3	77.23	17.23

It should be noted that the depths of the trenches was not controlled and ranged from 2 to 15 μm in this study and that a small variation of J_{sc} among the group was observed. A deeper trench resulted in slightly larger J_{sc} for most selective emitter cells in this study. The best efficiency 16.9% reported here was derived by the type of cells with a trench depth of $\sim 15 \mu\text{m}$. Compared with these cells, the conversion efficiency of the cell with 2 μm deep trenches was only reduced by 0.1–0.2% absolute. It is worth noting that the trenched selective emitter cell, for deep trench cases, has basically a buried contact structure with screen printed metal contact. However, it is not easy to form trenches as narrow as several tens of microns by wet etching, as in the laser drilling process for conventional buried contact structures. We believe at this moment that the cells with trenches of 2 μm depth can be considered to have a conversion efficiency essentially equivalent to a selective emitter structure without trenches as studied by other techniques. A future work may be focused on the effect of deeper trenches formed by the presented method and on the exploration of performance upgrade by narrow trenches achievable with a wet etching method.

A selective emitter solar cell with a-Si:H deposited on the back surface is, without a doubt, a good choice for improving the optical response at both shorter and longer wavelengths and accordingly J_{sc} , compared to the reference cell. The dashed curve in Figure 7 shows the spectral EQE for the selective emitter cell with back surface a-Si:H deposition. As shown in the last row of Table 2, the selective emitter cell with a-Si:H back surface deposition had an improved J_{sc} of 37.04 mA/cm² that was 1.66 mA/cm² higher compared to the reference cell. V_{oc} of the cell was about the same as that of the a-Si:H deposited cell, being 602.3 V, while F.F. was enhanced to 77.23%, which was higher than that of the reference cell owing to a reduced contact resistance. The conversion efficiency of the selective emitter cell with a-Si:H back surface deposition was accordingly increased to 17.23%. This efficiency is still much lower than those obtained by Pluto and Schmid's technologies. This low efficiency may be attributed to two reasons: the possible contamination in the process and the imperfect sintering in the cofiring step. The former is indicated by the low value of V_{oc} , which may result from a contaminated wafer surface through the cofiring process. The imperfect sintering caused a lower fill factor, which could be expectable as an unprofessional cofiring process was used in the study. This efficiency achieved here is by no means high enough for attracting industry's attention.

FIGURE 4: Cross-sectional SEM views for (a) a $2\mu\text{m}$ deep trench and (b) a $15\mu\text{m}$ deep trench, both being filled with silver paste. (c) is a prospective view for the silver-filled $15\mu\text{m}$ deep trench, while (d) indicates the top view dimension for the busbar/gridline pattern.

FIGURE 5: Cross-section of the rear side of the solar cell fabricated in this study.

However, the experimental results suffice to demonstrate the feasibility of the new selective emitter formation method.

Note that the trenched region has no texture in the presented method. The reflection of the trenched region not covered by metal contact is around 10% (11% down to 8% for 500 nm to 1000 nm, as Figure 6(a) reveals), while the reflection of the textured region ranges from $\sim 0.5\%$ to $\sim 2.7\%$, as Figure 6(b) indicates. As long as the area of the trenched region not covered by the metal contact is kept as small as possible, the higher reflection of the trenched region causes little effect on the photogenerated current. In our study, the

width of the trenched region is $300\mu\text{m}$, which can be further made smaller to reduce the reflection. An example would be $200\mu\text{m}$ trench width and $120\mu\text{m}$ metal contact width, which are both obtainable by using screening printing. For the case of $2300\mu\text{m}$ finger line spacing, the reflection increases only by 0.28% (relative) if an average reflection of 2% for a textured surface is assumed. Such increase in reflection would cause a reduction in photogenerated current and henceforth conversion efficiency of $<0.05\%$ (absolute), a loss which is negligible with respect to the gain from the selective emitter formed in the trenched region.

The width of the heavily doped area is $360\mu\text{m}$ for the fingers in this study, suggesting that an extra $60\mu\text{m}$ width of blue response is lost for each finger. The blue response loss may be kept as small as possible by reducing the additional width of the heavily doped region that is not covered by contact. However, such additional width is required for ensuring that screen printed contacts do not contact the lightly doped region. Use of a high-resolution aligning tool can reduce the additional width.

3.2. Effect of Back Surface a-Si:H on Homogeneous Emitter Cells. To clarify the effect of back surface a-Si:H deposition, we have carried out a different set of experiments with commercial pseudosquare $125 \times 125\text{ mm}^2$ silicon solar wafers used. They were p-type (100)-oriented Cz solar wafers with a resistivity of 1 to 3Ω . The experiments were conducted in a

FIGURE 6: Optical reflectance versus wavelength for wafers (a) without ARC deposited and (b) with ARC deposited. The legends refer to the etching time, with 0 min denoting an as-textured wafer, that is, a wafer that does not go through an etch-back process.

FIGURE 7: External quantum efficiency (EQE) versus optical wavelength for a reference cell (—), a back surface a-Si:H deposited cell (o o o), a selective emitter cell (▲▲▲) and a back surface a-Si:H deposited selective emitter cell (---).

cell manufacturing company, following a standard commercial manufacturing sequence, except that a sequence of a-Si:H deposition was added. The wafers were first cleaned in an SCl cleaning process, followed by a double-side alkaline texturization. These textured wafers after regular POCl_3 doping in an 880°C diffusion tube were cleaned and then processed by PECVD to form silicon nitride antireflection films on their front surfaces in the cell manufacturing company. Then, the wafers were sent to our institute, where 5 nm thick a-Si:H films were deposited on the rear sides by PECVD. The deposition temperature was 285°C , followed by an annealing

TABLE 3: Electrical parameters and conversion efficiencies measured, in a different set of experiments, for a reference cell (Ref.), and back-surface a-Si:H deposited cells annealed at 285°C (a-Si/ 285°C) and 400°C (a-Si/ 400°C). All of these cells have a homogeneous emitter.

	J_{sc} (mA/cm ²)	V_{oc} (mV)	F.F. (%)	η (%)
Ref.	36.84	625	78.56	18.09
a-Si/ 285°C	36.7	629.9	79.5	18.38
a-Si/ 400°C	36.79	630.1	79.51	18.43

step at either 285°C or 400°C for 10 minutes. After that, the wafers were sent back to the company for subsequent processing.

Table 3 shows the electrical parameters and conversion efficiencies of a reference cell (Ref.), and a-Si:H deposited cells annealed at 285°C (a-Si/ 285°C) and 400°C (a-Si/ 400°C), for this set of experiments. It is noted here that the cells in these experiments are superior to the foregoing cells owing to the use of standard industrial processing facilities for these cells. The reference cell was obtained following a standard commercial manufacturing sequence without a-Si:H deposited on the rear side. The two annealed a-Si:H deposited cells have a higher V_{oc} than the reference cell. This is believed to result from the reduction in back surface recombination velocity, which is reflected by the increased effective lifetime measured for these samples, as shown in Figure 8. The effective lifetime, measured by the microwave photoconductivity decay (μ -PCD) technique, reads $19.03\ \mu\text{s}$ and $23.27\ \mu\text{s}$ for the two annealed cells and $9.7\ \mu\text{s}$ for the reference cell. An optimal annealing temperature is expected in that the hydrogen atoms in a-Si would acquire sufficient energy to move toward the crystalline Si and form Si-H

FIGURE 8: Effective lifetimes of the reference cell (reference), the cell with 5 nm a-Si deposited on the rear side and annealed at 285°C (a-Si/285°C) and at 400°C (a-Si/400°C).

bonds thus passivating the dangling bonds at the a-Si/c-Si interface at a proper temperature, but most hydrogen atoms would be released from Si-H bonds at an elevated temperature, especially at the cofiring temperature. Since the high-temperature cofiring process only lasted for several tens of seconds, one may expect that the hydrogen leakage could not be so severe though. And this theory may support the long wavelength improvement in the EQE response. Nevertheless, a more sophisticated study may need to verify this. Note that the data given in each row of Table 3 were an average taken from measurement on 4 cells.

Questions may arise as to whether the 5 nm a-Si:H was consumed by Al alloying reaction at 800°C at the cofiring step and whether the a-Si still remained in the amorphous state or was crystallized. Even the a-Si might have been crystallized during the cofiring step, a part of the hydrogen atoms residing in the back side of the as-deposited wafer might still exist at the interface through a high-temperature soaking of a short time period. In this case, the wafer was passivated on the back side. On the other hand, perhaps there is another phenomenon occurring, such as the oxidation of the amorphous silicon layer during the aluminum alloying process. In that case, such a rear oxide layer may be offering some additional surface passivation. These questions may be further clarified by high-resolution SEM or TEM measurement in a future work. However, from the data we have obtained, we can now infer that the a-Si layer would still have surface passivation ability or otherwise similar effect through the cofiring (lasting for only several tens of seconds at the peak temperature) step.

4. Conclusion

A new fabrication method for selective emitter solar cells has been presented in this study. In the method, shallow trenches corresponding to front contact area were formed using a chemical etching method, followed by a heavy doping all over the front surface of the wafer. After screen printing a chemical-resistant mask to cover only the shallow trenches, the wafer was dipped into an etching solution to remove a part of silicon at the area not covered by the mask and thereby

form a lightly doped region on the front surface. We observed an enhanced optical response for the selective emitter cells in the UV-visible range. With a-Si:H deposited on the rear sides of the selective emitter cells, we further observed an improvement in the longer wavelength response. The experimental results show that selective emitter cells fabricated by the presented method are undoubtedly superior to homogeneous p-n junction cells. The purpose of experimental results here is to only demonstrate the feasibility of the new selective emitter formation method.

The conversion efficiency of selective emitter solar cell fabricated here is by no means high enough for attracting industry's attention. However, the presented technique can be considered as an alternative to current selective emitter techniques and this new technique can be adopted by industries as they only need to procure wet etching and screen printing facilities.

Acknowledgments

This research was financially supported by Grant 101N2518E1 from National Tsing Hua University, Hsinchu, Taiwan, and Grant 102-2221-E-007-089 from National Science Council, Taiwan. The authors would also like to thank Dr. Fangchi Hsieh, Jiangsu Aide Solar, Xuzhou, China, for allowing the authors to use facilities of his company as well as providing silicon wafers.

References

- [1] M. A. Green, J. Zhao, A. Wang, and S. R. Wenham, "Very high efficiency silicon solar cells-science and technology," *IEEE Transactions on Electron Devices*, vol. 46, no. 10, pp. 1940–1947, 1999.
- [2] J. M. Serra, R. Gamboa, and A. M. Vallera, "A study on selective emitter formation through an oxide mask for silicon solar cells," in *Proceedings of the 13th European Photovoltaic Solar Energy Conference*, pp. 1422–1425, 1995.
- [3] J. Horzel, J. Szlufcik, J. Nijs, and R. Mertens, "Simple processing sequence for selective emitters," in *Proceedings of the IEEE 26th Photovoltaic Specialists Conference (PVSC '97)*, pp. 139–142, October 1997.
- [4] H. Antoniadis, F. Jiang, W. Shan, and Y. Liu, "All screen printed mass produced silicon Ink selective emitter solar cells," in *Proceedings of the 35th IEEE Photovoltaic Specialists Conference (PVSC '10)*, pp. 1193–1196, June 2010.
- [5] J. H. Bultman, R. Kinderman, J. Hoornstra, and M. Koppes, "Single step selective emitter using diffusion barriers," in *Proceedings of the 16th European Photovoltaic Solar Energy Conference*, pp. 1424–1426, 2000.
- [6] S. Sivoththaman, W. Laureys, P. De Schepper, J. Nijs, and R. Mertens, "Selective emitters in Si by single step rapid thermal diffusion for photovoltaic devices," *IEEE Electron Device Letters*, vol. 21, no. 6, pp. 274–276, 2000.
- [7] A. Rohatgi, M. Hilali, D. L. Meier et al., "Self-aligned self-doping selective for screen-printed solar cells," in *Proceedings of the 17th European Photovoltaic Solar Energy Conference*, pp. 1307–1310, 2001.
- [8] L. M. Porter, A. Teicher, and D. L. Meier, "Phosphorus-doped, silver-based pastes for self-doping ohmic contacts for

- crystalline silicon solar cells,” *Solar Energy Materials and Solar Cells*, vol. 73, no. 2, pp. 209–219, 2002.
- [9] H. Haverkamp, A. Dastgheib-Shirazi, B. Raabe, F. Book, and G. Hahn, “Minimizing the electrical losses on the front side: development of a selective emitter process from a single diffusion,” in *Proceedings of the 33rd IEEE Photovoltaic Specialists Conference (PVSC '08)*, pp. 139–143, 2008.
- [10] M. Gauthier, M. Grau, O. Nichiporuk et al., “Industrial approaches of selective emitter on multicrystalline silicon solar cells,” in *Proceedings of the 24th European Photovoltaic Solar Energy Conference*, pp. 1875–1878, 2009.
- [11] Y. H. Wu, L. L. Chen, J. R. Wu, and M. L. Wu, “Selective emitter solar cell formation by NH₃ plasma nitridation and single diffusion,” *Semiconductor Science and Technology*, vol. 25, Article ID 015001, 2010.
- [12] http://www.pv-tech.org/news/schmids_selective_emitter_technology_supports_sunrise_global_solars_record.
- [13] D. Rudolph, K. Peter, A. Meijer, O. Doll, and I. Köhler, “Etch back selective emitter process with pocl₃ diffusion,” in *Proceedings of the 26th European Photovoltaic Solar Energy Conference*, pp. 1349–1352, 2011.
- [14] B. Hallam, S. Wenham, A. Sugianto et al., “Record large area p-type CZ production cell efficiency of 19.3% based on LDSE technology,” *IEEE Journal of Photovoltaics*, vol. 1, pp. 43–48, 2011.
- [15] G. Poulain, D. Blanc, A. Focsa et al., “Laser process for selective emitter silicon solar cells,” *International Journal of Photoenergy*, vol. 2012, Article ID 413863, 5 pages, 2012.
- [16] Z. Shi, S. Wenham, and J. Ji, “Mass production of the innovative PLUTO solar cell technology,” in *Proceedings of the 34th IEEE Photovoltaic Specialists Conference (PVSC '09)*, pp. 1922–1926, June 2009.
- [17] B. Ketola, K. R. McIntosh, A. Norris, and M. K. Tomalia, “Silicones for photovoltaic encapsulation,” in *Proceedings of the 23th European Photovoltaic Solar Energy Conference*, pp. 2969–2973, 2008.
- [18] N. E. Powell, B. K. Hwang, A. W. Norris, B. M. Ketola, G. Beaucarne, and K. R. McIntosh, “Improved spectral response of silicone encapsulated photovoltaic modules,” in *Proceedings of the 35th IEEE Photovoltaic Specialists Conference (PVSC '10)*, pp. 2791–2794, June 2010.