Research Article

Study of Small Molecule Organic Solar Cells Performance Based on Boron Subphthalocyanine Chloride and C₆₀

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The small molecule organic solar cells based on boron subphthalocyanine chloride (SubPc) and C₆₀ by varying the SubPc layer thickness from 3 nm to 21 nm were fabricated. The maximum power conversion efficiency (PCE) of 1.47% was obtained at the 9 nm SubPc layer under 100 mW/cm² AM1.5G illumination, which is attributed to reach the optimal balance between the light absorption efficiency and the carrier collection efficiency in the device. To increase the open-circuit voltage (V_{oc}) of device, the molybdenum oxide (MoO₃) and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) were inserted between the indium tin oxide and the SubPc layer, respectively. Finally, the V_{oc} of device increased from 0.46 V to 1 V by using MoO₃ buffer layer, resulting in the fact that the PCE of device increased from 1.47% to 2.52%.

1. Introduction

Solar cells are considered as an important source of renewable energy to solve the shortage of energy today. Various solar cells have been developed and one of the most promising solar cells is organic solar cells (OSCs). OSCs have received much attention recently due to several potential applications, including compatibility with flexible substrates, low-manufacturing cost, and roll-to-roll fabrication process [1–3]. In organic materials, light absorption leads to the formation of excitons (bound electron-hole pairs) rather than the free electron-hole pairs. The excitons dissociation occurred at the donor-acceptor interfaces, using the difference of energy level to overcome the binding energy of excitons, leading to the free electron and hole in device which can be extracted to the electrodes. Since Tang reported the first two-layer heterojunction OSC [4], the power conversion efficiency of OSCs had increased steadily in the recent years by using new materials and the different device structures [5–8]. The shortage of organic materials is narrow absorption range in visible region, which leads to the low short-circuit current

density (J_{sc}). Therefore, to get the highest J_{sc} for the best performance, optimizing the device structure is necessary [9, 10].

Boron subphthalocyanine chloride (SubPc) is a promising donor material for the small molecule OSCs due to its deep highest occupied molecular orbital (HOMO) energy level, which can get the higher V_{oc} of device. In this paper, we used SubPc as donor and changed the thickness of SubPc layer to investigate the influences on performance and to obtain the optimal thickness of SubPc for the best efficiency. In addition, the V_{oc} variation of device with different SubPc layer thicknesses and anode buffer layers is also investigated in detail.

2. Experimental

The indium tin oxide (ITO)/glass substrates (with a sheet resistance of 7 Ω /sq) are sequentially cleaned by ultrasonic treatment in acetone, isopropyl alcohol, and deionized water and blown by N₂ gas before deposition. The layer of poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate)

FIGURE 1: The configuration of device and the energy level diagram in the study.

FIGURE 2: The J - V characteristics of devices (ITO/SubPc/ C_{60} (30 nm)/BCP (10 nm)/Ag) with different SubPc layer thicknesses (3~21 nm).

(PEDOT:PSS) was formed by a spin-coating method. The spin coatings were performed at a rotation rate of 3500 rpm for 20s. The organic materials in the device were MoO₃ (99%), SubPc (99%), C₆₀ (99.95%), and BCP (99%), which were used without further purification. All layers in OSC were deposited at a deposition rate of 0.02~0.04 nm/s below the pressure of 6.4×10^{-4} Pa. The Ag as a cathode was deposited at a deposition rate of 0.2~0.3 nm/s by thermal evaporation through a shadow mask, giving an active area of 6 mm². The thickness of thin film was monitored by an oscillating quartz thickness monitor. The configurations of device and the energy level in this study are shown in Figure 1.

The current-voltage characteristics are measured with a Keithley 2400 sourcemeter, under an illumination of 100 mW/cm² with an AM1.5G sun simulator. The intensity of irradiation was measured by an optical power meter. All measurements were carried out in air without any encapsulation.

TABLE 1: Photovoltaic performance parameters of devices (ITO/SubPc (3~21 nm)/C₆₀ (30 nm)/BCP (10 nm)/Ag) with different SubPc layer thicknesses.

SubPc thickness (nm)	J_{sc} (mA/cm ²)	V_{oc} (V)	FF	R_s (Ω·cm ²)	η (%)
3	3.70	0.34	0.55	17.8	0.69
6	4.70	0.32	0.54	13.0	0.82
9	5.79	0.46	0.55	14.4	1.47
12	4.77	0.52	0.38	62.8	0.95
15	4.68	0.59	0.37	127.9	1.04
18	4.12	0.58	0.30	233.9	0.72
21	3.47	0.57	0.27	326.9	0.55

3. Results and Discussion

Figure 2 showed the current density-voltage (J - V) characteristics of device (ITO/SubPc (3~21 nm)/C₆₀ (30 nm)/BCP (10 nm)/Ag) with different SubPc layer thicknesses. The performance parameters and the series resistance (R_s) were listed in Table 1. The SubPc layer thickness of device has not only influence on the amount of light absorption but also influence on the ability of carrier transportation in device. Both of light absorption and the R_s increased as the SubPc layer thickness increased. In Table 1, the J_{sc} of device increased from 3.70 mA/cm² to 5.79 mA/cm² when the SubPc layer thickness from 3 nm to 9 nm, which is attributed to the more light absorption with thicker SubPc layer. However, the advantage of SubPc as an electron donor in device was not revealed, high V_{oc} value, which will be discussed later. It was found that the R_s of device with 12 nm SubPc layer is nearly four times than that of device with 9 nm SubPc layer, indicating that the carrier extracted from SubPc to ITO became hard as the thickness of SubPc layer exceeds 9 nm. It might result from the short diffusion length of SubPc which is only about 8 nm [11]. As a result, the J_{sc} of device continually decreased from 5.79 mA/cm² to 3.47 mA/cm² corresponding to the SubPc layer thickness from 9 to 21 nm. The fill factor (FF) of device is associated with the R_s , and the change of FF is consistent with the R_s variation. As the R_s of device increased, the FF of device decreased. Finally, the optimal balance between light absorption and carrier transportation was obtained at 9 nm SubPc, resulting in higher efficiency of 1.47% at 9 nm SubPc than that of device with other SubPc layer thicknesses.

The V_{oc} of device increased as the SubPc layer thickness increased from 3 nm to 15 nm and then saturation at 0.58 ± 0.1 V from 15 nm to 21 nm. The tendency of V_{oc} variation is in agreement with the result obtained by Kim and Yim [12]. To investigate the origin of V_{oc} which varied as a function of SubPc layer thickness, the surface morphologies of different SubPc layer thicknesses deposited on ITO/glass substrate were measured. Figure 3 showed the height profiles of bare ITO, 3 nm SubPc, 6 nm SubPc, and 9 nm SubPc deposited on ITO, respectively. It can be seen that the roughness of bare ITO is as high as 7 nm, resulting in that the vacancy of ITO cannot be fully covered by the 3 nm or 6 nm SubPc layer

FIGURE 3: The height profiles of (a) bare ITO, (b) ITO/SubPc (3 nm), (c) ITO/SubPc (6 nm), and (d) ITO/SubPc (9 nm).

(as shown in Figures 3(b) and 3(c)). As a result, the contact between the ITO and the C_{60} after depositing C_{60} on SubPc layer cannot be avoided, causing that the V_{oc} of device with 3 nm and 6 nm SubPc is only at 0.34 V and 0.32 V, respectively. In contrast, the 9 nm SubPc layer is thicker enough to cover the roughness of ITO, which can avoid the contact between ITO and C_{60} , resulting in that the V_{oc} of device with 9 nm SubPc layer is enhanced to 0.46 V. However, the V_{oc} of device still continually increased from 0.46 V to 0.59 V as the SubPc layer thickness increased from 9 nm to 15 nm. It results from the carrier accumulation in SubPc layer, which can be realized from the R_s which dramatically increased, resulting in the increase of electric potential in SubPc layer. The V_{oc} of device was maintained in a value at SubPc layer thickness from 15 nm to 21 nm, and it is due to the fact that the amount of carrier accumulated in SubPc layer is saturated. That is to say, the balance of carrier generation and recombination was achieved at SubPc layer thickness above 15 nm, leading to that the amount of carrier is the same in SubPc layer.

However, the V_{oc} of device based on SubPc and C_{60} is still lower than that of other studies which also used the

same materials. In theorem, the maximum V_{oc} of OSCs is limited by the energy difference between the HOMO energy level of donor and the lowest unoccupied molecular orbital (LUMO) energy level of acceptor [13], and the V_{oc} in device is determined by difference of work function of electrodes within the maximum V_{oc} [14]. From Figure 1, the energy level difference between HOMO of SubPc and the LUMO of C_{60} is 1.1 V. The V_{oc} of devices with different SubPc layer thicknesses ranges from 0.32 V to 0.59 V, which is far from 1.1 V. The results were attributed to the low work function of ITO typically at 4.7 V. To improve the work function of ITO, the MoO_3 layer and the PEDOT:PSS inserted between the ITO and the SubPc layer in the device with optimal SubPc layer thickness of 9 nm, respectively. The performance parameters were summarized in Table 2. The V_{oc} of device was enhanced to 0.77 V and 1 V by inserting the PEDOT:PSS and the MoO_3 layer, respectively. The surface morphologies of bare ITO, ITO/PEDOT:PSS, and ITO/ MoO_3 were measured to further clarify whether the V_{oc} enhancement is attributed to the roughness of ITO. Figure 4 showed the AFM images of bare ITO, ITO/PEDOT:PSS, and ITO/ MoO_3 corresponding to

FIGURE 4: The surface morphologies of (a) bare ITO, (b) ITO/PEDOT: PSS, and (c) ITO/MoO₃.

TABLE 2: Photovoltaic performance parameters of device (ITO/PEDOT:PSS or MoO₃/SubPc (9 nm)/C₆₀ (30 nm)/BCP (10 nm)/Ag) with different buffer layers.

Buffer layer	J_{sc} (mA/cm ²)	V_{oc} (V)	FF	R_s (Ω·cm ²)	η (%)
PEDOT:PSS	4.12	0.77	0.35	20.06	1.13
MoO ₃	4.56	1	0.55	31.7	2.52

the root mean square roughness of 3.73 nm, 2.08 nm, and 3.92 nm, respectively. It can be seen that the MoO₃ cannot smooth the ITO surface, indicating that the enhancement of V_{oc} was not related to the roughness of ITO. As a result, the improvement of V_{oc} can be ascribed to the work function of ITO modification by the PEDOT:PSS and the MoO₃. In addition, the V_{oc} of device using MoO₃ as a buffer layer is higher than that of device with PEDOT:PSS buffer layer due to the fact that the HOMO energy level of MoO₃ is deeper than that of PEDOT:PSS. The PEDOT:PSS layer was not optimized here, causing that the efficiency of device decreased from 1.47% to 1.13% by using PEDOT:PSS buffer layer. Eventually, the advantage of small molecule OSC based on the SubPc and the C₆₀, high V_{oc} , was achieved by depositing the MoO₃ layer on the ITO, resulting in the efficiency improvement from 1.47% to 2.56%.

4. Conclusions

The performances of devices with different SubPc layer thicknesses have been investigated. The maximum J_{sc} and FF were achieved simultaneously at 9 nm SubPc, which is

attributed to reach the optimal balance between the light absorption efficiency and the carrier collection efficiency in device, resulting in the efficiency of 1.47%. In addition, to obtain the highest V_{oc} of device not only needs the deepest HOMO level of donor but also needs the highest work function of anode. The V_{oc} of device by using MoO₃ as a buffer layer is better than that of device using PEDOT:PSS. As a result, the V_{oc} is greatly improved from 0.46 V to 1 V by inserting the MoO₃ layer between the ITO and SubPc layer, leading to an increase in efficiency of device from 1.47% to 2.52%.

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