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Research Article

A Novel LTPS-TFT Pixel Circuit to Compensate the Electronic Degradation for Active-Matrix Organic Light-Emitting Diode Displays

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A novel pixel driving circuit for active-matrix organic light-emitting diode (AMOLED) displays with low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) is studied. The proposed compensation pixel circuit is driven by voltage programming scheme, which is composed of five TFTs and one capacitor, and has been certified to provide uniform output current by the Automatic Integrated Circuit Modeling Simulation Program with Integrated Circuit Emphasis (AIM-SPICE) simulator. The results of simulation show excellent performance, such as the low average error rate of OLED current variation (<0.5%) and the low average nonuniformity of OLED current variation (<0.8%) while the shift of threshold voltage of the driving poly-Si TFT and the OLED are both in the worst case ($\Delta V_{TH} = \pm 0.33$ V for TFT and $\Delta V_{TH\_O} = +0.33$ V for OLED). The proposed pixel circuit shows high immunity to the threshold voltage deviation of both the driving poly-Si TFT and the OLED.

1. Introduction

The organic light-emitting diode (OLED) has gained a lot of attention due to its potential advantages, such as light weight, fast response time, wide viewing angle, and high brightness [1–3]. OLED display can be classified into two major driving types: the passive-matrix (PM) driving and active-matrix (AM) driving. The PM driving method has some merits of simple manufacturing process, high yield, and larger aperture ratio. However, it has a challenge of the large size and high-resolution panels because of its high power consumption and short OLED life time [4]. The AM driving uses a thin-film transistor (TFT) backplane to control the gray level of each pixel, achieving lower power consumption and longer OLED life time. Thus, the AM driving method would be a promising candidate to replace the PM driving for higher resolution and larger display sizes.

The low-temperature polycrystalline-silicon (poly-Si) thin-film transistors (LTPS-TFTs) have been widely utilized in active-matrix OLED (AMOLED) displays because of their high current driving capability. However, the LTPS-TFTs have an issue that is the nonuniformity of threshold voltage (V_{TH}) and mobility due to process variation, further resulting in different OLED current levels among pixels. In the conventional two-TFT pixel circuit for AMOLED, the various threshold voltages of driving TFT (DTFT) cause nonuniform gray-scale over the display area. Thus, several compensating methods have been developed and can be classified into voltage programming [5–12] and current programming [13–16]. Though the current programming method can compensate for the variation of both mobility and threshold voltage, but it has demerits in that low data current will result in long settling time because of the high parasitic capacitance of data lines. The long settling time is the critical issue for large panels

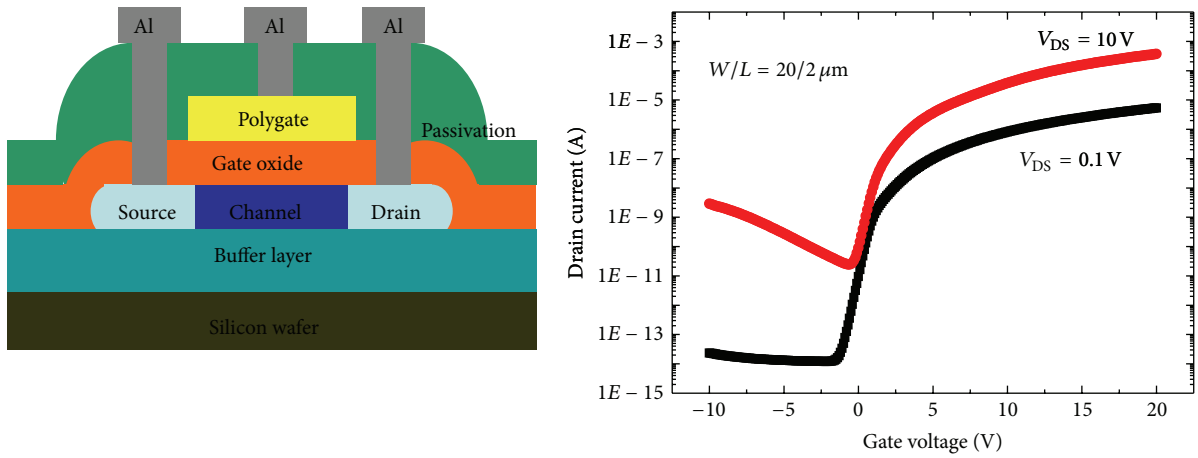

Figure 1: (a) Cross-section of the poly-Si TFT. (b) The device transfer curve.

with high resolution. Comparing with current programming method, the voltage programming method is more suitable to be applied in large size and high-resolution panels due to the ability of short settling time.

In addition, since the efficiency and threshold voltage of OLED decays to cause the luminance degradation under a long-time operation [17], many schemes have been reported to compensate for the threshold voltage variation of driving TFT. However, in the published compensated pixel circuits, the number of TFTs, the error rate of OLED current under the TFT threshold voltage deviation, and the degradation of OLED are not usually optimized at the same time [2, 6, 18]. In this study, we propose a new voltage programming AMOLED pixel design. The proposed pixel circuit, which comprised five TFTs and one capacitor (5T1C), has been verified to successfully compensate for the threshold voltage deviation of both the DTFT and the OLED at the same time. And the simulation results demonstrate that the novel design can effectively improve the average error rate (<0.5%) and the nonuniformity (<0.8%) of OLED current. Therefore, the proposed design successfully provides highly stable OLED current and is suitable for large-size and high-resolution displays.

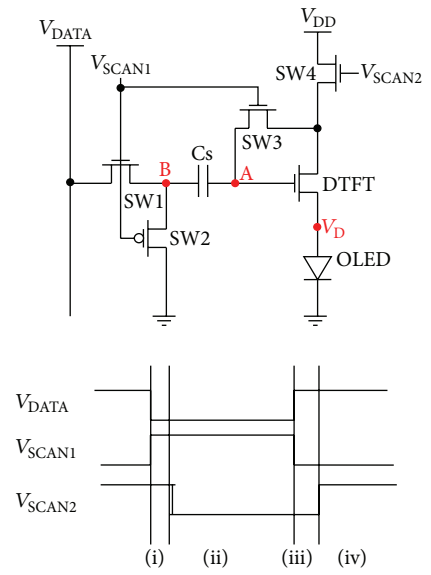

Figure 2: Proposed pixel design and timing scheme of the signal line.

2. Process Flow and Poly-Si TFT Characteristics

The poly-Si TFTs were fabricated on silicon wafer. Main features of the LTPS device structure are shown in Figure 1(a). A 110 nm amorphous silicon (a-Si) active layer was deposited on the buffer layer by low-temperature chemical vapor deposition (LPCVD) at 550°C, followed by annealing in nitrogen at 600°C. The poly-Si was patterned for active islands, and a 120 nm thick SiO_2 layer was deposited by plasma-enhanced chemical vapor deposited (PECVD) as a gate insulator. Then, a poly-Si layer was deposited and patterned for gate electrode. The source and drain region were doped with phosphorous ion by the self-aligned ion-implantation at 40 keV to a dose of 5×10^{15} cm^{-2}. The dopants were activated at 600°C for 24 hours. Finally, a 500 nm thick PECVD-TEOS oxide was deposited as a passivation layer and patterned for contact holes. Figure 1(b) shows the transfer characteristics of poly-Si TFT with a width of 20 μm and length of 2 μm at V_{DS} = 0.1 V and V_{DS} = 10 V, respectively.

3. New Pixel Circuit Design Scheme

As shown in the circuit configuration and timing diagram of Figure 2, the proposed pixel circuit employs five TFTs including four switching TFTs (SW1–SW4), one driving TFT (DTFT), one signal holding capacitor (C_s), two scan lines, and one signal data line. The relevant operation stage comprises four states, including precharging, compensating, data input, and emission states. The design parameters of proposed pixel

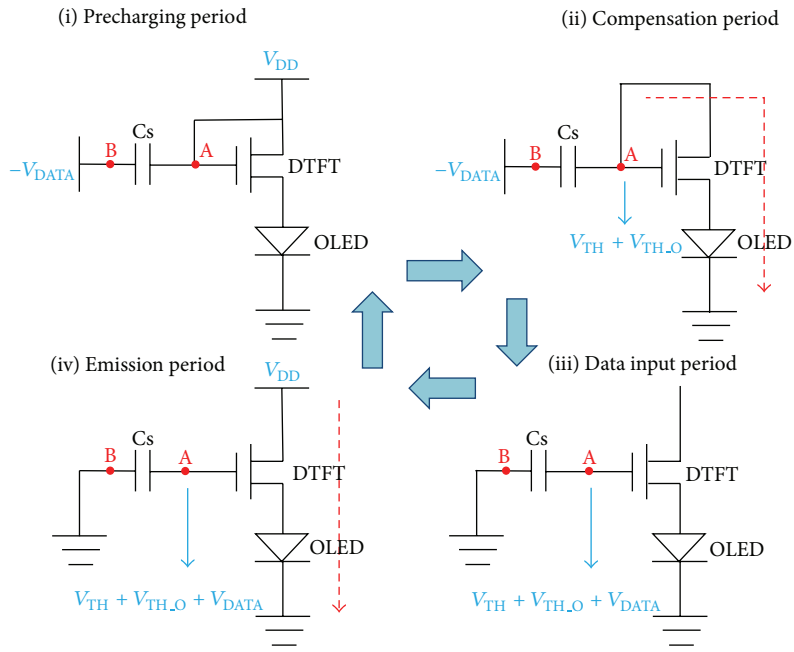

Figure 3: Equivalent circuit at each state in operation.

Table 1: Simulation parameters of the proposed circuit.

Devices	W/L (SW1–SW4) (μm)	8/2
	W/L (DTFT) (μm)	20/2
	C_s (pF)	0.1
	V_{TH} (DTFT) (V)	1
	V_{TH_O} (OLED) (V)	1
Signal line	V_{SCAN1} (V)	−9 to 9
	V_{SCAN2} (V)	−3 to 15
	V_{DD} (V)	9
	V_{DATA} (V)	−5 to −2

circuit are listed in Table 1. As shown in the equivalent operation circuit of Figure 3, the equivalent circuit includes a driving TFT (DTFT) and a signal holding capacitor C_s in addition to the OLED. It is to be noted that the signal holding capacitor C_s not only accumulates electric charges from the system power V_{DD} but also bleeds/discharges stored electric charges to ground via the DTFT and the OLED, respectively. The operational method and compensation principle of the proposed pixel design are described as follows.

3.1. Precharging Period. The task in this period is precharging and resetting the $V_{DD} + V_{DATA}$ stored in the capacitor C_s. Both V_{SCAN1} and V_{SCAN2} are high; so, SW1, SW3, and SW4 are turned on, and SW2 is turn turned off. Therefore, the voltage of the signal holding capacitor C_s located at node A is charged to approach V_{DD} through SW3 and SW4. Furthermore, the data line is biased by a negative voltage. Since the node B is coupled to the data line, the storage voltage across the signal holding capacitor C_s can be written as $V_A - V_B = V_{DD} + V_{DATA}$. Hence, the gate voltage of the DTFT connected to the signal holding capacitor C_s is also reset for initialization. This stage can get rid of the effects of previous operations.

3.2. Compensating Period. In this stage, the threshold voltages of both the DTFT (V_{TH}) and the OLED (V_{TH_O}) are detected by the compensation operation. When V_{SCAN1} remains high, it sustains SW1 and SW3 in the "on" state and SW2 in the "off" state. Meanwhile, V_{SCAN2} becomes low, and it turns off SW4 only. Hence, the gate voltage of the DTFT continues discharging through SW3, DTFT, and OLED until the DTFT is turned off. In this way, the gate voltage of the DTFT that has a diode-connect structure will reach $V_{TH} + V_{TH\_O}$, where V_{TH} is the threshold voltage of the DTFT, and V_{TH_O} is the threshold voltage of the OLED.

3.3. Data Input Period. In the data input stage, when V_{SCAN1} returns to a low value, it turns off SW1 and SW3 and turns on SW2 simultaneously. At this moment, V_{SCAN2} constantly remains low, which forces SW4 in the "off" state. Furthermore, voltage at node B is applied by zero voltage. Thus, the voltage at node B of the signal holding capacitor C_s becomes zero voltage, and the gate of DTFT is charged up to a high potential, which is high enough not to interfere with the compensation operation at the next frame. The gate voltage of the DTFT is boosted up to $V_{TH} + V_{TH\_O} + V_{DATA}$ by the conservation of charge in the capacitor C_s.

3.4. Emission Period. In the emission stage, when V_{SCAN1} continues low, it keeps both SW1 and SW3 in the "off" state and keeps SW2 in the "on" state. Meanwhile, V_{SCAN2} becomes high; as a result, it turns on SW4. In addition, the node B is continuously applied by zero voltage. Hence, the signal holding capacitor C_s maintains the gate voltage of the DTFT, as

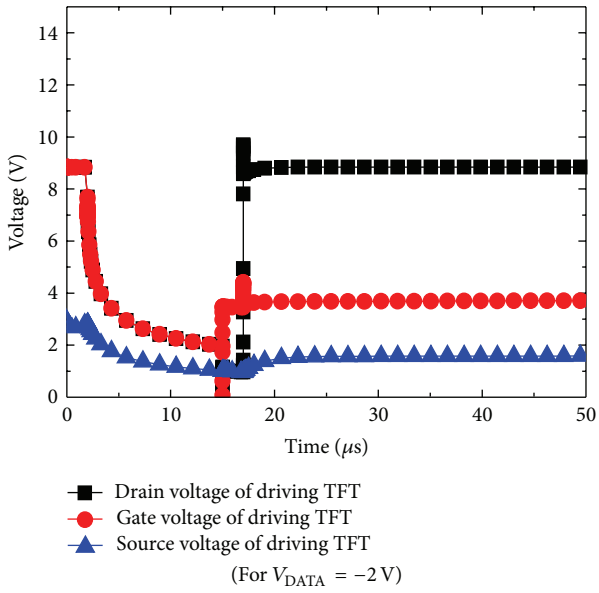

Figure 4: Gate, source, and drain voltage of DTFT with operation stages when V_{DATA} = −2 V.

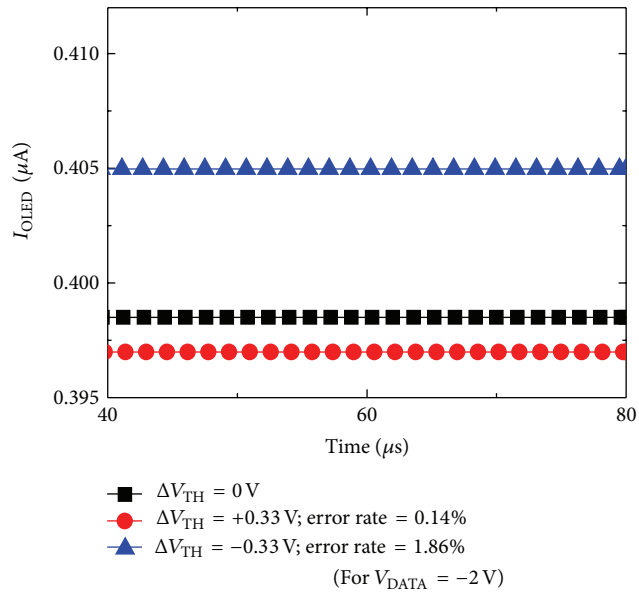

Figure 5: The OLED current with the variation in the threshold voltage of DTFT when V_{DATA} = −2 V.

mentioned eariler, up to the next cycle of precharging stage. The OLED current (I_{OLED}) can be written using the drain current of the DTFT in the saturation region as

$$\begin{aligned} I_{OLED} &= \frac{1}{2}K_{DTFT}\left(V_{GS_{DTFT}} - V_{TH}\right)^2 \\ &= \frac{1}{2}K_{DTFT}\left(V_{TH} + V_{TH\_O} + |V_{DATA}| - V_D - V_{TH}\right)^2 \\ &= \frac{1}{2}K_{DTFT}\left(|V_{DATA}| + V_{TH\_O} - V_D\right)^2, \end{aligned} \quad (1)$$

where V_D is the anode voltage of OLED when OLED is emitting. Therefore, I_{OLED} is independent of the threshold voltage deviation of DTFT, and only affected by V_{DATA}, V_{TH_O}, and V_D. The threshold voltage of OLED (V_{TH_O}) will be increased when the OLED degrades under long time operation, so that the OLED driving current is also increased to compensate for the degraded luminance of OLED during the emitting period. Thus, we believe that the proposed pixel circuit can also compensate the threshold voltage degradation of OLED and DTFT under the long operation time at the same time.

4. Result and Discussion

In this study, we had used poly-Si TFT model of AIM-SPICE with level 16 for pixel circuit simulation. And the OLED was modeled by a diode-connected poly-Si TFT and a capacitor. The OLED capacitance was set to 25 nF/cm^2 in this simulation. And the dimension of the channel width/length for DTFT had been set to 20/2 μm.

The gate, drain, and source node's voltages of DTFT under the data voltage V_{DATA} (−2 V) are shown in Figure 4. At the end of compensating period, the gate voltage of DTFT is discharged until 2 V (V_{TH} + V_{TH_O}), where V_{TH} is the threshold voltage of DTFT, and V_{TH_O} is the threshold voltage of OLED. The expectancy of circuit operation is verified by the simulation result. During the emission period, the gate voltage of DTFT is 4 V (V_{TH} + V_{TH_O} + $|V_{DATA}|$). Thus, the V_{GS} of DTFT is V_{TH} + V_{TH_O} + $|V_{DATA}|$ − V_D, where V_D is the voltage of OLED when OLED is emitting light. Thus, the proposed pixel circuit can efficiently compensate for the OLED degradation.

The OLED current with the threshold voltage deviation of DTFT (ΔV_{TH} = ±0.33 V) under the data voltage (−2 V) is shown in Figure 5. The error rate of the OLED current is defined as the difference between the shifted OLED current of driving TFT (ΔV_{TH} = ±0.33 V) and the normal OLED current (ΔV_{TH} = 0 V) divided by the normal OLED current (ΔV_{TH} = 0 V), as follows:

$$\text{error rate} = \frac{I_{OLED}\left(\Delta V_{TH} = \pm 0.33\text{ V}\right) - I_{OLED}\left(\Delta V_{TH} = 0\text{ V}\right)}{I_{OLED}\left(\Delta V_{TH} = 0\text{ V}\right)}. \quad (2)$$

It is found that the error rates of the OLED current under the ΔV_{TH} = ±0.33 V of DTFT for input V_{DATA} = −2 V were 0.14% and 1.86%, respectively. The driving current of OLED will affect the luminance of OLED and thus represent the display brightness because the OLED is current driving unit. The simulation result has shown that the current variation of OLED caused by the threshold voltage deviation of DTFT is very small. Figure 6 shows the error rates of OLED current at different data voltages ($|V_{DATA}|$) with the threshold voltage deviation of DTFT (ΔV_{TH} = ±0.33 V). The error rate of OLED current is the deviation percentage of the original OLED current (ΔV_{TH} = 0 V) when the varied threshold voltage of DTFT is +0.33 or −0.33 V. It can be clearly showed that the maximum error rate of OLED current is below 2%, and the average error rate is 0.5% for the proposed pixel circuit. In the conventional 2T1C pixel circuit, the average error rate

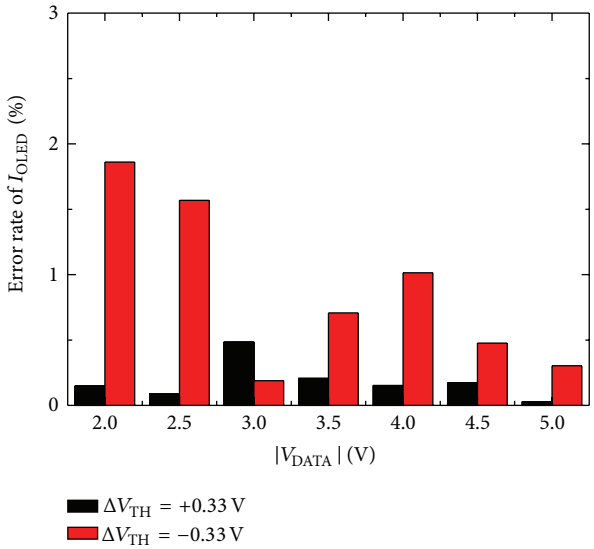

FIGURE 6: The error rates of I_{OLED} at different V_{DATA} with threshold voltage variations (ΔV_{TH} = −0.33 and +0.33 V); the average error rate is 0.5%.

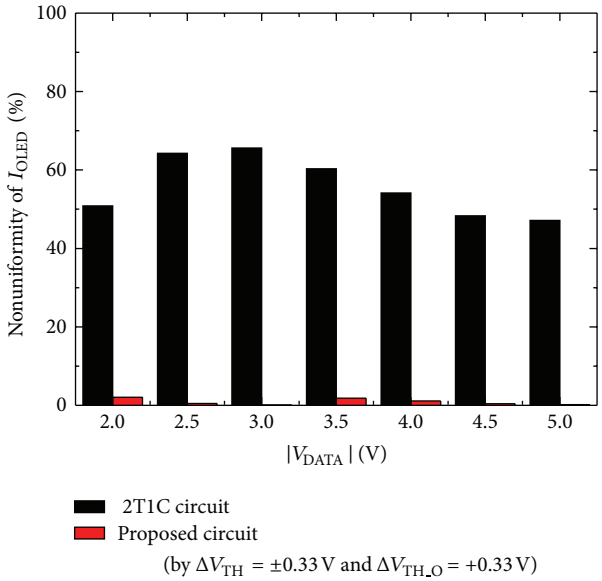

FIGURE 7: The nonuniformity of I_{OLED} at different V_{DATA} under the worst case (ΔV_{TH} = ±0.33 V and ΔV_{TH_O} = +0.33 V). The average nonuniformity is 0.89%.

is about 30%. Therefore, the display image quality of the proposed pixel circuit will be more uniform than that in the other reports [12]. The results can prove that the proposed pixel circuit has high immunity to the threshold voltage deviation of DTFT. As a result, the proposed pixel circuit is capable of providing a uniform OLED driving current regardless of the variation in the poly-Si TFT performance.

The increases in OLED threshold voltage (V_{TH_O}) with emission for a long time degrade the display image quality. Figure 7 shows the nonuniformity of OLED current in the worst case (ΔV_{TH} = ±0.33 V and ΔV_{TH_O} = +0.33 V) for different data voltages ($|V_{DATA}|$) for the proposed pixel circuit and the conventional 2T1C pixel circuit, respectively. The I_{OLED} nonuniformity is defined as the difference between the maximum OLED current ($I_{OLEDMAX}$ when ΔV_{TH} = −0.33 V for TFT, ΔV_{TH_O} = 0 for OLED) and the minimum OLED current ($I_{OLEDMIN}$ when ΔV_{TH} = +0.33 V for TFT, ΔV_{TH_O} = +0.33 for OLED), divided by their average OLED current (($I_{OLEDMAX}$ + $I_{OLEDMIN}$)/2) as follows:

$$\text{nonuniformity} = \frac{I_{OLEDMAX}\left(\Delta V_{TH} = -0.33\,\text{V}, \Delta V_{TH\_O} = 0\right)}{\left(I_{OLEDMAX} + I_{OLEDMIN}\right)/2} - \frac{I_{OLEDMIN}\left(\Delta V_{TH} = +0.33\,\text{V}, \Delta V_{TH\_O} = +0.33\right)}{\left(I_{OLEDMAX} + I_{OLEDMIN}\right)/2}. \quad (3)$$

The uniformity of display image can be improved by reducing the nonuniformity of OLED current. Compared with simulation results for the conventional 2T1C pixel circuit and the reported compensating circuit [19], the proposed circuit can offer a more stable driving current, which is independent of the threshold voltage variation of DTFT (ΔV_{TH} = ±0.33 V) and the degraded OLED threshold voltage (ΔV_{TH_O} = +0.33 V) for different data voltages. For the proposed pixel circuit, the average nonuniformity is approximately 0.89%. In addition, the average nonuniformity of the conventional 2T1C pixel circuit and the reported compensating circuit (5T2C) is about 55% and 5.7%, respectively [19]. Clearly, the proposed pixel circuit has high immunity to DTFT threshold voltage shifts and OLED degradation, resulting from the compensation for the threshold voltage deviation of DTFT and OLED aging phenomenon at the same time.

5. Conclusion

A novel voltage programming pixel circuit for active-matrix organic light-emitting diode (AMOLED) displays was studied. The proposed circuit was verified by AIM-SPICE simulator. The proposed circuit consisted of five TFTs and one capacitor and successfully compensated for the threshold voltage deviation of DTFT and the degradation of OLED. The average nonuniformity of the proposed pixel circuit is approximately 0.8% in the worst case. The proposed pixel circuit design can provide stable driving current to the AMOLED panel for achieving high-resolution images, thereby promising candidate for the large size and high-resolution AMOLED panels.

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