Research Article

Grid Connected Solar PV System with SEPIC Converter Compared with Parallel Boost Converter Based MPPT

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The main objective of this work is to study the behaviour of the solar PV systems and model the efficient Grid-connected solar power system. The DC-DC MPPT circuit using chaotic pulse width modulation has been designed to track maximum power from solar PV module. The conversion efficiency of the proposed MPPT system is increased when CPWM is used as a control scheme. This paper also proposes a simplified multilevel (seven level) inverter for a grid-connected photovoltaic system. The primary goal of these systems is to increase the energy injected to the grid by keeping track of the maximum power point of the panel, by reducing the switching frequency, and by providing high reliability. The maximum power has been tracked experimentally. It is compared with parallel boost converter. Also this model is based on mathematical equations and is described through an equivalent circuit including a PV source with MPPT, a diode, a series resistor, a shunt resistor, and dual boost converter with active snubber circuit. This model can extract PV power and boost by using dual boost converter with active snubber. By using this method the overall system efficiency is improved thereby reducing the switching losses and cost.

1. Introduction

Because of constantly growing energy demand, grid-connected photovoltaic (PV) systems are becoming more and more popular, and many countries have permitted, encouraged, and even funded distributed-power-generation systems. Currently, solar panels are not very efficient with only about 12–20% efficiency in their ability to convert sunlight to electrical power. The efficiency can drop further due to other factors such as solar panel temperature and load conditions. In order to maximize the power derived from the solar panel, it is important to operate the panel at its optimal power point. To achieve this, a maximum power point tracker will be designed and implemented.

The MATLAB/PSpice model of the PV module is developed [1–4] to study the effect of temperature and insolation on the performance of the PV module. The power electronics interface, connected between a solar panel and a load or battery bus, is a pulse width modulated (PWM) DC-DC converter or their derived circuits used to extract maximum

power from solar PV panel. *I-V* characteristic curve of photovoltaic generators based on various DC-DC converters [5–8] was proposed and concluded that SEPIC converter is the best alternative to track maximum power from PV panel. The various types of nonisolated DC-DC converters for the photo voltaic system is reviewed [9].

The maximum power tracking for PV panel using DC-DC converter is developed [10] without using microcontroller. This approach ensures maximum power transfer under all atmospheric conditions. The analogue chaotic PWM is used to reduce the EMI in boost converter. The conversion efficiency is increased when CPWM is used as a control technique [11–13]. To increase conversion efficiency, an active clamp circuit is introduced into the proposed one to provide soft switching features to reduce switching losses. Moreover, switches in the converter and active clamp circuit are integrated with a synchronous switching technique to reduce circuit complexity and component counts, resulting in a lower cost and smaller volume [14].

Multilevel inverter consists of an array of power semiconductor switches, capacitor voltage sources, and clamping diodes. The multilevel inverter produces the stepped voltage waveforms with less distortion, less switching frequency, higher efficiency, lower voltage devices, and better electromagnetic compatibility [15]. The commutation (process of turn off) of the switches permits the addition of the capacitor voltages, which reach high voltages at the output [16].

A modular grid-connected PV generation system presents an actual behavioural model of a grid tied PV system suitable for system level investigations. Simplified means for modelling the PV array and investigating a gradient based MPPT into a very simple averaged model of the power converter was developed, and the model has been experimentally vetted [17, 18]. A single-phase grid-connected inverter which is usually used for residential or low-power applications of power ranges that are less than 10 kW [15]. Types of single-phase grid-connected inverters have been investigated [19]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [20].

MATLAB-based modelling and simulation scheme which is suitable for studying the I - V and P - V characteristics of a PV array under a nonuniform insolation due to partial shading [21] was proposed. The mathematical model of solar PV module is useful for the computer simulation. The power electronics interface, connected between a solar panel and a load or battery bus, is a pulse width modulated (PWM) DC-DC converter or their derived circuits used to extract maximum power from solar PV panel [22]. The main drawback of PV systems is that the output voltage of PV panels is highly dependent on solar irradiance and ambient temperature. Therefore PV panels outputs cannot connect directly to the load. To improve this, a DC-DC boost converter is required to interface between PV panels and loads [23]. The boost converter is fixing the output voltage of the PV system. Converter receives the variable input voltage which is the output of PV panels and gives up constant output voltage across its output capacitors where the loads can be connected. In general, a DC-DC boost converter operates at a certain duty cycle. In this case, the output voltage depends on that duty cycle. If the input voltage is changed while the duty cycle is kept constant, the output voltage will vary. Duty cycle is varied by using a pulse width modulation (PWM) technique [24].

Silicon carbide (SiC) represents an advance in silicon technology because it allows a larger energy gap. SiC is classified as a wide-band-gap (WBG) material, and it is the mainstream material for power semiconductors [25, 26]. Among the different types of power semiconductors, the power diode was the best device to adopt SiC technology. The main advantage of SiC is high-breakdown voltage and reverse-recovery current is small [27–29]. As a result, higher efficiency and higher power density can be brought to power electronic

FIGURE 1: Equivalent circuit of solar PV module.

systems in different applications [30, 31]. In this research, a new active snubber circuit is proposed to contrive a new family of PWM converters. This proposed circuit provides perfectly ZVT turn on and ZCT turn off together for the main switch of a converter by using only one quasiresonant circuit without an important increase in the cost and complexity of the converter. This paper proposes to implement Chaotic PWM as a control method to improve the steady state performance of the DC-DC SEPIC converter based MPPT system for solar PV module. The nominal duty cycle of the main switch of DC-DC SEPIC converter is adjusted so that the solar panel output impedance is equal to the input resistance of the DC-DC converter which results in better spectral performance in the tracked voltages when compared to conventional PWM control. The conversion efficiency of the proposed MPPT system is increased when CPWM is used; this will be compared with parallel boost converter. Multilevel inverters are promising as they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [29].

2. MATLAB Model of L1235-37W Solar PV Module

The output characteristics of the solar PV module depend on the irradiance and the operating temperature of the cell. The equivalent circuit of PV module is shown in Figure 1.

From Figure 1, the current and voltage equation is given by

$$\begin{aligned} I_{sc} &= I_D + I_{PV} + \left(\frac{V_D}{R_p} \right), \\ V_{PV} &= V_D - (I_{PV} * R_s), \end{aligned} \quad (1)$$

where diode current is $I_D = I_o + (e^{(V_D/V_T)} - 1)$.

Based on the electrical equation (1) and the solar PV module are modelled in MATLAB as shown in Figure 2, which is used to enhance the understanding and predict the V - I characteristics and to analyze the effect of temperature and irradiation variation. If irradiance increases, the fluctuation of the open-circuit voltage is very small. But the short circuit

FIGURE 2: MATLAB model for PV module.

FIGURE 3: L1235-37W solar module under test.

current has sharp fluctuations with respect to irradiance. However, for a rising operating temperature, the open-circuit voltage is decreased in a nonlinear fashion [4].

The V - I characteristics are validated experimentally in the L1235-37Wp solar module as shown in Figure 3. The technical specifications of L1235-37Wp solar module under test are given in Table 1. Figure 4 shows the V - I characteristics of L1235-37Wp which is based on the experimental results under irradiation (G) = 1000 W/m² and temperature = 25°C.

2.1. Space Modelling of SEPIC Converter Input at MPP. The relation between input and output currents and voltage are given by

$$\begin{aligned} \frac{V_{OUT}}{V_{IN}} &= \frac{D}{(1-D)}, \\ \frac{I_{IN}}{I_{OUT}} &= \frac{D}{(1-D)}. \end{aligned} \quad (2)$$

The duty cycle of the SEPIC converter under continuous conduction mode is given by

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D}. \quad (3)$$

TABLE 1: Specifications of L1235-37W solar PV panel.

Short circuit current (I_{sc})	2.5 A
Voltage at MPP (V_m)	16.4
Current at MPP (I_m)	2.25
Open circuit voltage (V_{oc})	21 V
Length	645 mm
Width	530 mm
Depth	34 mm
Weight	4 kg
Maximum power (P_{max})	37 W

FIGURE 4: V - I characteristics of L 1235-37W solar panel.

V_D is the forward voltage drop across the diode (D). The maximum duty cycle is

$$D_{max} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D}. \quad (4)$$

The value of the inductor is selected based on the below equations

$$L_1 = L_2 = L = \frac{V_{IN(MIN)} * D_{max}}{\Delta I_L * f_s}. \quad (5)$$

ΔI_L is the peak-to-peak ripple current at the minimum input voltage and f_s is the switching frequency. The value of C_1 depends on RMS current, which is given by

$$I_{C_1(\text{RMS})} = I_{\text{OUT}} * \sqrt{\frac{V_{\text{OUT}} + V_D}{V_{\text{IN}(\text{MIN})}}}. \quad (6)$$

The voltage rating of capacitor C_1 must be greater than the input voltage. The ripple voltage on C_1 is given by

$$\Delta V_{C_1} = \frac{I_{(\text{OUT})} * D_{\text{max}}}{C_1 * f_s}. \quad (7)$$

The parameters governing the selection of the MOSFET are the minimum threshold voltage $V_{\text{th}(\text{min})}$, the on-resistance $R_{\text{DS(ON)}}$, gate-drain charge Q_{GD} , and the maximum drain to source voltage $V_{\text{DS(max)}}$. The peak switch voltage is equal to $V_{\text{IN}} + V_{\text{OUT}}$. The peak switch current is given by

$$I_{Q_1(\text{Peak})} = I_{L_1(\text{PEAK})} + I_{L_2(\text{PEAK})}. \quad (8)$$

The RMS current is given by

$$I_{Q_1(\text{RMS})} = I_{\text{OUT}} \sqrt{(V_{\text{OUT}} + V_{\text{IN}(\text{MIN})}) * \frac{V_{\text{OUT}}}{V_{\text{IN}(\text{MIN})}^2}}. \quad (9)$$

The total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss (as shown in the second term). I_G is the gate drive current. The $R_{\text{DS(ON)}}$ value should be selected at maximum operating junction temperature and is typically given in the MOSFET datasheet

$$P_{\text{switch}} = (I_{Q_1(\text{RMS})} * R_{\text{DS(ON)}} * D_{\text{MAX}}) + (V_{\text{IN}(\text{MIN})} + V_{\text{OUT}}) * I_{Q_1(\text{Peak})} * \frac{(Q_{\text{GD}} * f_s)}{I_G}. \quad (10)$$

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC converter, the diode peak current is the same as the switch peak current $I_{Q_1(\text{Peak})}$. The minimum peak reverse voltage the diode must withstand is

$$V_{\text{RD}} = V_{\text{IN}(\text{MAX})} + V_{\text{OUT}(\text{MAX})}. \quad (11)$$

2.2. Dynamic Input Characteristics of a SEPIC Converter at MPP. The input voltage and the equivalent input resistance of the converter are V_s and R_i , respectively. As the input power ρ_i to the converter is equal to the output power ρ_o of the solar PV module

$$\rho_i = \rho_o = \frac{V_s^2}{R_i}. \quad (12)$$

The rate of change ρ_i with respect to V_s and R_i can be shown below

$$\partial \rho_i = \frac{2V_s}{R_i} \partial V_s - \frac{V_s^2}{R_i^2} \partial R_i. \quad (13)$$

At the MPP, the rate of change of ρ_i equals zero and $R_i = r_g$

$$\partial \rho_i = 0, \quad \text{hence} \quad \frac{\partial V_s}{\partial R_i} = \frac{V_s}{2R_i}. \quad (14)$$

The equation gives the required dynamic resistance characteristics of the tracker at MPP.

2.3. Generation of Chaotic PWM. In order to improve the steady state performance of solar powered system, direct control Chaotic Pulse width modulated (CPWM) SEPIC converter is proposed to track maximum power from solar PV module. Therefore, in order to get chaotic frequency f_Δ or chaotic amplitude A_Δ , chaos-based PWM (CPWM) is analyzed to generate chaotic PWM. The MATLAB simulation is carried out as shown in Figure 5. The analogue chaotic PWM has its advantages over the digital in its low costs and easy-to-design, making it suitable for high-frequency operation and situations when design flexibility, high converter conversion efficiency, and low cost. In order to generate chaotic pulse width modulation, Chua's diode is used to trigger the main switch of SEPIC converter and to be used for reducing spectral peaks in tracked converter voltage.

The CPWM adopts sawtooth to modulate, but its carrier period T'_Δ changes according to

$$T'_\Delta = \frac{X_i}{\text{Mean}(x)} * T_\Delta, \quad (15)$$

where T_Δ is invariant period, X_i , $i = 1, 2, \dots, N$, a chaotic sequence, $x = (x_1, x_2, \dots, x_N)$, and $\text{Mean}(x)$ average of the sequence defined as

$$\text{Mean}(x) = \lim_{N \rightarrow \infty} \sum_{i=1}^N |X_i| \frac{1}{N}; \quad N \rightarrow \infty. \quad (16)$$

Similarly the CPWM also adopts sawtooth to modulate, but its carrier amplitude A'_Δ changes according to

$$A'_\Delta = \left\{ 1 + K \frac{X_i}{\text{Mean}(x)} \right\} A_\Delta, \quad (17)$$

where A_Δ is the invariant amplitude, X_i , $i = 1, 2, \dots, N$, a chaotic sequence, $x = (x_1, x_2, \dots, x_N)$ and $\text{Mean}(x)$, average of the sequence, and K is the modulation factor of the amplitude which can be set required in practice. The value of K is selected as low so that the ripple in the output voltage of the SEPIC converter is low. Also the ripple in the output voltage controlled by chaotic PWM is low. The analog chaotic carrier is generated based on the circuit; the resistances ($R_{d1} \dots R_{d6}$) are used to realise linear resistor called Chua diode. The parameters for Chua's diode are designed and chosen as $R_{d1} = 2.4 \text{ k}\Omega$, $R_{d2} = 3.3 \text{ k}\Omega$, $R_{d3} = R_{d4} = 220 \Omega$, and $R_{d5} = R_{d6} = 20 \text{ k}\Omega$. The other parameters of Chua's oscillator used in the experiment are $L_1 = 2.2 \text{ mH}$, $C_1 = 4.7 \text{ nF}$, $C_2 = 500 \text{ pF}$, and $R = 1.75 \text{ K}\Omega$.

FIGURE 5: Chaotic PWM pulse generation.

FIGURE 6: Hardware setup.

FIGURE 7: Chaotic PWM.

2.4. Experimental Setup: Standalone PV System. Figure 6 shows the experimental setup of the proposed SEPIC converter-based MPPT for solar PV module, which is constituted by a power stage and a control circuit. The power stage includes an inductor L_1, L_2 , capacitor C_1, C_2 , a switch S , a load resistance, and a solar PV module (L1235-37Wp). The analog chaotic carrier is generated based on the hardware output of CPWM is in Figure 7.

3. Mathematical Model for Parallel Boost Converter with Active Snubber Circuit

Figure 12 represents the circuit diagram of the parallel boost converter with active snubber. It consists of five inductors $L_{f1}, L_{f2}, L_{R1}, L_{R2}, L_n$ and three capacitors C_s, C_r, C_o . V_g and V_o represents supply and output voltage, respectively; S (S_1, S_2) is an active primary switch, D (D_{f1}, D_{f2}) is a free-wheeling diode, D_s (D_1, D_2, D_3) is a Snubber diode, and R_L is the load resistance. S (S_1, S_2, S_3) operates at a switching frequency f_s with duty ratio d .

Choose the switching frequency of switches $S_1 = S_2 = 100$ KHz and $S_3 = 200$ KHz.

When $S_1 = S_2 = 0$ and $S_3 = 1$ as in Figure 8

$$\begin{aligned} \frac{diL_F}{dt} &= \frac{1}{L_F} [V_g = V_o], \\ \frac{dV_o}{dt} &= \frac{1}{C_o} \left[iL_F - \frac{V_o}{R_L} - iL_S \right]. \end{aligned} \quad (18)$$

Also the switches $S_1 = S_2 = S_3 = 1$ as in Figure 9

$$\begin{aligned} \frac{diL_F}{dt} &= \frac{1}{L_F} [V_g - V_o], \\ \frac{dV_o}{dt} &= \frac{1}{C_o} \left[iL_F - \frac{V_o}{R_L} \right]. \end{aligned} \quad (19)$$

Similarly, the switches $S_1 = S_2 = 1$ and $S_3 = 1$ or 0 as in Figure 10

$$\begin{aligned} \frac{diL_F}{dt} &= \frac{V_g}{L_F}, \\ \frac{dV_o}{dt} &= \frac{1}{C_o} \left[-\frac{V_o}{R_L} \right]. \end{aligned} \quad (20)$$

FIGURE 8: When $S_1 = S_2 = 0$ and $S_3 = 1$. FIGURE 9: When $S_1 = S_2 = S_3 = 1$.

By using state-space averaging method the state equations during switch-on and switch-off conditions are

$$\begin{aligned}\dot{x}_1 &= \frac{-(1-d_1)}{L_F}x_2 - \frac{(1-d_2)}{L_F}x_2 + \frac{V_g}{L_F}, \\ \dot{x}_2 &= \frac{-1}{R_L C_o}x_2 + \frac{(1-d_1)d_2}{C_o}x_1 + \frac{(1-d_1)(1-d_2)}{C_o}x_1,\end{aligned}\quad (21)$$

where x_1 and x_2 are the moving averages of i_{LF} and V_o , respectively.

4. Proposed Parallel Boost Converter for PV Application

Figure 11 shows the Block Diagram of PV based parallel boost converter with active snubber. It is the combination of new active snubber circuit with parallel boost converter. Three switches S_1 , S_2 , and S_3 are used; S_1 and S_2 act as main switch and S_3 acts as an auxiliary switch. S_1 and S_2 are controlled by ZVT and ZCT, respectively; also S_3 is controlled by ZCS. This circuit operates with the input of solar power.

Assume both the main switches (S_1 and S_2) operate in the same frequency. The features of proposed parallel boost converter are as follows.

- (i) All the semiconductors work with soft switching in the proposed converter.
- (ii) The main switches S_1 and S_2 turn on with ZVT and turn off with ZCT.
- (iii) The secondary switch is turned on with ZCS and turned off with ZCS.

FIGURE 10: When $S_1 = S_2 = 1$ and $S_3 = 1$ or 0.

- (iv) All other components of the parallel boost converter functions based on this soft switching.
- (v) There is no additional current or voltage force on the main switches S_1 and S_2 .
- (vi) There is no additional current or voltage force on the secondary switch S_3 .
- (vii) Also there is no additional current or voltage force on the main diodes D_{f1} and D_{f2} .
- (viii) According to the ratio of the transformer, a part of the resonant current is transferred to the output load with the coupling inductance. So there is less current stress on the secondary switch with satisfied points.
- (ix) At resistive load condition, in the ZVT process, the main switches voltage falls to zero earlier due to decreased interval time and that does not make a problem in the ZVT process for the main switch.
- (x) At resistive load condition, in the ZCT process, the main switches body diode on state time is increased when the input current is decreased. However, there is no effect on the main switch turn off process with ZCT.
- (xi) This parallel boost converter operates in high-switching frequency.
- (xii) This converter easily controls because the main and the auxiliary switches are connected with common ground.
- (xiii) The most attractive feature of this proposed converter is using ZVT and ZCT technique.
- (xiv) The proposed new active snubber circuit is easily adopted with other basic PWM converters and also switching converters.
- (xv) Additional passive snubber circuits are not necessary for this proposed converter.
- (xvi) SIC (silicon carbide) is used in the main and auxiliary diodes, so reverse recovery problem does not arise.
- (xvii) The proposed active snubber circuit is also suitable for other DC-DC converters.

4.1. Procedure for Constructing a Proposed Converter. Steps to obtain a system level modeling and simulation of proposed power electronic converter are listed below.

FIGURE 11: Block diagram of PV based parallel boost converter with active snubber.

TABLE 2: Specification of parallel boost converter with active Snubber.

Main inductor L_{f1}	750 μ H
Main inductor L_{f2}	750 μ H
Upper Snubber inductor L_{R1}	5 μ H
Lower Snubber inductor $L_{R2} (L_m + L_d)$	2 μ H
Magnetization inductor $L_M (L_n + L_{ol})$	3 μ H
Parasitic capacitor C_s	1 μ F
Snubber capacitor C_R	4.7 nF
Output capacitor C_o	330 μ F/450 V
Output load resistance $R = R_L$	530 Ω

- (i) Determine the state variables of the proposed power circuit in order to write its switched state-space model, for example, inductance current and capacitance voltage.
- (ii) Assign integer variables (ON-1 and OFF-0 state) to the proposed power semiconductor to each switching circuit.
- (iii) Determine the conditions controlling the states of the proposed power semiconductors or the switching circuit.
- (iv) Assume the main operating modes, apply Kirchhoff's Current law and Kirchhoff's Voltage law and combine all the required stages into a switched state-space model, which is the desired system-level of the proposed model.
- (v) Implement the derived equations with MATLAB Simulink.
- (vi) Use the obtained switched space-state model to design linear or nonlinear controllers for the proposed power converter.

The algorithm for solving the differential equations and the step size should be chosen before running any simulation. This step is only suitable in closed-loop simulations [21].

4.2. Operation of Proposed Boost Converter with Snubber Circuit. The proposed PV based converter is shown in Figure 12, and it is based on a dual boost circuit where the first one (switch S_1 and choke L_{f1}) is used as main chock of boost converter circuit and where the second one (switch S_2 and choke L_{f2}) is used to perform an active filtering. The proposed converter applies active snubber circuit for soft switching. This snubber circuit is built on the ZVT turn on and ZCT turn off processes of the main switches. Specification of proposed parallel boost converter with active snubber is in Table 2.

The power from the solar flows through the two parallel paths. High efficiency was obtained by this method. So as to reach soft switching (SS) for the main and the auxiliary switches, main switches turn on with ZVT and turn off with ZCT. The proposed converter utilizes active snubber circuit for SS. This snubber circuit is mostly based on the ZVT turn on and ZCT turn off processes of the main switch. L_{R2} value is limited with $(V_{out}/L_{R2})t_{rise}S_2 \leq I_{i\max}$ to conduct maximum input current at the end of the auxiliary switch rise time ($t_{rise}S_2$) and $L_{R1} \geq 2L_{R2}$. To turn off S_1 with ZCT, the duration of t_{ZCT} is at least longer than fall time of S_1 ($t_{fall}S_1$) $t_{ZCT} \geq t_{fall}S_1$. Though the main switches are in off state, the control signal is functional to the auxiliary switch. The parasitic capacitor of the main switch should be discharged absolutely and the main switches antiparallel diode should be turned on. The on state time of the antiparallel diode is named t_{ZVT} and in this time period, the gate signal of the main switch would be applied. So, the main switch is turned on below ZVS and ZCS with ZVT.

Whereas the main switches are in on state and ways input current, the control signal of the auxiliary switch is applied. After the resonant starts, the resonant current should be higher than the input current to turn on the antiparallel diode of the main switch. The on state time of the antiparallel diode (t_{ZCT}) has to be longer than the main switches fall time ($t_{f_{S1}}$). After all these terms are completed, while antiparallel diode is in on state, the gate signal of the main switch should be cutoff to provide ZCT for the main switch. Auxiliary switch turn on with ZCS and turn off with ZCS. The auxiliary switch is turned on with ZCS for the coupling inductance limits the current rise speed.

FIGURE 12: Circuit diagram of PV based parallel boost converter with active snubber with resistive load.

The current passing through the coupling inductance must be partial to conduct maximum input current at the end of the auxiliary switch rise time (t_{rs3}). So, the turn on process of the auxiliary switch with ZCS is offered. To turn off the auxiliary switch with ZCS, though the auxiliary switch is in on state, the current passing through the switch should fall to zero with a new resonant. Then, the control signal can be cutoff. If C_S is ignored, L_{R1} value should be two times added with L_{R2} to make the auxiliary switch current fall to zero. As the current cannot stay at zero as long as the auxiliary switch fall time (t_{fs3}), the auxiliary switch is turned off nearly with ZCS.

The proposed Simulink topology is shown in Figure 13. The inductors L_{f1} and L_{f2} have the similar values, the diodes D_{f1} - D_{f2} are at the same type and the same guess was for the switches (S_1 & S_2). All the inductors have individual switches and they resemble paralleling of classic converters.

5. Design of MLI Module

A multilevel converter is a power electronic system that synthesizes a desired output voltage levels from the DC inputs supply. Compared with the traditional two-level voltage converter, the primary advantage of multilevel converters is their smaller output voltage step, which results in high power quality, lower harmonic components, better electromagnetic compatibility, and lower switching losses. The functionality verification of the simplified seven-level inverter is done using MATLAB simulation which is shown in Figure 14.

This single-phase simplified seven-level inverter was developed using a single-phase full bridge (H-bridge) inverter, two bidirectional auxiliary switches, and a capacitor voltage divider formed by C_1 , C_2 , and C_3 , as shown in Figure 14. The simplified multilevel inverter topology is

TABLE 3: Switching pattern for the single-phase seven-level inverter.

V_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	1	0	0	1	0	0
$2V_{dc}/3$	0	0	0	1	1	0
$V_{dc}/3$	0	0	0	1	0	1
0	0	0	1	1	0	0
0^*	1	1	0	0	0	0
$-V_{dc}/3$	0	1	0	0	1	0
$-2V_{dc}/3$	0	1	0	0	0	1
$-V_{dc}$	0	1	1	0	0	0

significantly advantageous over other topologies. The advantages of simplified topology are requirement of less power switch, power diodes, and less capacitors for this inverter. Photovoltaic arrays were connected to the inverter via a DC-DC SEPIC converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The DC-DC SEPIC converter was required because the PV arrays had a voltage that was lower than the grid voltage. High DC bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance L_f was used to filter the current injected into the grid. Proper switching of the inverter can produce seven levels of output-voltage (V_{dc} , $2V_{dc}/3$, $V_{dc}/3$, 0, 0^* , $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$) from the DC supply voltage. Table 3 shows the switching pattern for the single-phase simplified seven-level inverter.

6. Grid-Connected Solar Power System

The modelling and simulation of PV, MPPT, CPWMSEPIC converter, simplified seven-level MLI, and controller had

FIGURE 13: Simulink model of proposed PV based parallel boost converter with active snubber circuit with MLI.

FIGURE 14: Simulated model for seven-level inverter.

been carried out in MATLAB Simulink environment. The basic block diagram of reliable high efficient grid-connected solar power system has been shown in Figure 15.

The grid-connected PV system consists of MPPT tracking using SEPIC converter which is used to track the maximum voltage. The tracked voltage is boosted in to 325 V. A simplified seven-level MLI is designed to convert into an AC voltage with seven levels which should connect to grid. The simulated results for the MLI output are in Figures 16 and 17.

7. Results and Discussions

A modular solar PV based DC-DC converter using parallel boost converter with active filter of the proposed system is simulated using MATLAB Simulink program. The waveforms of parallel boost converter voltage and MLI filtered output voltage is shown in Figures 18 and 19. The control signals of the switches are shown in Figures 20 and 21, respectively. The simulation results show the proposed PV based soft switched parallel boost DC-DC converter has the proper response. The detailed comparison of SEPIC and parallel boost converter is in Table 4.

TABLE 4: Comparison of SEPIC and parallel boost converter.

Parameters	SEPIC converter	Parallel boost converter
Duty cycle	45%	47%
No. of switches	7	9
Input	148	148
Output	325 V	448 V
Efficiency	92.15%	98.7%

8. Conclusion

The behaviour of solar module (L1235-37Wp) is studied. The maximum power is extracted from solar PV module using CPWM and PWM for different converters. The spectrum performance is improved when CPWM control is used for MPPT purposes. The performance of MLI is studied and the proto type model of MLI is carried out. The main objective of this research was to improve efficiency of the solar PV based parallel boost converter and reduce the switching losses. Simulations were initially done for conventional boost converter with snubber circuit. The changes in the input current waveform were obtained. A parallel boost converter

FIGURE 15: Block diagram of reliable high efficient grid-connected solar power system.

Time offset: 0

FIGURE 16: MLI output current.

Time offset: 0

FIGURE 19: MLI filtered output voltage (V_o).

Time offset: 0

FIGURE 17: MLI output voltage.

Time offset: 0

FIGURE 20: Control signals of switches S_1 and S_2 .

Time offset: 0

FIGURE 18: Parallel boost converter output voltage.

Time offset: 0

FIGURE 21: Control signals of switch S_3 .

was designed with soft switching which is provided by the active snubber circuit. The main switches and all the other semiconductors were switched by ZVT and ZCT techniques. The active snubber circuit was applied to the parallel boost converter, which is fed by solar input line. This latest converter was achieved with 148 V input. Due to the main and the auxiliary switches have a common ground, the converter was controlled easily. The proposed new active snubber circuit can be simply functional to the further basic PWM converters and to all switching converters thereby increasing efficiency and improving output voltage.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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