Editorial

Selected Papers from ReConFig 2008

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The fourth edition of the International Conference on Reconfigurable Computing and FPGAs (ReConFig 2008) was held in Cancun, Mexico, from December 3 to 5, 2008. ReConFig is a Leading edge forum for researchers and engineers across the world to present their latest research and to discuss future research and applications. The conference seeks to promote the use of reconfigurable computing and FPGA technology for research, industry, education, and applications.

This special issue covers actual and future trends on reconfigurable computing given by academic and industrial specialists from all over the world. Papers presented in this special issue were selected from all ReConFig 2008 submissions and were peer reviewed for the final publication in this journal with the breadth and depth needed for readers involved in the reconfigurable computing field.

There are a total of 12 articles in this issue. We begin the special issue with two papers that extend across the digital signal processing domain. The paper by G. Caffarena et al. "Architectural synthesis of fixed-point datapaths using FPGAs" addresses the automatic synthesis of fixed-point datapaths by combining a multiple wordlength approach with a wise mapping of operations to the embedded FPGA resources leading improvements around 50%. In "Pipeline FFT architectures optimized for FPGAs," by B. Zhou et al. optimized implementations of two pipeline FFT processors using general optimization and architecture-specific optimizations and different rounding schemes to achieve better performances with lower resources than previous works.

Four papers are within the broad area of automated design and multiprocessors systems on chips. The paper by H. Ishebebi et al. presents an automated design approach for multiprocessor systems on FPGAs which customizes architectures for parallel programs by simultaneously solving the

problems of task mapping, resource allocation, and scheduling. Results show performance improvements by three orders of magnitude highlighting the potential for solving difficult instances of automated synthesis. In a second paper, "An ILP formulation for the task graph scheduling problem tailored to bi-dimensional reconfigurable architectures," by F. Redaelli et al. proposes an exact ILP formulation for the task scheduling problem on a 2D dynamically and partially reconfigurable architecture taking into account physical constraints of the target device. Also, this work proposes a reconfiguration-aware heuristic scheduler in an HW/SW codesign method reducing the schedule length of application by a factor of 2 in the best case. M. Saldaña et al., in "A message-passing hardware/software co-simulation environment for reconfigurable computing systems," address the need for cosimulating a complete heterogeneous application in high-performance configurable computers by providing a message-passing simulation framework to simulate and develop an interface enabling an MPI-based approach to exchange data between $\times 86$ processors and hardware engines embedded in FPGAs. The development, exploration, and validation methodology of real-time operating systems for reconfigurable Systems-on-Chip is covered in "OverSoC: a framework for the exploration of RTOS for RSoC platforms," by Benoît Miramond. They present a method for the distribution of operating services on such platforms with an accurate modeling of the dynamic and deterministic behavior of applications and RTOs.

Three articles are presented in the area of algorithms and implementations mapped on reconfigurable hardware. J. H. B. Zambrano et al. in "Parallel processor for 3D recovery from optical flow" present a parallel processor for 3D recovery from optical flow under real-time constraints. The

presented design exhibits a good trade-off between hardware resource usage, image resolution, and the processing speed. S. Lloyd et al. in “Hardware accelerated sequence alignment with traceback” present a space-efficient, global sequence alignment algorithm and 256 processing elements architecture to speedup sequence alignment used in molecular biology and biomedical applications. Performance gains over 300 times that of a desktop computer demonstrated showing the potential to analyze genetic data in a timely manner. B. Girau et al. in “Reaction-diffusion and chemotaxis for decentralized gathering on FPGAs,” describe the feasibility of gathering multiple computational units by means of decentralized and simple local rules by a stochastic model and discuss a fully parallel hardware implementation so as to study its ability to provide a massively distributed computational model for decentralized gathering.

The next article, by Y.-H.E. Yang et al., “Software toolchain for large-scale RE-NFA construction on FPGA,” presents a toolchain which automates the construction and optimizations of regular expression matching engines (REMEs) on FPGA. The automated REME optimizations include centralized character classifications, multicharacter matching, and staged pipelining. Also, authors designed a benchmark generator which can produce RE-NFAs with configurable pattern complexity parameters, including state count, state fan-in, loop-back, and feed-forward distances. A. Mendon et al. in “A hardware filesystem implementation with multi-disk support,” describes a file system implementation with four basic operations (open, read, write, and delete) and the potential of improving the performance of data-intensive applications by connecting secondary storage directly to FPGA compute accelerator. Last but not least, the article “Analysis and enhancement of random number generator in FPGA based on oscillator rings” by Knut Wold addresses the fast implementation of a true random number generator into an FPGA device. The proposed implementation passes the standard statistical test without postprocessing showing good quality randomness characteristics. The throughput of the TRNG is 100 Mbps and the resources used in the FPGA are less than 100 logic elements in an Altera Cyclone II FPGA.

We sincerely thank authors for their valuable contributions and all reviewers for their help to ensure the quality of this special issue. We hope that you enjoy the articles in the ReConFig 2008 special issue and find its contents useful and give readers a good idea of where researchers have been focusing, both on long-studied problems still needing more work and on newer challenges.

Please stay tuned for the coming issues of the International Journal on Reconfigurable Computing and FPGAs.

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