Editorial

Selected Papers from ReconFig 2009 International Conference on Reconfigurable Computing and FPGAs (ReconFig 2009)

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The fifth edition of the International Conference on Reconfigurable Computing and FPGAs (ReConFig 2009) was held in Cancun, Mexico, from December 9 to 11, 2009. ReConFig is a leading edge forum for researchers and engineers across the world to present their latest research and to discuss future research and applications. The conference seeks to promote the use of reconfigurable computing and FPGA technology for research, industry, education, and applications.

This special issue covers actual and future trends on reconfigurable computing given by academic and industrial specialists from all over the world. Papers presented in this special issue were selected from all ReConFig 2009 submissions and were peer reviewed for the final publication in this journal with the breadth and depth needed for readers involved in the reconfigurable computing field.

There are a total of 15 articles in this issue. We begin the special issue with two papers that extend across the digital signal processing domain, and especially Software Define Radio. The paper by J. A. Surís et al. "*RapidRadio: A Domain-Specific Productivity Enhancing Framework*" addresses a framework enhancing tool reducing the required knowledge base for implementing a receiver on an FPGA-based SDR platform. In "*Space-Based FPGA Radio Receiver Design, Debug, and Development of a Radiation-Tolerant Computing System*," Z. K. Baker et al. proposed a processing capability which enables very advanced algorithms such as wideband RF compression scheme to operate at the source, allowing bandwidth-constrained applications to deliver previously unattainable performance.

Three papers are within the area of arithmetic applied to digital signal processing. The paper by M. Baesler et al.

presents a new parallel decimal fixed-point multiplier designed to exploit the features of Virtex-5 FPGA in order to provide important operation with least possible rounding error.

In the next paper, "*Partial Reconfigurable FIR Filtering System Using Distributed Arithmetic*," D. Llamocca et al. propose two efficient dynamic partial reconfiguration systems allowing to implement a wide range of 1D FIR filters. For both systems, the required partial reconfiguration region is kept small by using distributed arithmetic implementations. R. A. Arce-Nazario et al., in "*Reconfigurable Hardware Implementation of a Multivariate Polynomial Interpolation Algorithm*," address a new methodology based on Lagrange interpolation. The generalized algorithm can be efficiently mapped to a systolic array in which each processing cell implements a pair of binary operations between an incoming and a stored value. The FPGA implementation of the reduction operations and the complete application achieved speedups of up to 172× and 67×, respectively, as compared to software implementations run on a contemporary CPU, with moderate resource utilization.

Five papers are within the broad area of automated design and multiprocessors systems on chips. As discussed in "*Reconfigurable Multiprocessor Systems: a Review*" by T. Dorta et al., run-time reconfigurability uses the dynamic reconfiguration feature of FPGAs to obtain a new degree of freedom in the design of multiprocessor systems, making these systems more flexible to target different applications using the same hardware. L. Kirischian et al. propose in "*Mechanism of Resource Virtualization in RCS for Multitask Stream Applications*" a mechanism for the virtualization

of computing resources for multitask and multi-mode stream applications. The comparative analysis made on the Multitask Adaptive Reconfigurable System demonstrated negligible hardware overhead offset by sufficient gains in the main performance parameters. Memory access is a key point for modern design. In “*Traversal Caches: A Framework for FPGA Acceleration of Pointer Data Structures*,” J. Coole and G. Stitt introduce an original traversal cache framework that enables efficient FPGA execution of applications with irregular memory access patterns. Such approach greatly improves effective memory bandwidth for repeated traversals. The next paper describes the way to make the reconfigurable resources available for all applications in the embedded systems domain, particularly mobile devices or networked devices where the requirements change. S. Döbrich and C. Hochberger show that the AMIDAR concept allows providing a general-purpose processor that can automatically take advantage of reconfigurable resources. The last paper of this section, “*3D Network-on-Chip Architectures using Homogeneous Meshes and Heterogeneous Floorplans*,” by V. de Paulo and C. Ababei proposed original 3D 2-layer and 3-layer NoC architectures using homogeneous networks on a separate layer and heterogeneous floorplans on different layers. A design methodology that consists of floorplanning, routers assignment, and cycle-accurate NoC simulation was implemented and utilized to investigate new architectures.

One domain addressed by this special issue is how security should be considered into FPGA architecture. For this reason 3 papers are dealing with this exciting domain. The paper of L. Sauvage et al., “*Exploiting Dual-Output Programmable Blocks to Balance Secure Dual-Rail Logics*,” proposes a new logic, dedicated to FPGA, robust against side channel attacks. The presented approach gave evidence that differential placement and routing of an FPGA implementation can be done with a granularity fine enough to improve the security gain. One major issue in security concerns the way to generate true random number. The paper “*True-Randomness and Pseudo-Randomness in Ring Oscillator-Based True Random Number Generators*,” by N. Bochard et al. deals with true random number generators employing oscillator rings. A mathematical analysis, a simulation model, and FPGA implementations are discussed in depth. The last paper concerning security “*Proof-Carrying Hardware: Concept and Prototype Tool Flow for Online Verification*” by S. Drzevitzky et al. elaborates on the discussion of proof-carrying hardware (PCH) as a novel approach to reconfigurable system security. PCH takes a key concept from software security, known as proof-carrying code, into the reconfigurable hardware domain.

The last two papers show how FPGA could be efficiently used for robotics applications. The first paper proposed by J. Kalomiros and J. Lygouras “*Robotic Mapping and Localization with Real-Time Dense Stereo on Reconfigurable Hardware*” discusses about a new reconfigurable architecture for dense stereo and an observation framework for a real-time implementation of the simultaneous localization and mapping problem in robotics. The second paper “*A Reconfigurable System Approach to the Direct Kinematics of a 5 D.o.f Robotic Manipulator*” by D. F. Sánchez et al. describes

an FPGA implementation of kinematics of a spherical robot manipulator using floating-point units operators. The proposed architecture was designed using a Time-Constrained Scheduling. Synthesis results show that the proposed hardware architecture for direct kinematics of robots is feasible in modern FPGAs families.

We hope you enjoy reading these papers, related to reconfigurable computing, and will serve the community to share new results in this field of research.

We sincerely thank authors for their valuable contributions and all reviewers for their help to ensure the quality of this special issue. We hope that you enjoy the articles in the ReConFig 2009 special issue and find its contents useful and give readers a good idea of where researchers have been focusing, both on long-studied problems still needing more work and on newer challenges.

Please stay tuned for the coming issues of the International Journal on Reconfigurable Computing and FPGAs.

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