Editorial

Selected Papers from SPL 2009: Programmable Logic and Applications

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Basically, FPGA devices contain programmable logic blocks and a hierarchy of programmable interconnects that allow data routing between the blocks and to the output pins. In this way FPGAs can be used to implement any logical function that an ASIC could perform. Furthermore, the ability to update the functionality after shipping and the low nonrecurring engineering costs relative to an ASIC design, offers advantages for many applications. Many emerging applications in communications, computing, and consumer electronics industries demand that their functionality stays flexible after the system has been manufactured. Such flexibility is required in order to cope with changing user requirements, improvements in system features, changing protocols and data-coding standards, demands to support variety of different user applications, and so forth. Like microprocessors, RAM-based FPGAs can be infinitely reprogrammed. Design revisions, even for a fielded product, can be implemented quickly and painlessly. Nowadays the FPGA market is a \$2.75 billion one, with more than 100,000 designs starting in 2010.

The interest on FPGAs is reflected in several first class conferences on programmable logic around the world and the number of papers published by the research community. The Southern Conference on Programmable Logic (SPL, <http://www.splconf.org/>) is the austral meeting point for researchers interested in FPGA technology. Started in 2005, SPL has since 2007 the technical cosponsorship of the IEEE Circuits and Systems Society (CAS). The selection of articles presented in this special issue is coming from the last SPL conference (V Southern Conference on Programmable Logic), held in São Carlos, Brazil, during April 1 to 3, 2009.

Thirty two researchers helped us in the revision process to select the final seven contributions. The issue begins with a paper by Hanyu Liu and Ali Akoglu, “Timing-driven non-uniform Depopulation Based Clustering” where a timing-driven nonuniform depopulation-based clustering technique that targets critical path delay and channel width constraints simultaneously is presented. Next, in “Flexible interconnection network for dynamically and partially reconfigurable architectures” L.Devaux et al. study various communication architectures in the context of dynamic reconfiguration, in particular interconnection networks. In “Parameterized hardware design on reconfigurable computers: an image processing case study” M.Huang et al. show how the speedup a reconfigurable computer can reach depends on the intrinsic parallelism of the target application as well as the characteristics of the target platform.

Yuet Ming Lam et al. in “Multi-loop parallelisation using unrolling and fission” present a technique for parallelising multiple loops in a heterogeneous computing system. Experimental results show that a maximum speedup of 34 is achieved on a 274 MHz FPGA for the N-Body over a 2.6 GHz microprocessor, which is 4.1 times higher than an approach without unrolling. “Power characterisation for fine-grain reconfigurable fabrics” by Tobias Becker et al. presents a benchmarking methodology for characterising the power consumption of the fine-grain fabric in reconfigurable architectures.

In “High speed FPGA 10’s complement adders-subtractors” Gery Bioul et al. redesign BCD adders to fit within FPGA’s platforms with promising results that enable this technology to implement new decimal floating-point

cores according to the IEEE 754-2008 standard. Finally, in “Concurrent calculations on reconfigurable logic devices applied to the analysis of video images” Sergio Geninatti et al. present the design and implementation of an algorithm for computing similarities between neighbouring frames in a video sequence using luminance information on FPGA.

We would like to express our sincere thanks to the reviewers for their hard work, to Dr. René Cumplido, the Editor-in-Chief, and to the editorial staff of Hindawi. We hope that you enjoy this special issue and that it inspires more research to overcome future challenges in the areas related to programmable logic.

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