Editorial

Selected Papers from the 17th Reconfigurable Architectures Workshop (RAW2010)

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This special issue of IJRC includes papers selected from the 17th Reconfigurable Architectures Workshop (RAW 2010) held in Atlanta, GA, USA, in April 29-30, 2010. RAW 2010 was associated with the 24th Annual International Parallel & Distributed Processing Symposium (IPDPS 2010) and was sponsored by the IEEE Computer Society Technical Committee on Parallel Processing. The workshop is one of the major meetings for researchers and practitioners to present ideas, results, and ongoing research, on both theoretical and practical advances in reconfigurable computing.

The program of RAW 2010 provided a venue to facilitate creative and productive interaction between most disciplines of reconfigurable computing. High-quality research papers, focusing models and architectures, devices, algorithms and applications, and design technologies and tools were presented. This special issue aims at providing an important venue to show most of the best RAW's 2010 scientific contributions to reconfigurable computing, here in extended and improved versions. This special issue includes extended and improved papers selected from the peer-reviewed papers that were presented at RAW 2010 and consists of the seven following papers.

The paper "A Vector-like reconfigurable floating-point unit for the logarithm," by N. Alachiotis and A. Stamatakis, presents a pipelined datapath for calculating the logarithm function of data represented in single and double-precision floating point in FPGAs. A vector-like extension is also presented, which is capable of calculating two results/cycle. They compare the performance of the architectures with

the software implementations of GNU and Intel Math Kernel Library (MKL). Their approach is able to accelerate the logarithm function even when comparing to highly optimized software solutions running in current microprocessors.

The paper "A streaming high-throughput linear sorter system with contention buffering," by J. Ortiz and D. Andrews, presents a sorting unit consisting of multiple linear sorters and implemented in an FPGA. The linear sorters run in parallel to achieve higher throughput. The architecture presented in this paper is able to process multiple data values per clock cycle and presents speedups over a quicksort software solution running in a MicroBlaze softcore.

The paper "The potential for a GPU-like overlay architecture for FPGAs," by J. Kingyens and J. G. Steffan, proposes a soft processor inspired by GPUs. The architecture supports multithreading, vector operations, predication, and pipelining. They highlight the mechanisms for managing threads and register files that maximize data-level and instruction-level parallelism. An efficient approach to overcome the challenges of port limitations of the FPGA block memories is also presented in this paper. The proposed architecture can be programmed in the same programming model of GPUs and can be an interesting option for accelerating applications suitable to be mapped to GPU-like architectures.

The paper "Boosting parallel applications performance on applying DIM technique in a multiprocessing environment," by Mateus Rutzig et al., extends the DIM (dynamic instruction merging) approach to be used in a multiprocessor scenario. They present experimental evidence that

the acceleration achieved by the parallelism met using multi-core architectures can be effectively improved by augmenting the ILP (instruction-level parallelism) in each core.

The paper “High-level synthesis of in-circuit assertions for verification, debugging, and timing analysis,” by J. Curreri et al., presents an approach to support the integration of ANSI-C assertions when synthesizing C code to FPGAs. The approach enables the implementation of assertions in hardware. This can be important to verify and debug circuits generated by high-level synthesis. Furthermore, the approach also supports timing assertions and thus, can be used to verify timing properties.

The paper “Floorplacement for partial reconfigurable FPGA-based systems,” by A. Montone et al., presents a framework for floorplacement which is aware of resources and configuration tailored for Xilinx V4 and V5 FPGAs. Their approach identifies reconfigurable functional units that can share the same area of the FPGA and highlights the reduction of external wirelengths and the reuse of communication links compared to using purely area-driven approaches.

The paper “Operating system for runtime reconfigurable multiprocessor systems,” by D. Göhringer et al., presents an operating system able to do scheduling, resource allocation, and reconfiguration and to manage accesses to the internal configuration access port (ICAP). The operating system is used in the context of RAMPSoC, a runtime adaptive multiprocessor system-on-chip. In this SoC, the hardware tasks are transferred to the reconfigurable hardware via the configuration access port, and the software tasks can be loaded into the local memory of each microprocessor by using also a configuration access port or the on-chip communication infrastructure.

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