Editorial

Selected Papers from the Symposium on Integrated Circuits and Systems Design (SBCCI 2011)

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SBCCI is an international forum dedicated to Integrated Circuits and Systems Design, Test and CAD, held annually in Brazil, copromoted by SBC, SBMicro, IEEE CAS, ACM SIGDA, and IFIP WG 10.5. The 24th edition of the Symposium on Integrated Circuits and Systems Design (SBCCI) was held in João Pessoa, PB, Brazil, from August 30 to September 2, 2011.

Track 2.1 of SBCCI 2011 was dedicated to Reconfigurable Computing. Some of the papers of this track have been selected for this special issue.

This special issue presents some of the latest developments in the area of design, specification, and modeling languages and applications of reconfigurable computing; reconfigurable architectures and novel applications of FPGAs; hardware-software codesign and coverification; emulation and prototyping techniques.

Ten articles are in this issue.

The main disadvantages of the reconfigurable approaches are still the costs in area and power consumption. In “*HoneyComb: an application-driven online adaptive reconfigurable hardware architecture*,” A. Thomas et al. present a solution for application driven adaptation of a reconfigurable architecture at register transfer level to reduce the resource requirements and power consumption while keeping the flexibility and performance for a predefined set of applications. A prototype chip of this architecture designed in 90 nm standard cell technology manufactured by TSMC is presented.

Multiprocessor system-on-chip (MPSoC) security is becoming an important requirement. The challenge is to

provide MPSoC security that makes possible a trustworthy system that meets the performance and security requirements of all the applications. The network-on-chip (NoC) can be used to efficiently incorporate security. In “*QoS hierarchical NoC-based architecture for MPSoC dynamic protection*,” J. Sepulveda et al. propose the implementation of Quality of Security Service to overcome present MPSoC vulnerabilities. The paper presents the implementation of a layered dynamic security NoC architecture to overcome actual MPSoC vulnerabilities.

Networked multiprocessor system-on-chips are used to implement novel embedded applications characterized by increasing requirements on processing performance as well as the demand for communication between several devices. Such systems require a detailed exploration on both, architectures and system design. In “*Efficient execution of networked MPSoC models by exploiting multiple platform levels*,” C. Roth et al. present a methodology that embeds previous work into a simulation platform, which facilitates efficient execution of cross-domain simulation models on different abstraction levels.

In “*Open systemC simulator with support for power gating design*,” G. S. Silveira et al. present an open source SystemC simulator with support to Power Gating design. This simulator is an alternative to assist the functional verification accomplishment of systems modeled in RTL. The possibility of controlling the retention and isolation of Power Gated Functional Block is presented turning the simulations more stable and accurate.

In “*Modeling and implementation of a power estimation methodology for systemC*,” M. Kuehnle et al. describe a methodology to model power consumption of logic modules. A detailed mathematical model is presented and incorporated in a tool for translation of models written in VHDL to SystemC. The power analysis is based on a statistical model of the underlying HW structure and an analysis of input data.

In “*Development of a SoC for digital television set-top box: architecture and system integration issues*,” A. B. Soares et al. present the development of a set-top box for Digital Television compliant to the SBTVD standard. It is a complex digital system integrating audio and video decoders and a CPU to run user interface and applications. Practical strategies used to solve integration problems are discussed. The SoC architecture is validated and is prototyped using a Xilinx Virtex-5 FPGA board.

In “*Algorithm and hardware design of a fast intra-frame mode decision module for H.264/AVC encoders*,” D. Palomino et al. present a fast intra mode decision algorithm and its hardware architecture design for an H.264/AVC video encoder. The proposed algorithm allows the complete elimination of the encoding loop present in Rate-Distortion-Optimization based mode decision, which is substituted by simple distortion calculations and comparisons, decreasing the complexity of the video encoder. The designed architecture of the fast intradecision algorithm was described in VHDL and synthesized targeting Stratix II FPGA and TSMC 0.18 μm standard cell library. The motion estimation is the most complex module in a video H.264/AVC encoder requiring a high processing throughput and high memory bandwidth, mainly when the focus is high definition videos. The throughput problem can be solved increasing the parallelism in the internal operations. The external memory bandwidth may be reduced using a memory hierarchy. In “*A memory hierarchy model based on data reuse for full search motion estimation on high-definition digital videos*,” A. S. B. Lopes et al. present a memory hierarchy model for a full search motion estimation core. The proposed memory hierarchy expressively reduces the external memory bandwidth required for the motion estimation process and it provides a high data throughput. A case study for the proposed hierarchy was implemented and prototyped on a Virtex 4 FPGA.

In “*An FPGA-based omnidirectional vision sensor for motion detection on mobile robots*,” J. Y. Mori et al. present a FPGA-based omnidirectional vision system for mobile robotic applications. The proposed architecture is suitable for robot localization, allowing to compute the distance between the robot and the surrounding objects. The overall architecture has been mapped onto a Cyclone II FPGA device, using a hardware/software codesign approach, which comprises a NIOS II embedded microprocessor and specific image processing blocks implemented in hardware.

In “*An optimization-based reconfigurable design for a 6-bit 11-MHz parallel pipeline ADC with double-sampling S&H*,” W. Carvajal and W. V. Noije present a 6 bit, 11 MS/s time-interleaved pipeline A/D converter design. The specification process, from block level to elementary circuits, is covered to draw a design methodology. Prelayout simulations of the

complete ADC are presented to characterize the designed converter, which consumes 12 mW while sampling a 500 kHz input signal. The circuit will be sent to fabrication in a CMOS 0.35 μm AMS technology, and some postlayout results are shown.

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