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# Special Issue on
# High-Level Design for Reconfigurable Platforms

# CALL FOR PAPERS

In recent years, reconfigurable devices have emerged as a serious contender for efficient implementation of computationally intensive applications. Unlike their competition, multicore CPUs and GPGPUs, reconfigurable devices such as Field-Programmable Gate Arrays (FPGAs), do not implement a fixed hardware architecture but rather can be tailored to the application at hand. In conjunction with the recent advances in high-level design, FPGAs are now accessible to programmers who can both implement advanced algorithms and design the ultimate computing fabric for them at the same time.Historically, FPGA devices have been heavily used in communications, ASIC prototyping, and commercial audio/video applications as well as signal processing and many others. The challenge has always been the need to describe a design using low-level timed structures, typically in languages such as Verilog or VHDL. These languages, albeit accurate and effective, are prohibitive for many developers. Recent advances in high-level compilers for FPGAs have resulted in increasing adoption of FPGAs in a variety of market segments by addressing two most significant challenges designers face: familiarity with the intricacies of hardware design and rapid design exploration. Novel industrial high-level design tools, such as those provided by Altera and Xilinx to implement OpenCL applications as well as academic ones such as LegUp have enabled users without hardware design expertise to design and implement their applications on modern FPGAs. As a consequence of using high-level design tools, users have found themselves in a unique position to be able to perform rapid design space exploration at the design level, shortening a first-try design time from months to days. This rapid architectural exploration has enabled users to make trade-offs between area, performance, and power to implement applications as efficiently as possible, often maximizing performance per area and performance per Watt. Furthermore, additional knobs usually provided by high-level design tools permit fine tuning of an application at a low-level on a particular target platform to address more complex optimization objectives.

As for high-level design tools for reconfigurable platforms trend towards maturity, we begin to consider a path where high-level design replaces low-level Verilog and VHDL design for majority of designs in much the same way optimizing compilers have enabled the replacement of the assembly language with C/C++ and other languages to accelerate design time and productivity. There are several key questions that will need to be answered in the near future, including but not limited to languages, language features, design patterns, and compiler optimizations as well as profiling and debugging to drive high-level design tools into the mainstream.

We invite authors to contribute original research articles, as well as review articles, that advance the state-of-the-art in high-level design for reconfigurable platforms and stimulate further research to improve high-level design tools and compilers.

Potential topics include but are not limited to the following:

- Novel high-level design tools, algorithms, approaches, and languages for application development
- Novel profiling and debugging tools
- Advances in reconfigurable device architectures to enable application development
- Emerging applications suitable for reconfigurable platforms and their implementation from high-level description

Authors can submit their manuscripts through the Manuscript Tracking System at http://mts.hindawi.com/submit/journals/ijrc/ecrp/.

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