International Scholarly Research Network
ISRN Nanotechnology
Volume 2012, Article ID 617214, 10 pages
doi:10.5402/2012/617214

Research Article

Development of Quantum Simulator for Emerging Nanoelectronics Devices

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Received 5 April 2012; Accepted 21 June 2012

Academic Editors: B. Coasne, G. A. Kachurin, D. K. Sarker, and D. Tsoukalas

We have developed NEMO-VN2, a new quantum device modeling tool that simulates a wide variety of quantum devices including the resonant tunneling diode, the single electron transistor, the molecular field effect transistor, the carbon nanotube field effect transistor, and the spin field effect transistor. In this work the nonequilibrium Green's function is used to perform a comprehensive study of the emerging nanoelectronics devices. The program has been written by using graphic user interface of Matlab. NEMO-VN2 uses Matlab to solve Schrodinger equation to get current-voltage characteristics of quantum devices. In the paper, we present a short overview of the theoretical methodology using non-equilibrium Green's function for modeling of various quantum devices and typical simulations used to illustrate the capabilities of the NEMO-VN2.

1. Introduction

The dimensional scaling of complementary metal-oxide-semiconductor (CMOS) device and process technology will become much more difficult as the semiconductor industry approaches 10 nm (6 nm physical channel length) around year 2019 and will eventually approach asymptotic end according to the International Technology Roadmap for Semiconductor for emerging research devices [1]. Beyond this period of traditional CMOS, it may be possible to continue functional scaling by integrating alternative electronic device onto a silicon platform. These alternative electronic devices include 1D structures such as carbon nanotube field effect transistor (CNTFET), resonant tunneling diode (RTD), single electron transistor (SET), molecular field effect transistor (MFET), and spin devices, all of which are discussed in this paper.

Despite these exciting possibilities, nanoelectronic devices are still in their relative infancy. The expense and difficulty of device fabrication precludes simply building and testing vast arrays of quantum devices. To focus efficiently on the best design, engineers need a tool that predicts electronic characteristics as a function of the device geometry and composition. In the more scientific mode, such a simulator would greatly enhance the understanding of quantum effects that drive the transport process and provide a means to investigate new device concepts.

Even conventional devices require a correction for quantum effects associated with the smaller device features. MOS devices, for example, exhibit electron confinement effects in the inversion layer. This phenomenon is a function of decreasing oxide thickness rather than the overall size of the device. Quantum effects become important as the oxide layer thickness decreases below the 3 nm, which will soon be a standard for manufactured integrated circuits. Problems of this nature will become more prevalent as device geometries continue to shrink.

Nanoelectronic device modeling requires a fundamental quantum-mechanical approach. Many forms of quantum correction to classical electronic device models have been proposed or implemented. These include MOSFET specific quantum corrections [2–7] and generic quantum corrections to the drift-diffusion [8], hydrodynamic [9–11], and Boltzmann transport equation [12] models. Therefore, the semiconductor industry needs a new fully quantum-mechanically based TCAD tool.

Recently, there are various groups achieving success in pursuing to build simulator for SET [13, 14]. The Monte

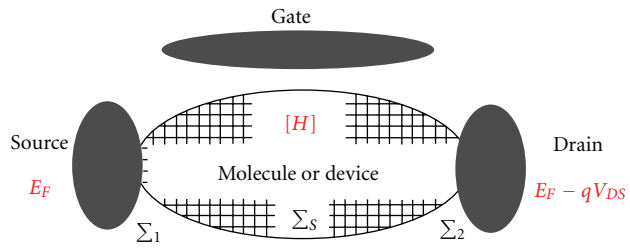


Figure 1: A generic transistor comprised of a device channel connected to source and drain contacts. The source-drain current is modulated by a third electrode, the gate. The quantities involved in NEGF formalism are also shown.

Carlo simulations (e.g., SIMON [15], MOSES [16], and KOSEC [17]) and master equation methods [18, 19] that are quite accurate but also very time consuming, and they are not simple. In contrast, model used non-equilibrium Green's function method (NEGF) [20, 21] commonly used in the nanoscale devices and are superior in terms of simplicity.

In this work, we developed a general purpose quantum device simulator called NEMO-VN2. NEMO-VN2 can simulate a wide variety of nanoelectronic devices, including resonant tunneling diode, single electron transistor, molecular field effect transistor, carbon nanotube field effect transistor, and spin field effect transistor. It has a collection of models that allows user to trade off between calculation speed and accuracy. NEMO-VN2 also includes a graphic user interface (GUI) of Matlab that enables parameter entry, calculation control, display of calculation results, and in situ data analysis methods.

Another important goal of the NEMO-VN2 project was to make a user-friendly simulator that provides as much control as possible over every aspect of the simulation. Flexibility and ease of use are difficult to achieve simultaneously, but given the complexity of quantum device simulations became clear that both criteria were vital to program success. Consequently, graphic user interface development was a major part of the NEMO-VN2 program.

This paper reviews the capabilities of NEMO-VN2, summarizes the theoretical approach, and gives examples of several NEMO-VN2 simulations.

2. Overview of Quantum Devices and Their Simulations

2.1. Nonequilibrium Green's Function Method in Modeling of Quantum Devices. The NEGF model of the quantum devices used for transport simulations is shown in Figure 1.

Here, H is the device Hamiltonian, and the self-energy functions $\Sigma_{1,2}$ present the semi-infinite ideal source-drain contacts. Σ_S is the self-energy for the e-ph interaction, and one sets $\Sigma_S = 0$ for the ballistic approximation.

The retarded Green's function for the device in matrix form is given by

$$G(E) = \left[(E + i\eta^+)I - H - \Sigma(E)\right]^{-1}, \quad (1)$$

where η^+ is an infinitesimal positive value, and I is the identity matrix.

The self-energy contains contributions from all mechanisms of relaxation, which are the source and drain electrodes, and from scattering

$$\Sigma(E) = \Sigma_1(E) + \Sigma_2(E) + \Sigma_S(E). \quad (2)$$

Note that, in (2), the self-energy functions are, in general, energy dependent. The current flows from source to drain can be defined as follows:

$$I = \frac{4e}{\hbar}\int_{-\infty}^{+\infty}\frac{dE}{2\pi}T(E)\left[f\left(E - E_S^F\right) - f\left(E - E_D^F\right)\right], \quad (3)$$

where $f(E)$ is the Fermi distribution, and $E_{S/D}^F$ denotes the source and drain Fermi energies, respectively. With the transmission coefficient $T(E)$ given by:

$$T(E) = \text{Trace}\left[\Gamma_S(E)G(E)\Gamma_D G^+(E)\right], \quad (4)$$

where level broadening can be defined as follows:

$$\Gamma(E) = i\left[\Sigma(E) - \Sigma^+(E)\right], \quad (5)$$

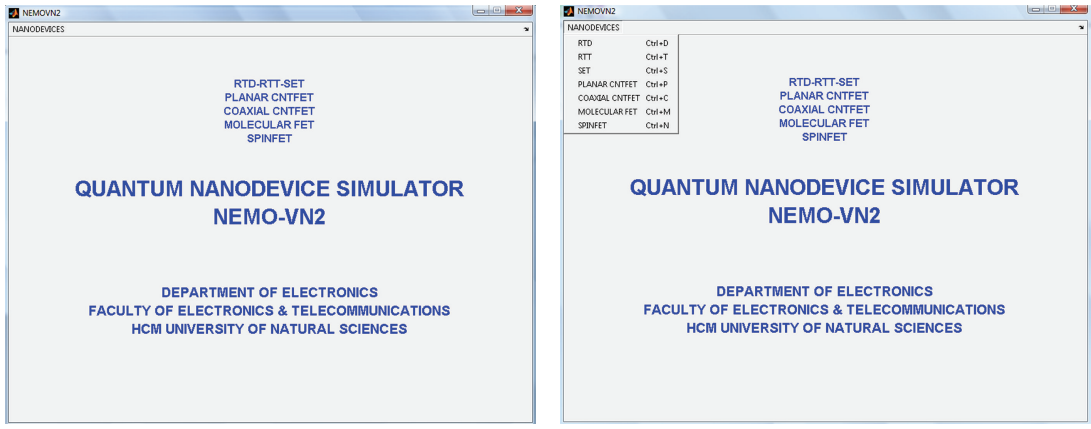
where $\Sigma^+(E)$ represents the Hermitian conjugate of Σ matrix defined by (2).

2.2. Main Screen NEMO-VN2. NEMO-VN2 has a rich variety of simulation models, while this provides the maximum flexibility in term of applicability to types of different devices and test conditions. The problem is that NEMO-VN2 requires over 100 simulation parameters. Traditional device simulators force the users to familiarize themselves with all available simulation parameters and ensure that they are set correctly. To minimize this burden for the users, NEMO-VN2 uses a hierarchical approach to input and display simulation parameter values. The top level of this hierarchy specifies the highest level option (nanodevices). Subsequent levels contain more detailed options such as current-voltage characteristics of devices, types of material, size of devices, temperature, colors, and so forth.

The main screen shown in Figure 2(a) is the central location where the user controls the NEMO-VN2 simulation. From main screen, the user can choose various types of quantum device simulations by clicking the left mouse pointer on submenu of nanodevices (in the left top corner). In this manner, the user can quickly enter the device list and hot keys with minimum of typing. Clicking the left mouse pointer on each item in the device list or using hot keys initiates the selection of models which is used to calculate the current-voltage characteristics (Figure 2(b)).

2.3. Emerging Quantum Devices

2.3.1. Resonant Tunneling Devices. Resonant tunneling devices for logic applications include resonant tunnel transistors (RTTs) and hybrid devices incorporating resonant tunneling diodes and one or more FETs (RTDs-FET). The RTDs are two terminal devices that have a very high



(a) (b)

Figure 2: (a) The NEMO-VN2 main screen, (b) pressing the left mouse pointer on "NANODEVICES" displays a list of simulation quantum devices.

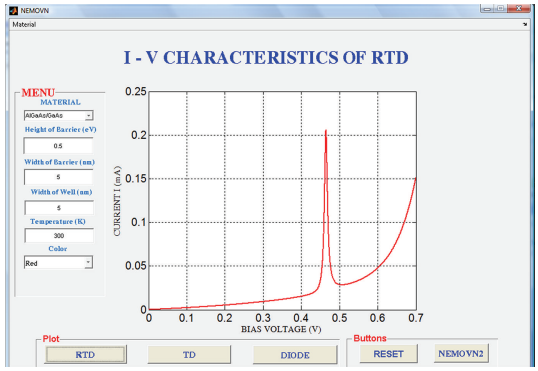


Figure 3: Current-voltage characteristics of RTD at room temperature.

switching speed and exhibit a region of negative differential resistance in their I-V curves. These two characteristics make them potentially attractive as high-speed switching devices.

Adding a control terminal to RTDs extends their usability to a variety of applications. This approach has been used to build resonant tunneling transistor. RTTs have a negative transconductance that can be used in several logic circuits, for example, in XOR gate with only one transistor.

Traditionally, RTDs have been fabricated in III-V material systems that have limited widespread applicability. Recently, several papers have described fabrication of group IV devices with silicon compatible materials. Overall, the resonant tunneling devices may be used for certain niche applications requiring high speed and low dynamic range and low peak currents provided the manufacturing issues associated with uniformity of the tunneling barrier can be resolved. The principle focus of the recent research activity involving RTDs has been in the area of integration on the silicon platform [1].

Current-voltage characteristics of the RTD are shown in Figure 3. Characteristic curve is divided into two parts: positive and negative resistances. Here, it should be emphasized that the current peak and the valley currents of the RTD are perfectly represented by the model.

2.3.2. Single Electron Transistor. A model of single electron transistor (SET) usually called a capacitance model is shown in Figure 4. An SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal supported by a very thin (about 1 nm) insulator. The only way for electrons is from one of the metal electrodes to travel to the other electrode is to tunnel through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction in multiples of e, the charge of electron.

A quantum dot (QD) is usually formed in two dimensional electron gas (2DEG) in GaAs/AlGaAs using standard electron beam lithography. The quantum dot is connected to the source and drain electrodes through tunnel barriers. The potential in the dot can be controlled by the gate electrode which is capacitively coupled to the quantum dot (Figure 4(b)). The current through the quantum dot can be periodically modulated by the gate voltage ($V_G = (2n + 1) \times e/2C_G$, Coulomb oscillations). When the current is zero (Coulomb blockade, CB), the number of electrons is fixed. Therefore it differs exactly by one on both sides of the current peak.

By utilizing the simulator, namely, NEMO-VN2, the I_D-V_G characteristics of SET having the given parameters are shown in Figure 5.

Figure 5 demonstrates the typical Coulomb oscillation behavior in SET I_D-V_G characteristics. It shows that the SET Coulomb oscillation period (e/C_G, e is the electronic charge) is dictated by SET's gate capacitance. Values of gate voltage at the first and the second peaks are $e/2C_G$ (80 mV) and $3e/2C_G$ (240 mV), respectively. Here, it should be emphasized that the peak and the valley currents of Coulomb oscillations are perfectly represented by the model. The results calculated according to model ($e/2C_G$ for $C_G = 1$ aF) coincide well with the simulated ones. Current-voltage (I_D-V_G) characteristics showing the suppression of the Coulomb oscillation by

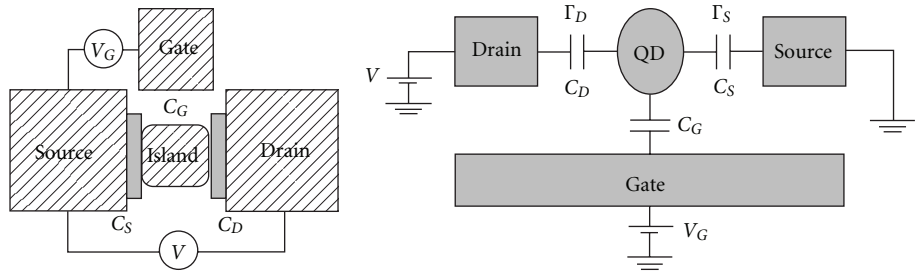


Figure 4: (a) Structure of single electron transistor, (b) equivalent schematic diagram of SET. The quantum dot is connected to the source and drain electrodes through small tunnel barriers. The potential in the quantum dot can be modified by the gate electrode which is capacitively coupled to the quantum dot, $V_G = (2n + 1)e/2C_G$. The DC bias (V_D) is applied and the current is measured as a function of V_D and V_G. The SET's parameters are C_S, C_D, C_G, Γ_S, and Γ_D.

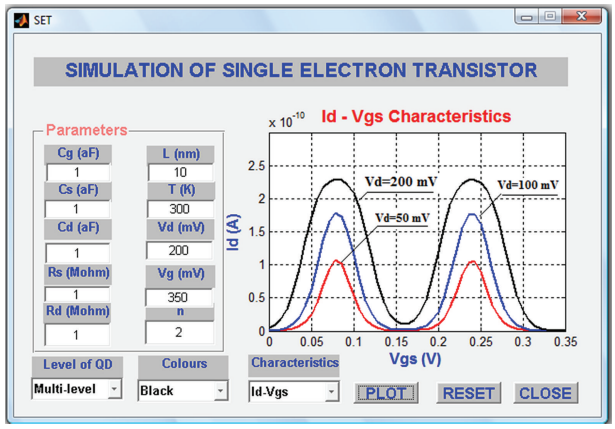


Figure 5: Typical I_D-V_G characteristics (Coulomb oscillations) of SET simulated by the simulator NEMO-VN2 for various values of V_D = 50 mV, 100 mV, and 200 mV at room temperature, T = 300 K. The SET device parameters are L = 10 nm, $C_G = C_S = C_D$ = 1 aF, and $R_S = R_D$ = 1 MΩ.

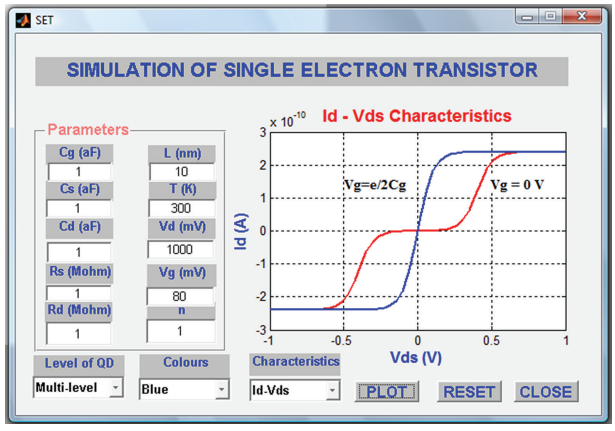


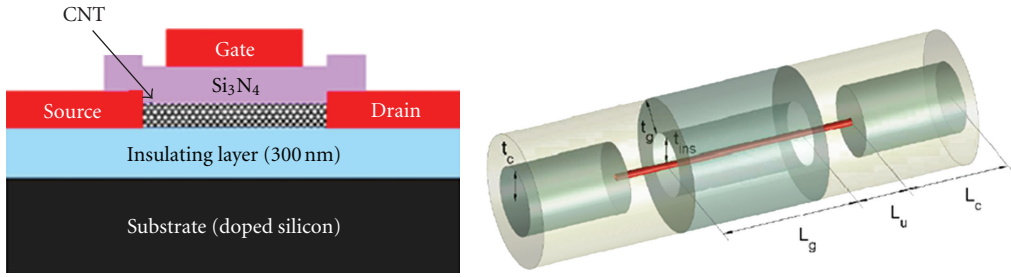
Figure 6: I_D-V_D characteristics simulated by the simulator at room temperature for various values of V_G = 0 mV and $V_G = e/2C_G$. The SET device parameters are L = 10 nm, $C_G = C_S = C_D$ = 1 aF, and $R_S = R_D$ = 1 MΩ.

broadening current peaks increased at high V_D (200 mV). It also reveals the fact that it is difficult to obtain the Coulomb oscillations in the device characteristics at high V_D greater than $3e/C_T$ (C_T is total capacitance of the SET), (160 mV). It should be noted that high drain voltage, V_D, undermines SET's current-voltage characteristics.

Figure 6 reproduces SET's I_D-V_D characteristics at room temperature (T = 300 K) for different gate biases, V_G = 0 mV and $V_G = e/2C_G$ (Coulomb oscillation). For V_G = 0 mV, V_D starts from the Coulomb blockage (CB) region and increases (or decreases) through the single-electron tunneling region. For $V_G = e/2C_G$ (at the first Coulomb oscillation peak), I_D starts from zero and increases (or decreases) linearly.

2.3.3. Carbon Nanotube Field Effect Transistor. Since the discovery of carbon nanotubes (CNTs) by Iijima in 1991 [22], significant progress has been achieved for both understanding the fundamental properties and exploring possible engineering applications. The possible application for nanoelectronic devices has been extensively explored since the demonstration of the first carbon nanotube transistors in 1998 [23]. Carbon nanotubes are attractive for nanoelectronic applications due to its excellent electric properties. In a nanotube, low bias transport can be nearly ballistic across distances of several hundred nanometers. The conduction and valence bands are symmetric, which is advantageous for complementary applications. The bandstructure is direct, which enables optical emission, and finally, CNTs are highly resistant to electromigration.

Significant efforts have devoted to understand how a carbon nanotube transistor operates and to improve the transistor performance [24, 25]. It has been demonstrated that most CNTFETs to date operates like nonconventional Schottky-barrier transistors [26, 27], which results in quite different device and scaling behaviors from the MOSFET-like transistors. Important techniques for significantly improving the transistor performance, including the aggressively scaling of the nanotube channel, integration of thin high-κ gate dielectric insulator [28], use of excellent source-drain metal contacts [29], and demonstration of the self-align techniques, have been successfully developed. Very recently,



(a) (b)

Figure 7: Structures of CNTFETs: (a) planar CNTFET, (b) coaxial CNTFET.

a nanotube transistor, which integrates ultrashort channel, thin high-κ top gate insulator, and excellent Pd source-drain contacts, is demonstrated using a self-align technique [30]. Promising transistor performance exceeding the state-of-the-art Si MOSFETs is achieved. The transistor has a near-ballistic source-drain conductance of $0.5 \times e^2/h$ and delivers a current of 20 μA at $|V_G - V_T| \sim 1$ V. In this work, numerical simulations are developed to explain experiments, to understand how the transistor operates and what controls the performance, and to explore the approaches to improve the transistor performance. New simulation approaches are necessary for a carbon nanotube transistor because it operates quite different from Si transistors. The carbon nanotube channel is a quasi-one-dimensional conductor, which has fundamentally different carrier transport properties from the Si MOSFET channel. It has been demonstrated that treating the Schottky barriers at the metal/CNT interface and near-ballistic transport in the channel are important for correctly modeling the transistor. The CNT channel is a cylindrical semiconductor with a ~1 nm diameter, which means the electrostatic behavior of the transistor is quite different from Si MOSFETs with a 2D electron gas. All carbon bonds are well satisfied at the carbon nanotube surface, which results in a different semiconductor/oxide interface. Furthermore, the phonon vibration modes and carrier scattering mechanisms are quite different in carbon nanotubes, which results in different roles of phonon scattering in CNTFETs. Recent progress in the field of CNTFET has been summarized in [31–33].

CNTFET is a three-terminal device consisting of a semiconducting nanotube bringing two contacts (source and drain), and acting as a carrier channel, which is turned on or off electrically via the third contact (gate). Presently, there are several types of CNTFETs that have been fabricated, but CNTFET geometries may be grouped in two major categories: planar and coaxial CNTFETs, whether planar or coaxial relies on simple principles, while being governed by additional phenomena such as 1D density of states (DOS), ballistic transport, and phonon scattering.

Planar CNTFETs (Figure 7(a)) constitute the majority of devices fabricated to date, mostly due to their relative simplicity and moderate compatibility with existing manufacturing technologies. The coaxial geometry (Figure 7(b)) maximizes the capacitive coupling between the gate electrode and the nanotube surface, thereby inducing more channel charge at a given bias than other geometries. This improved coupling is desirable in mitigating the short-channel effects that plague technologies like CMOS as they downside device features. The key device dimensions are the gate inner radius, R_g and thickness, t_g; the nanotube radius, R_t and length L_t; the insulator thickness $t_{\text{ins}} = R_g - R_t$; the end-contact radius, t_c (the source and drain may sometimes be of different sizes) and length, L_c; the gate-underlap L_u.

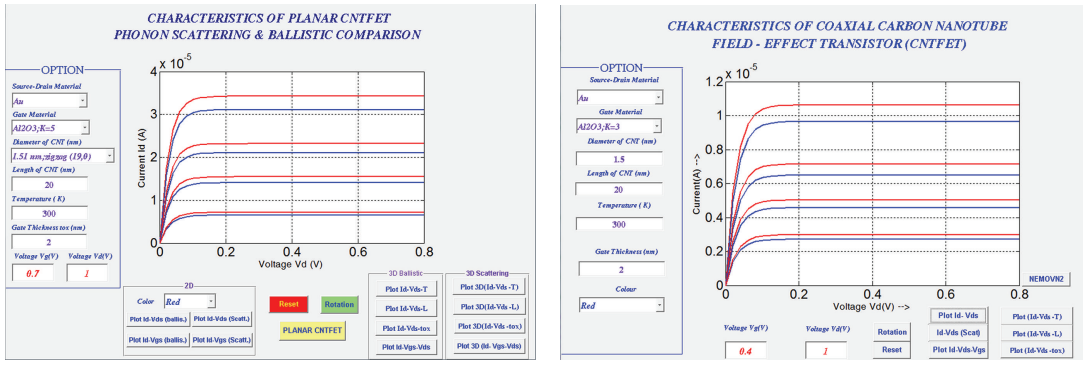
Figure 8 compares the I_{DS}-V_{DS} results for two types of planar and coaxial CNTFETs having the length of 20 nm under ballistic transport and that with phonon scattering. It is shown that scattering can have an appreciable effect on the ON current. At $V_{GS} = 0.7$ V, in the planar and coaxial CNTFETs, the ON current is reduced by 9% due to the phonon scattering. It can be noted that when the gate voltage is increased the saturated drain current gradually increased.

Figure 9 compares the length dependence of I_{DS}-V_{DS} results for the (19,0) CNTFETs under phonon scattering. The ON current at $V_{GS} = 0.7$ V is reduced when the length is changed by 15, 10, 5, and 2.5 nm.

In Figure 9(a), it is also shown that the impact of phonon scattering in planar CNTFET increases for shorter length tubes at high voltage bias. It should be noted that ON current strongly depends on reducing the length of CNTFET. At high gate voltage bias ON current of CNTFET having length of 15 nm is by 30 μA, when length of CNTFET reduced to 2.5 nm ON current is by 8 pA. In Figure 9(b), it is also shown that the impact of phonon scattering in coaxial CNTFET. ON current increases for shorter length tubes at high voltage bias. It should be noted that ON current strongly depends on reducing the length of CNTFET. At high gate voltage bias ON current of the coaxial CNTFET having length of 15 nm is by 9 μA, when length of CNTFET reduced to 2.5 nm ON current is by 150 nA.

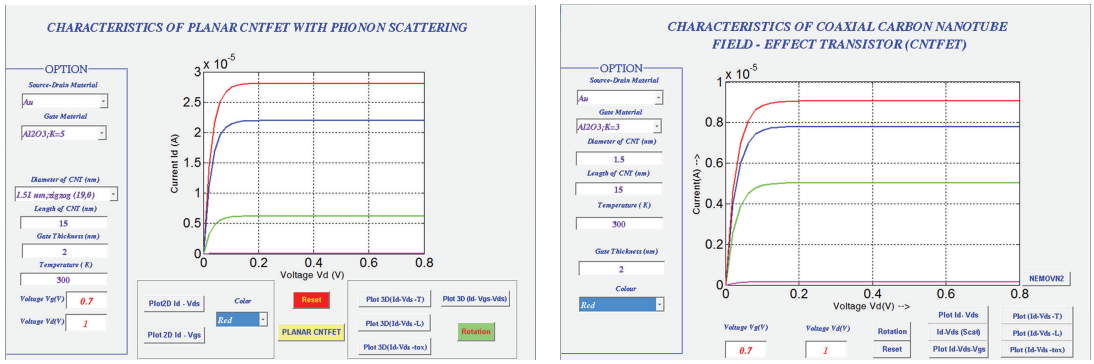
Figure 10 shows 3D I_{DS}-V_{GS} characteristics of planar and coaxial CNTFETs. When the gate voltage is small, the drain current is gradually increased. When the gate voltage is greater than $V_{GS} = 0.3$ V, the drain current is exponentially increased.

2.3.4. Molecular Field Effect Transistor. Current interest in molecular electronics is largely driven by expectations that



(a) (b)

Figure 8: I_{DS}-V_{DS} characteristics of (a) planar and (b) coaxial CNTFETs having the length of 20 nm under ballistic transport (red colour), with scattering (green colour) at various gate biases in the range from 0.4 to 0.7 V in the step of 0.1 V. The bottom and top curves are at the gate voltages of 0.4 V and 0.7 V, respectively.



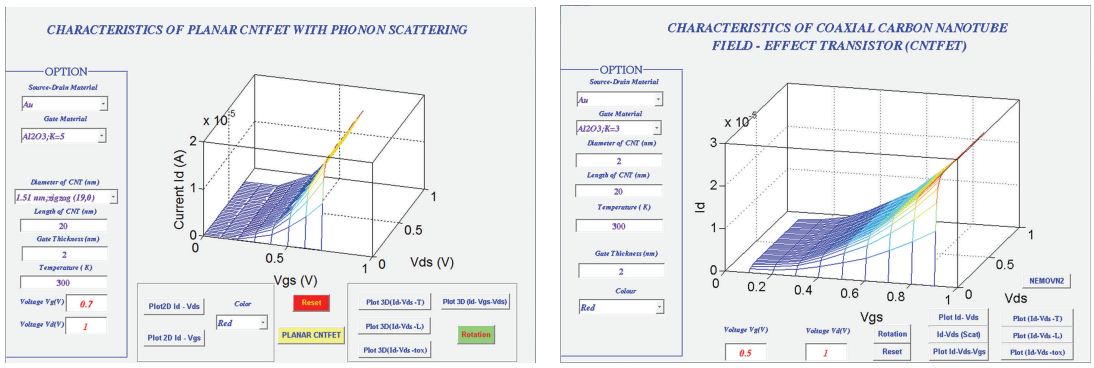
(a) (b)

Figure 9: The length dependence of I_{DS}-V_{DS} results for the (19, 0) CNTFETs under phonon scattering: (a) planar CNTFETs; (b) coaxial CNTFETs. The lengths of CNTFETs are of 15, 10, 5, and 2.5 nm from top to bottom curves.

molecules can be used as nanoelectronic components able to complement or replace standard silicon CMOS technology on the way down to 10 nm circuit components. The first speculations about molecular electronic devices (diodes, rectifiers) were apparently made in mid 1970s [34]. That original suggestion of a molecular rectifier has generated a large interest in the field and a flurry of suggestions of various molecular electronic components.

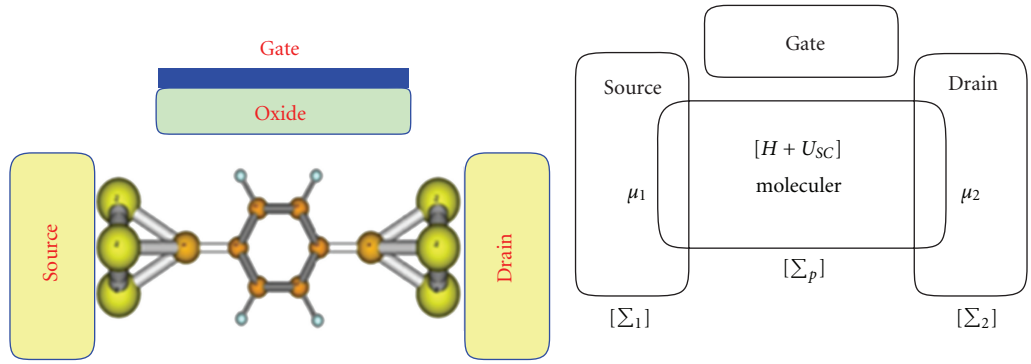
The theoretical description of electron transport through molecular electronics (MEs) systems is a complex many-particle problem, where the full solution is not possible in practice. The available approaches use certain approximations; however, the basis for transport calculations is the description of the ME device itself, which implies that approaches to the simulation of transport and structure cannot be chosen independently. A diverse spectrum of approaches to the transport calculations was developed to study the whole spectrum of problems ranging from exact many-particle problem treatment within some simplified models (e.g., the two-barrier potential) for the system, to semiempirical models for transport through quite realistic structures consisting of few hundred atoms. Although some of these methods were developed for purposes apparently different from the ME design, like intramolecular donor-acceptor charge transfer or scanning tunneling microscopy (STM) image calculation, they are often applicable to ME systems.

Two distinct approaches to the transport calculations are suitable for proper accounting of the full chemical structure of the system: the *Green's function* (GF) method [35] and the *density functional* (DF) method [36]. The conceptual difference is that in the GF approach the interactions within the system are treated in the phenomenological way, in the sense that transport calculations and calculations of system properties are separated, thus enabling any level of input to be used. The range of examples varies from semiempirical models to discrete tight-binding or continuous DF descriptions. Within the DFT framework, the charge carrier density is the unique parameter, hence the current is naturally calculated simultaneously with other system properties that depend on or constitute the density. Consequently, at least in theory, the system could be seamlessly restructured under the bias, but neither the tight-binding nor semiempirical level of the description is naturally allowed within the DF method.



(a) (b)

Figure 10: Three-dimensional simulations of I_{DS}-V_{GS} characteristics of CNTFETs having the length of 20 nm: (a) planar CNTFET, (b) coaxial CNTFET.



(a) (b)

Figure 11: (a) Schematic view of a molecule coupled to source and drain contacts. (b) The molecule is described by a Hamiltonian H and a self-consistent potential U_{SC}. The effect of the large contacts is described using self-energy matrices $\Sigma_{1,2}$. Scattering processes may be described using another self-energy matrix Σ_p. The source and drain contacts are identified by their respective Fermi levels μ_1 and μ_2.

Hence, GF is often used in a semiempirical way to fit the experimental data. The fitting parameter is usually the shape of the voltage drop over the system.

The central focus of this work is to introduce a model of three-terminal molecular devices, namely the molecular field effect transistor. MFET is a promising alternative candidate of traditional MOSFET in future due to its small size, low power, and high speed. The structure of the MFET is in shape like traditional MOSFET, but its conductive channel is replaced by a benzene-1,4-dithiolate molecule.

A schematic view of a molecule coupled to gold source (S) and drain (D) contacts is shown in Figure 11. As an example we use the benzene-1,4-dithiol molecule which consists of a phenyl ring with thiol(-SH) end groups. A gate terminal may be used to modulate the conductance of the molecule. The coupling between the gate and the molecule is purely capacitive; there is no gate current.

The molecular energy levels consist of a set of occupied levels separated by a gap from a set of unoccupied levels. At equilibrium, the Fermi energy is typically located in the gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), but when a bias is applied, the Fermi energy in the source contact (μ_1) floats up by qV_D relative to the Fermi level in the drain contact (μ_2). The molecule conducts when the bias is large enough that one or more of the molecular energy levels lie between μ_1 and μ_2.

Current-voltage (I-V) characteristics of the molecular field effect transistor at different values of bias voltage are shown in Figure 12.

2.3.5. Datta and Das Spin Field Effect Transistor. In recent years, a vigorous research effort to demonstrate spin transistors has been pursued. One of the motivations has been that spin transistors are identified as one of the most promising alternatives to traditional MOSFET by the International Technology Roadmap for Semiconductors [1]. Simulations have predicted that spin transistors can scale in their size with smaller switching energy and less overall power dissipation than MOSFET.

The idea of spin field-effect transistor sparked after Baibich et al. [37] and Binasch et al. [38] had discovered the giant magneto resistance effect in magnetic multilayer systems in 1988. They found huge differences in current

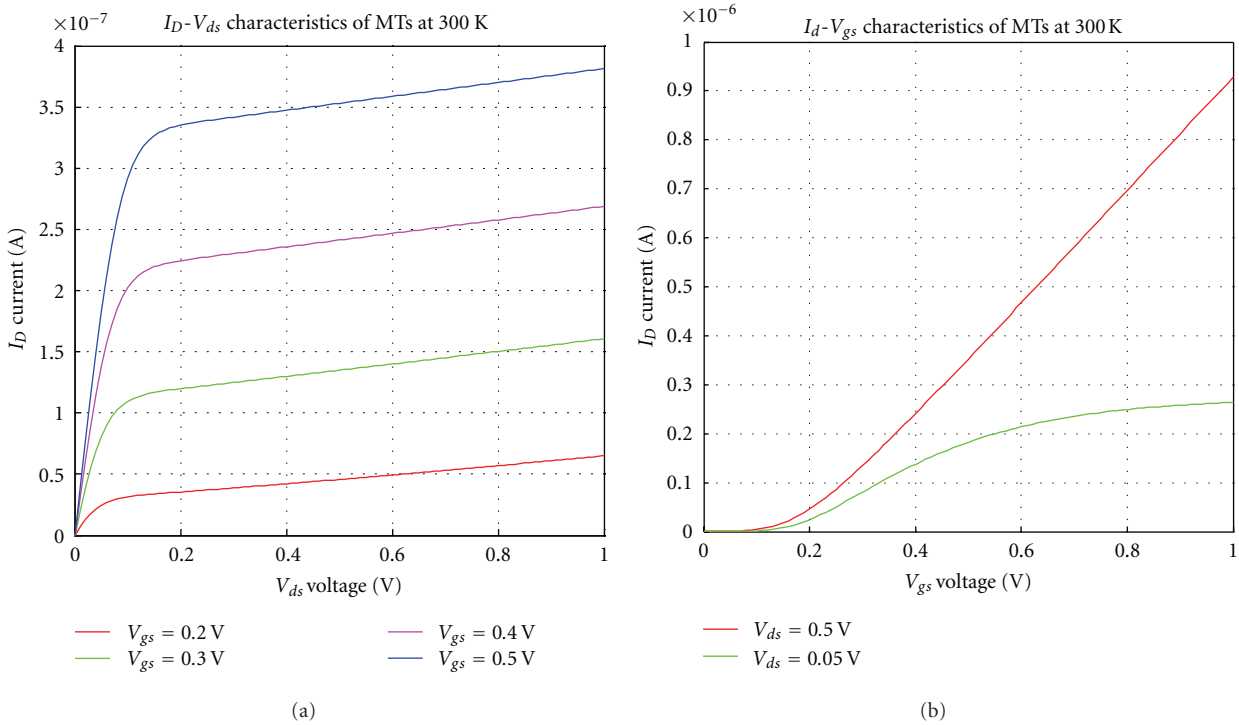


FIGURE 12: Current-voltage characteristics of the MFET: (a) $I_D = f(V_D)$ for different values of the gate voltages and (b) $I_D = f(V_G)$ for different values of the drain voltages.

coming out of a magnetic and metallic multilayer system when the magnetic layers had the same or different scattering of electrons. Shortly thereafter room temperature magnetic field sensors were made [39] using spin property which had much better performance than previously used anisotropic magneto resistance property.

In the late 1989 Datta and Das from Purdue University proposed an electron wave analog of the electrooptic light modulator [40]. Most of the today's interest in spintronics is motivated by their well-known proposed device which is now known as the spin field-effect transistor.

Datta-Das paper spurs new research direction. The operation of ideal Datta-Das spin FET can be sketched in Figure 13.

Electric field is seen as B-field in electron rest frame and given by:

$$B_{\text{eff}} = \frac{2m^*}{eh^2}\alpha E_y v = \frac{2m^* V_G}{eh^2 t_{ox}}\alpha v, \tag{6}$$

where B_{eff}, m^*, e, h, α, E_y, v, V_G, and t_{ox} are effective magnetic field, effective mass, electron charge, Planck constant, Rashba coefficient, electric field, drift velocity, gate voltage, and gate thickness, respectively. Electric field can induce precession of electron's spin in the semiconductor channel.

The spin direction of electrons can be manipulated by the gate voltage. The spin precession angle of the electrons in the semiconductor channel depends on the strength of applied voltage described by a phenomenon which is known

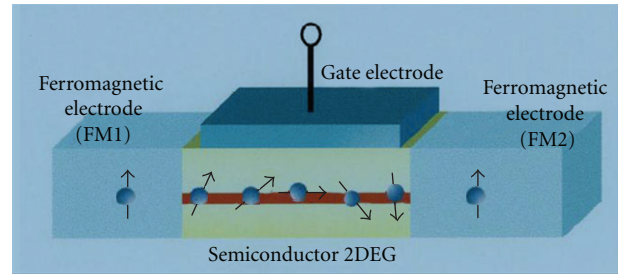


FIGURE 13: Basic configuration of a spin field-effect transistor proposed by Datta and Das.

as *Rashba effect*. The spin precession angle of electrons, $\Delta\theta$, is given by:

$$\Delta\theta = \frac{2m^* L_G}{\hbar^2}\Delta\alpha, \tag{7}$$

where, $\Delta\alpha$, L_G, and $\hbar$ are Rashba coefficient, the gate length, and modified Plank constant, respectively. Rashba coefficient, $\Delta\alpha$, can be written by:

$$\Delta\alpha = \frac{e\hbar^2 \Delta E_z}{4m^{*2}c^2} \propto V_G, \tag{8}$$

where c is light velocity in vacuum.

By utilizing the simulator namely NEMO-VN2, the I_D-V_D characteristics of spin FET having the given parameters are shown in Figure 14.

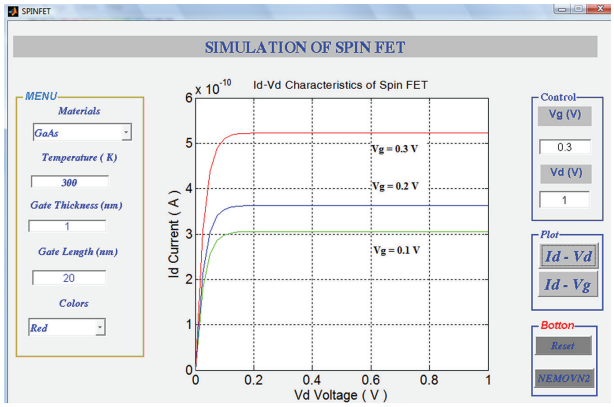


Figure 14: Typical I_D-V_D characteristics of spin FET simulated by the simulator NEMO-VN2 for various values of V_g = 0.1 V, 0.2 V and 0.3 V at room temperature, T = 300 K. The spin FET device parameters are material, GaAs, L_G = 20 nm, and the gate thickness is 1 nm.

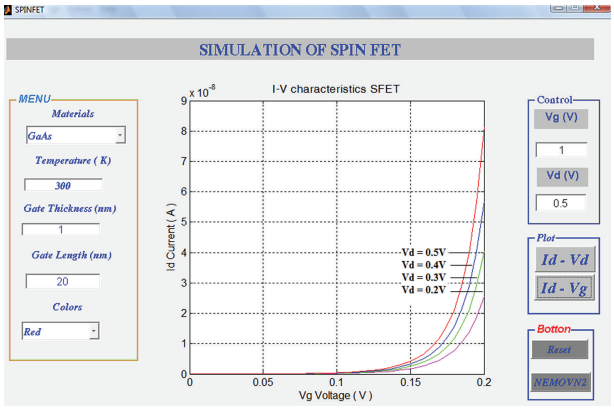


Figure 15: I_D-V_D characteristics simulated by the simulator, NEMO-VN2 at room temperature, T = 300 K for various values of V_D = 0.2 V; 0.3 V; 0.4 V; 0.5 V. The parameters of spin FET are material, GaAs, and the gate length, L_G of 20 nm, and the gate thickness of 1 nm.

Using "menu" of the main screen we can choose materials, temperature, gate thickness, and gate length for simulation of I_D-V_D characteristics of spin FET. Seven semiconductors such as GaAs, Si, InAs, InSb, $Hg_{0.775}Cd_{0.225}Te$ can be chosen for constructing channel of spin FET by using menu. I_D-V_D curves can be divided into two regions: linear and saturation. I_D starts from zero and increases linearly when drain voltage, V_D, is small. I_D is not changed when V_D is greater than (V_G-V_{th}), where V_{th} is threshold voltage.

Figure 15 demonstrates I_D-V_G characteristics of spin FET at various values of V_D: 0.2 V, 0.3 V; 0.4 V, 0.5 V at room temperature using NEMO-VN2.

3. Conclusion

We present briefly here the description of the quantum simulator, NEMO-VN2. The NEGF method is used to simulate transport of carriers in quantum devices such as the resonant tunneling diode, the single electron transistor, the molecular field effect transistor, and the planar and coaxial CNTFETs, with the account of both quantum effects and phonon scattering, the spin FET. We also demonstrate abilities of NEMO-VN2 for simulating nanodevices using GUI in Matlab. Finally, we display some typical simulation results obtained by this method, such as the current-voltage characteristics in 2D and 3D simulations. They enable a researcher to uncover the operation of quantum nanodevices and to predict their interesting performances.

Acknowledgment

This work is supported in part by the Grant-in-Aid for scientific research no. B2010-18-28 from VNU in HCM City.

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