Journal of Computer Networks and Communications

Hindawi

Special Issue on

Hardware Architectures for Advanced Error-Correction Decoders

CALL FOR PAPERS

Today error control coding (ECC) is involved in almost every communication and storage system: long-haul networks, space data-link protocols, digital TV, wireless communications, optical storage systems, magnetic storage systems, flash memories, and so forth.

However, with the improvement of processors, communication systems, and storage resources, three constraints force us to search for better decoding algorithms and implementations:

1) The technology scaling, which entails lowering the operating voltages and increasing the integration densities and, hence, increases the number of errors.

2) The increase in speed of both communication and processing, which requires high-throughput subsystems that do not slow down the whole application.

3) The need to reduce the devices' power consumption, a factor extremely important for mobile devices, which depend on their battery life.

So the primary challenge in ECC is the design of a decoder with the maximum error-correction capability and a throughput large enough not to bottleneck the system.

For this reason, the design of hardware solutions with both error-correction capability and high performance physical parameters (i.e., low silicon area, high throughput, and low power) is important to achieve the best solutions that serve the constraints of different scenarios.

Potential topics include but are not limited to the following:

- Modeling of different scenarios for error control coding: fault and statistical analysis
- Architectures for encoders and decoders with high performance such as LDPC, product codes, and polar codes
- Architectures for encoders and decoders for fault tolerance solutions
- Configurable platforms for computing parameters related with the design of different codes or emulating different communication and/or storage scenarios
- Design of platforms for testability in, for example, FPGA, ASIC, and SoC of different solutions
- Design or optimization of algorithms oriented to hardware-friendly implementations
- Integration of digital decoders in analog environments, design, implementation, and test of mixed circuits
- Procedures to optimize FPGA and/or ASIC designs of reconfigurable error control decoders

Authors can submit their manuscripts through the Manuscript Tracking System at http://mts.hindawi.com/submit/journals/jcnc/aecd/.

Lead Guest Editor
Kiran Gunnam, Santa Clara University, California, USA
kgunnam@ieee.org

Guest Editors
Francisco M. Garcia-Herrero, European University Miguel de Cervantes, Valladolid, Spain
fragarh2@gmail.com

Erbao Li, National University of Defence Technology, Changsha, China
lierbaonudt@gmail.com

Manuscript Due
Friday, 12 May 2017

First Round of Reviews
Friday, 4 August 2017

Publication Date
Friday, 29 September 2017