

## Research Article

# Current Control and Active Damping for Single Phase LCL-Filtered Grid Connected Inverter

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LCL filter has been widely used in the grid connected inverter, since it is effective in attenuation of the switching frequency harmonics in the inverter. However, the resonance in this filter causes stability problems and must be damped effectively to achieve stability. There are some methods to damp the resonance; one method is passive damping of resonance by adding a series resistor with the filter capacitor, but passive element reduces the inverter efficiency. Other method uses active damping (AD) by adding a proportional control loop of filter capacitor current, but this method needs additional sensor to measure filter capacitor current; moreover, when the control loops are digitally implemented, the computation delay in AD control loop will lead to some difficulties in choosing control parameters and maintaining system stability. This paper presents current control scheme for the grid connected inverter with the LCL filter. The proposed scheme ensures the control of injected current into grid with AD of the resonance in the LCL filter while keeping system stability and eliminating the effect of computation delay of the AD loop. An estimation of filter capacitor current with one step ahead is performed using the discrete time observer based on measuring the injected current. This reduces the cost and increases the robustness of the system. Proportional Resonant (PR) controller is used to control the injected current. Design of control system and choosing its parameters are studied and justified in details to ensure suitable performance with adequate stability margins. Simulation and experimental results show the effectiveness and the robustness of the proposed control scheme.

## 1. Introduction

With the rapid growth in global energy consumption, distributed power generation systems (DPGS) based on renewable energy sources such as solar energy and wind energy has attracted much more interest because of its environment friendly features, where they minimize greenhouse gas emissions and pollution. The grid connected voltage source inverter (VSI) plays an important role in DPGS, where it connects DPGS to the utility power grid. The inverter injects sinusoidal current to the grid, and this current must be synchronized with grid voltage [1, 2].

Conventional proportional integral PI controller has well-known drawbacks as inability to track sinusoidal reference without the steady state error in the stationary reference frame, so it needs to convert AC quantities to DC

quantities in d-q synchronous reference frame based on Park transformation, but this transformation increases the burden on DSP and it is difficult to be applied in single phase systems [3–5]. For those reasons, proportional resonant (PR) controller is more attractive since it provides infinite gain at grid fundamental frequency. So, it eliminates the steady state error and contributes in rejection of current harmonics caused by grid voltage. Also, it could be used in the single phase system without any transformations and has the ability of harmonics compensation [6–8].

Pulse Width Modulation (PWM) of VSI adds harmonics to grid current. So, a filter is needed to attenuate these harmonics. The LCL filter is more preferable than the L filter since it can provide higher attenuation ability, smaller volume, and lower cost compared with the conventional L filter [9–13]. However, the LCL filter generates high gain

peak at resonant frequency. So, any harmonics in grid voltage or inverter voltage close to resonance frequency will cause resonance in the injected current. In the literature, many resonance damping methods have been investigated. The simplest method is the passive damping which is implemented by adding a series resistor to the filter capacitor. This method increases the power loss in the inverter [6, 14]. For this reason, the active damping (AD) method is more attractive. The most widely used method to achieve AD is the proportional control loop (i.e., damping loop) of filter capacitor current [6, 15]. However, this method requires measurement of filter capacitor current. Moreover, some problems related to system stability will appear when the controller is digitally implemented due to computation and modulation delays, especially the delay of AD loop [16, 17]. It has been proved in [16, 17] that the AD loop is necessary when the resonant frequency  $\omega_{\text{res}}$  is smaller than one sixth of the sampling frequency  $\omega_s$  ( $\omega_{\text{res}} < \omega_s/6$ ). The system can be stable without the AD loop if  $\omega_{\text{res}} > \omega_s/6$ . If  $\omega_{\text{res}} = \omega_s/6$  (i.e., the boundary case), the system cannot be stable even with the AD loop. So, it is preferable to reduce the computation delay in the AD loop [16]. One solution proposed is to shift the capacitor current sample instant toward PWM update instant [16], but aliasing in measured current could happen. Some other techniques were proposed to avoid using additional current sensor and achieve damping [18, 19]. In [19], estimate the capacitor current was performed directly from the model depending on the derivative of the measured current, where inverter side current is used as feedback; however, differentiation of measured current will amplify the noise. Ideally, to estimate the capacitor current based on measuring grid side current, second derivative of the measured current is required. However, in practice second derivative could not be implemented due to noise amplification [18]. In [20], the second derivative of the measured current is replaced by the first-order high pass filter, but there would be some difficulties in choosing parameters of high pass filter to maintain stability. The full state feedback controller is used with 11 states' model in [21]. The robust observer using LMI criterion is implemented to achieve active damping in [22]. In [23], inverter side current is measured and capacitor current is estimated. The extended state observer (ESO) is used to estimate capacitor current and grid voltage but the effects of delays were not discussed. In [24], the full state observer is used with measuring grid side current and an additional lead lag network to compensate control delay. The notch filter to eliminate resonance harmonics components in inverter output voltage is used in [25]. However, the notch filter must be tuned carefully since erroneous tuning will compromise the LCL-filter stability.

In this paper, step by step design of grid current control is presented. The current control consists of the PR controller to control the grid current, and AD control loop to eliminate the resonance caused by the LCL filter. The AD control loop is implemented without the additional capacitor current sensor. Discrete time full state Luenberger observer is used to estimate capacitor current and avoid the computation delay in the AD loop. Design of control system parameters, to ensure suitable stability margins, and effects

of delay on the single-phase system are explained in the context of this paper. Simulation and experimental results show the effectiveness of the proposed control scheme.

This paper is organized as follows. In Section 2, the model of LCL filter and inverter is presented. It shows the necessity of damping the resonance in the LCL filter to achieve system stability. In Section 3, synchronous sampling and delay sources will be studied and modelled, and the effect of delay in the AD loop will be discussed. Section 4 presents choosing of controller parameters when the delay in the AD loop is cancelled, as well as the discrete time Luenberger observer is designed to avoid measuring filter capacitor current and the delay in the AD loop. In Section 5, simulation and experimental results are presented to validate the proposed control scheme. In Section 6, the conclusion is stated.

## 2. Modelling of the Inverter and LCL Filter

The closed loop for grid current control with AD based on measuring filter capacitor current is shown in Figure 1. The VSI is connected to the grid through the LCL filter. The LCL filter and inverter model could be written as follows:

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{dv_c}{dt} \\ \frac{di_i}{dt} \end{bmatrix}_{\dot{X}} = \begin{bmatrix} 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C} & 0 & \frac{1}{C} \\ 0 & \frac{1}{L_1} & 0 \end{bmatrix}_A \begin{bmatrix} i_g \\ v_c \\ i_i \end{bmatrix}_X + \begin{bmatrix} 0 \\ 0 \\ \frac{K_{\text{PWM}}}{L_1} \end{bmatrix}_B u_i + \begin{bmatrix} -\frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}_D v_g, \quad (1)$$

$$y = i_g = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}_C X, \quad (2)$$

where  $L_1$ ,  $L_2$ , and  $C$  are the filter parameters,  $i_i$ ,  $i_g$ ,  $v_c$ ,  $v_i$ , and  $v_g$  are, respectively, inverter side current, grid side injected current, filter capacitor voltage, inverter output voltage, and grid voltage,  $u_i$  is the control signal,  $K_{\text{PWM}}$  is the gain of the inverter and the modulator,  $v_i = K_{\text{PWM}}u_i$ . To track equations easily, Table 1 contains the main parameters definitions used in this paper. Taking the average model of the PWM modulator,  $K_{\text{PWM}}$  could be determined as  $K_{\text{PWM}} = V_{\text{DC}}/V_{\text{carrier}}$ . So, if  $V_{\text{carrier}}$  is scaled to equal  $V_{\text{DC}}$ , then  $K_{\text{PWM}} = 1$ . The system given by equations (1) and (2) could be modelled in S domain as the block diagram shown in Figure 2. The LCL resonance frequency is given by

$$\omega_{\text{res}} = 2\pi f_{\text{res}} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}}. \quad (3)$$

The grid side injected current can be written as follows:

$$i_g(s) = G_{i_g u_i}(s)v_i(s) + G_{i_g v_g}(s)v_g(s). \quad (4)$$

The transfer functions  $G_{i_g u_i}$  and  $G_{i_g v_g}$  could be expressed as follows:

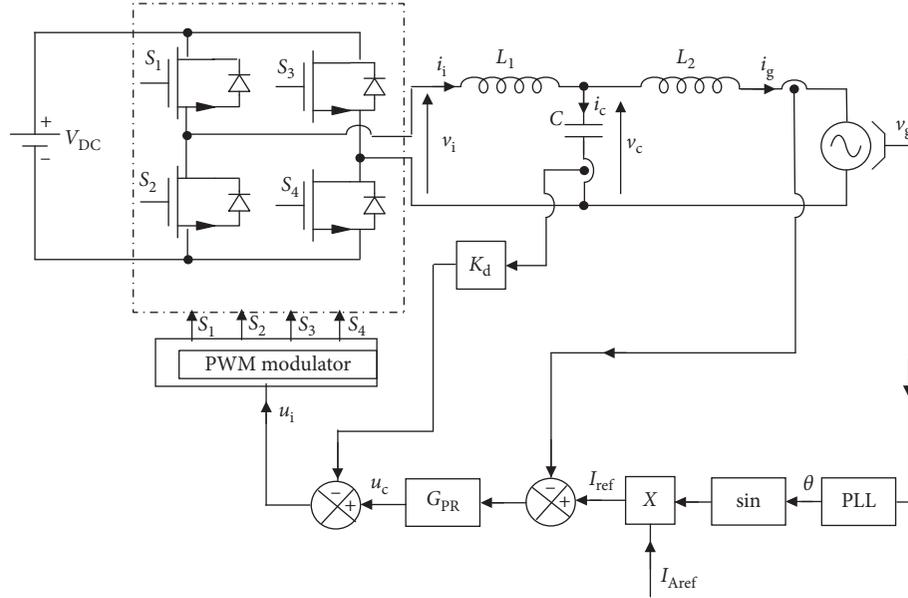


FIGURE 1: Grid current control scheme of grid connected VSI with active damping by measuring capacitor current.

TABLE 1: Parameter definition.

$L_1$	Inverter side inductance
$L_2$	Grid side inductance
$C$	Filter capacitor
$f_{res}$	Resonant frequency
$f_s$	Sampling frequency
$f_g$	Grid frequency
$v_g$	Grid voltage
$V_{DC}$	DC line voltage
$k_p$	Proportional gain
$v_i$	Inverter voltage
$v_c$	Capacitor voltage
$i_i$	Inverter side current
$i_g$	Grid side current
$u_i$	Control signal
$k_r$	Resonant gain
$K_d$	Active Damping gain
PM	Phase margin
GM	Gain margin
$\zeta$	Damping factor
$\omega_c$	Cut-off frequency
$K_{PWM}$	Inverter gain
$R_v$	Virtual resistor of active damping loop
$C_{eq}$	Equivalent capacitor of active damping loop
$R_{eq}$	Equivalent resistor of active damping loop

$$G_{i_g u_i}(s) = \frac{i_g(s)}{u_i(s)} = \frac{K_{PWM}}{L_1 L_2 C s (s^2 + \omega_{res}^2)}, \quad (5)$$

$$G_{i_g v_g}(s) = \frac{i_g(s)}{v_g(s)} = -\frac{1 + L_1 C s^2}{L_1 L_2 C s (s^2 + \omega_{res}^2)}. \quad (6)$$

From equation (4), the first term is the grid current caused by the inverter voltage and the second term is the grid current caused by the grid voltage, which plays the role of output disturbance of the controlled system and must be

rejected by the controller. The loop gain given in equations (5) and (6) has infinite gain at the resonant frequency  $\omega_{res}$ , so any harmonics in the grid voltage or inverter voltage close to resonant frequency will cause resonant current and instability. To solve this problem, a series resistor is added to the filter capacitor, but it will increase the power loss in the inverter and that is known as passive damping. For this reason, AD is more preferred, the most widely used method to achieve AD is by taking capacitor current  $i_c$  multiplied by proportional gain  $K_d$  and adding it to the input of the modulator, which is equivalent to add a parallel resistor (virtual resistor) to the filter capacitor [26, 27].

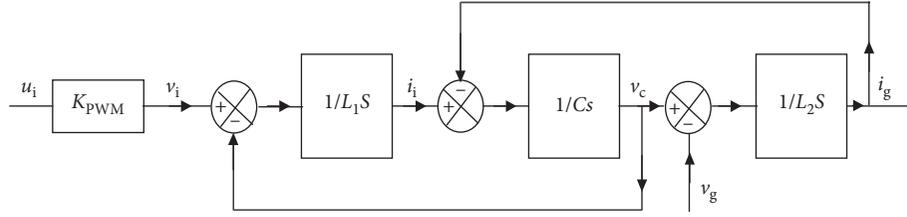
As shown in Figure 1, Phase Locked Loop PLL is used to estimate the angle  $\theta$  of the grid voltage. The signal  $I_{Aref}$  is the desired amplitude of the grid current to be injected into the grid. Grid current reference must be synchronized with the grid voltage. Then, the grid current reference could be generated as follows:

$$I_{ref} = I_{Aref} \sin(\theta). \quad (7)$$

Error signal  $e_1 = I_{ref} - i_g$  is the input of the current controller  $G_{PR}$ , which is the PR controller. Since it achieves high gain at the grid frequency, the PR controller high gain reduces the steady state error and rejects the effect of the grid voltage on the controlled current. The transfer function of the PR controller is given as follows:

$$G_{PR}(s) = k_p + k_r \frac{2\omega_g s}{s^2 + 2\omega_g s + \omega_g^2}. \quad (8)$$

The parameters  $k_p$ ,  $k_r$ , and  $\omega_g$  are proportional gain, resonant gain, and grid frequency, respectively. In equation (8), the gain of resonant term at  $\omega_g$  is  $k_r$ , and the controller has some margins around  $\omega_g$ , where the gain of resonant term at  $\omega_g \pm \omega_1$  is  $k_r/\sqrt{2}$ , where  $\omega_1$  could be chosen  $1\%\omega_g$  [3, 28, 29].

FIGURE 2: Block diagram of the inverter and LCL filter in  $S$  domain.

### 3. Delay Sources and Its Effect on Active Damping

When the current controller of VSI is digitally implemented, synchronous sampling of the measured current is preferred where samples are taken when the PWM counter of the DSP reaches its maximum and/or minimum value [30]. This sampling technique avoids sampling the harmonics in measured current caused by switching and gets the average value of the current. Moreover, it avoids switching noise or electromagnetic interference (EMI) when the transistors switch on or off [1, 31].

Figure 3 shows the digital control process; bipolar PWM is used to drive VSI. The triangular signal has normalized amplitude carrier. At time instant  $k$ , the interrupt of the PWM occurs and the PWM comparison register is updated according to duty ratio  $D_k$ , simultaneously the analog to digital converter (ADC) takes the measurements. Then, the controller starts computing the convenient duty ratio  $D_{k+1}$  and the computation must be finished before time instant  $k+1$ , where the PWM comparison register will be updated again, which means that the digital controller produces delay equal to one sampling period. This delay is commonly called computation delay and it is modelled in  $S$  domain as  $G_{cd}(s) = e^{-T_s S}$ . After updating the PWM comparison register, it is compared with the carrier to generate the duty ratio. This behavior could be modelled by ZOH as follows:

$$G_h(s) = \frac{1 - e^{-sT_s}}{s}. \quad (9)$$

In frequency domain,  $s = j\omega$ ; then,

$$G_h(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega} = \frac{e^{0.5*j\omega T_s} - e^{-0.5*j\omega T_s}}{j\omega} e^{-0.5*j\omega T_s} \approx T_s e^{-0.5*j\omega T_s}. \quad (10)$$

Since the spectrum of a sampled signal, which is the input of the ZOH, is divided by  $T_s$ , then the delay caused by modulation is  $G_{md}(s) = e^{-0.5sT_s}$ , which means the modulation delay equals half sampling period.

Taking the delay into account makes the control design more complex. Figure 4 shows the block diagram of the control system, which takes into account the delay. The transfer functions  $G_{cd1}$  and  $G_{cd2}$  are, respectively, the computation delay in the AD control loop and in the grid current control loop. Generally,  $G_{cd1} = G_{cd2} = e^{-T_s S}$ . From the block diagram, it could be found that

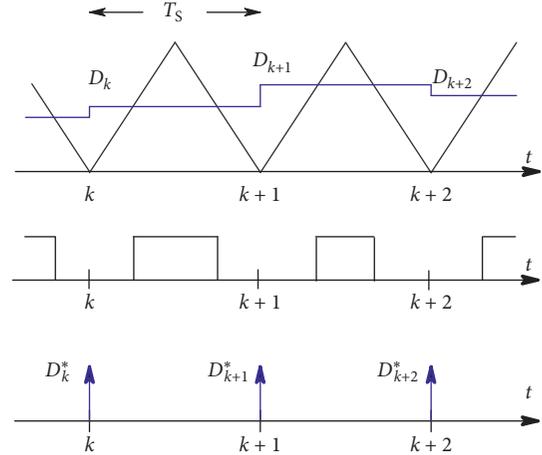


FIGURE 3: Digital control process to drive VSI using bipolar PWM.

$$i_g = \frac{G_{ol}(s)}{1 + G_{ol}(s)} I_{ref} + \frac{G_g(s)}{1 + G_{ol}(s)} v_g(s). \quad (11)$$

The transfer function  $G_{ol}$  is the open loop transfer function from grid current error  $e_1$  to grid current  $i_g$  when  $v_g = 0$ .  $G_g$  is the open loop transfer function from grid voltage to grid current when  $e_1 = 0$ .  $G_g$  and  $G_{ol}$  are given by equations (12) and (13), where delays are included in  $S$  domain [32]:

$$G_{ol} = \frac{G_{PR} G_{cd2} G_{md} K_{PWM}}{L_1 L_2 C s (s^2 + (K_d K_{PWM} G_{md} G_{cd1} / L_1) s + \omega_{res}^2)}, \quad (12)$$

$$G_g = \frac{C L_1 s^2 + C K_d K_{PWM} G_{md} G_{cd1} s + 1}{L_1 L_2 C s (s^2 + (K_d K_{PWM} G_{md} G_{cd1} / L_1) s + \omega_{res}^2)}. \quad (13)$$

It could be seen from equation (11) that the stability of the system depends on the open loop transfer function  $G_{ol}$ . The AD loop adds a term related to the AD gain  $K_d$  in the denominator of the open loop transfer function. This parameter  $K_d$  could be tuned together with the control parameters to achieve suitable damping, good stability margins, and good current performance.

Without the AD loop (i.e.,  $K_d = 0$ ), the system can be stable if the resonant frequency is greater than  $\omega_s/6$ , where  $\omega_s$  is the sampling frequency [17, 33]. This is because of the delay in the system  $G_{cd2} G_{md} = e^{-1.5T_s S}$ , which causes a phase lag in the open loop transfer function  $G_{ol}$  and will contribute a  $-90^\circ$  in phase at  $\omega_s/6$ . So, if the resonant frequency is greater than  $\omega_s/6$ , then the phase of the open loop will cut

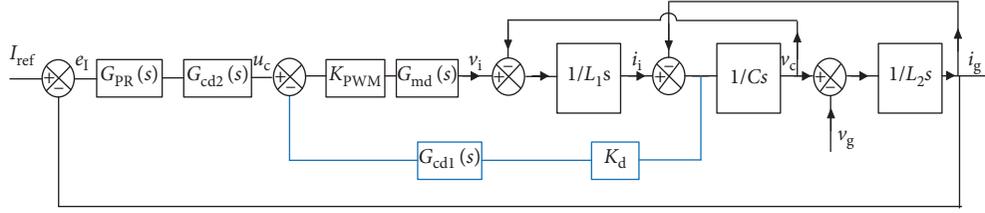


FIGURE 4: Block diagram of the control system including delay with AD by measuring capacitor current.

$-180^\circ$  at  $\omega_s/6$ . Since the proportional resonant controller is equivalent to proportional gain  $k_p$  at high frequency, the system can be stable by choosing a suitable controller gain without the need of the AD loop. Figure 5 shows the bode plot of  $G_{ol}$  without the AD loop, with and without considering the delay.

Indeed, high resonant frequency will cause higher PWM current ripples. Good attenuation for PWM current ripple means reducing resonant frequency. So, if  $\omega_{res} \leq \omega_s/6$ , the AD loop is essential to achieve system stability with good PWM harmonics attenuation.

When the delay is taken into account, the AD loop is equivalent to a virtual impedance instead of the virtual resistor connected in parallel with the filter capacitor [16, 26, 27]. By replacing the feedback from capacitor current  $i_c$  to capacitor voltage  $v_c$  and adding the effect of the active damping loop to the output of  $1/L_1s$ , as shown in Figure 6,

$$Z_{eq} = \frac{L_1}{CK_d K_{PWM} G_{md} G_{cd1}} = \frac{L_1}{CK_d K_{PWM}} e^{1.5T_s s} = R_v e^{1.5T_s s}. \quad (14)$$

Virtual impedance can be introduced as resistor  $R_{eq}$  and capacitor  $C_{eq}$  in parallel with  $C$ , as shown in Figure 7. Replacing  $s = j\omega$  in equation (14), then

$$Z_{eq} = R_v e^{1.5T_s s} = R_v \cos(1.5\omega T_s) + j \sin(1.5\omega T_s) = R_{eq} \parallel \frac{1}{j\omega C_{eq}}. \quad (15)$$

$R_{eq}$  and  $C_{eq}$  are determined as

$$R_{eq} = \frac{R_v}{\cos(1.5\omega T_s)}, \quad (16)$$

$$j \frac{1}{\omega C_{eq}} = -j \frac{R_v}{\sin(1.5\omega T_s)}, \quad (17)$$

where  $R_{eq}$  plays the main role in damping the resonant frequency peak. However, it must be noted that the equivalent resistor can go negative for the frequency  $\omega > \omega_s/6$ . And the negative equivalent capacitor  $C_{eq}$  will change the resonant frequency of the system. So, increasing AD gain  $K_d$  will increase the actual resonant frequency. If  $\omega_{res}$  is equal or closed to  $\omega_s/6$ , then a small change in  $K_d$  will shift the resonant frequency to be in the negative resistor region. This negative resistor will cause two unstable open loop poles and the system will be nonminimum phase system, which should preferably be avoided if a fast-dynamic response is demanded [18]. According to [16, 17], the system can be stable if

$\omega_{res} = \omega_s/6$ , and it is difficult to achieve good damping if  $\omega_{res}$  is close to  $\omega_s/6$ . From equation (16), it could be seen that if the AD loop delay  $G_{cd1} = 1$  (no computation delay in AD loop), negative resistor will appear at  $\omega > \omega_s/2$  which is far from  $\omega_s/6$  and that means the possibility of extending  $K_d$  range and achieving good damping and avoiding unstable poles pair.

#### 4. Control Design

As seen previously it is better to eliminate AD loop computation delay. Suppose that AD loop computation delay is cancelled (i.e.,  $G_{cd1} = 1$ ); then, the open loop transfer function in equation (12) is given as follows:

$$G_{ol} = \frac{G_{PR} K_{PWM} e^{-1.5T_s s}}{L_1 L_2 C s (s^2 + (K_d K_{PWM} e^{-0.5T_s s} / L_1) s + \omega_{res}^2)}. \quad (18)$$

In general, the cutoff frequency  $\omega_c$  should be chosen higher enough than grid frequency to achieve fast dynamic response, at the same time should be less enough than the resonant frequency to achieve good stability margins [6, 29, 34]. The LCL filter can be approximated by the L filter, where  $L = L_1 + L_2$  at frequencies lower than resonant frequency (i.e., the capacitor current can be neglected). At the same time, the proportional resonant controller can be approximated by proportional gain  $k_p$ . So, the open loop gain can be approximated as follows:

$$|G_{ol}(s)| \approx \left| \frac{k_p K_{PWM} e^{-1.5T_s s}}{(L_1 + L_2) s} \right|. \quad (19)$$

It could be seen that choosing the cutoff frequency  $\omega_c$  depends on  $k_p$  only. By replacing  $s = j\omega_c$  and taking  $|G_{ol}(j\omega_c)| = 1$  in equation (19), then  $k_p$  can be found as follows:

$$k_p = \frac{(L_1 + L_2) \omega_c}{K_{PWM}}. \quad (20)$$

The gain margin (GM) of the open loop depends on AD gain  $K_d$ . GM in dB is  $GM = -20 \log(|G_{ol}(j\omega_0)|)$  and  $\omega_0$  is the frequency, where the phase of the open loop cut  $-180^\circ$ .  $\omega_0$  can change with  $K_d$  according to equation (21), where equation (21) can be obtained from  $\angle G_{ol}(j\omega_0) = -\pi$ :

$$\frac{\pi}{2} - 1.5T_s \omega_0 - a \tan \left( \frac{K_d K_{PWM} \omega_0 \cos(0.5T_s \omega_0)}{L_1 (\omega_{res}^2 - \omega_0^2) + K_d K_{PWM} \omega_0 \sin(0.5T_s \omega_0)} \right) = 0. \quad (21)$$

Then, GM at  $\omega_0$  is given by

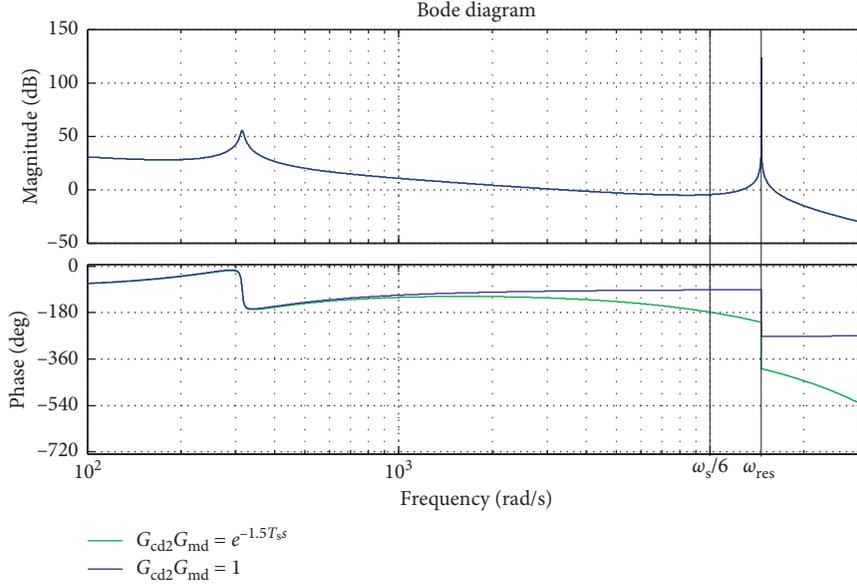


FIGURE 5: Bode plot of  $G_{ol}$  without the AD loop, with and without considering the delay when  $\omega_{res} > \omega_s/6$ .

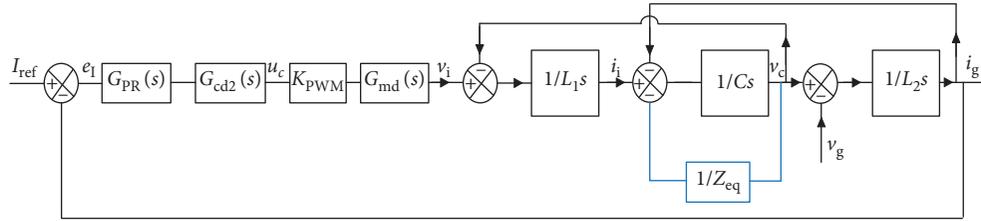


FIGURE 6: Block diagram of the control system with equivalent virtual impedance of the AD loop.

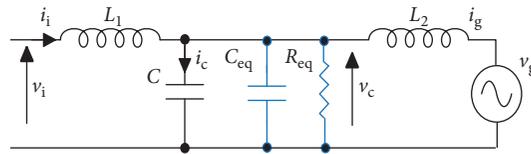


FIGURE 7: Equivalent circuit of the virtual impedance.

$$GM = -20 \log \left( \frac{k_p K_{PWM} / L_2 C \omega_0}{\sqrt{(L_1 (\omega_{res}^2 - \omega_0^2) + K_d K_{PWM} \omega_0 \sin(0.5T_s \omega_0))^2 + (K_d K_{PWM} \omega_0 \cos(0.5T_s \omega_0))^2}} \right). \quad (22)$$

Figure 8 shows the open loop bode plot for different damping gain values  $K_d$ ; then,  $K_d$  can be tuned to achieve good damping and suitable gain margin ( $GM > 3$  dB). It should be noted that increasing the damping gain too much will affect the phase margin badly.

After choosing suitable values for  $k_p$  and  $K_d$  to guarantee suitable cutoff frequency and good gain margin, then phase margin (PM) can be manipulated by changing  $k_p$ . Commonly, PM is chosen to be ( $PM > 45^\circ$ ).  $PM = \pi + \angle G_{ol}(j\omega_c)$  then from equation (18) PM could be calculated as follows:

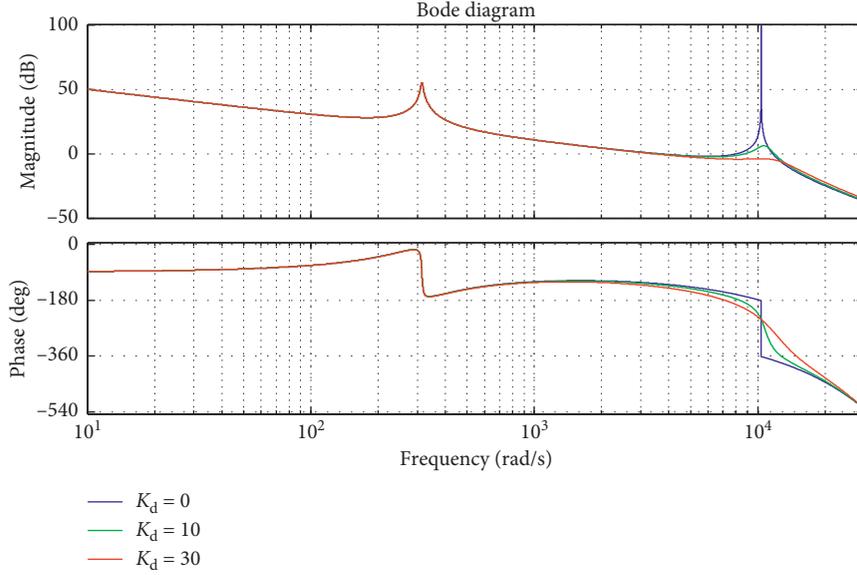


FIGURE 8: Bode plot of the open loop for different damping gains  $K_d$  and  $k_p = 25$ ,  $k_r = 1500$ ,  $f_{res} = 1.65$  kHz, and  $f_s = 10$  kHz.

$$PM = \frac{\pi}{2} - 1.5T_s\omega_c + a \tan\left(\frac{2\omega_i\omega_c(k_r + k_p)}{k_p(\omega_g^2 - \omega_c^2)}\right) - a \tan\left(\frac{2\omega_i\omega_c}{(\omega_g^2 - \omega_c^2)}\right) - a \tan\left(\frac{K_d K_{PWM}\omega_c \cos(0.5T_s\omega_c)}{L_1(\omega_{res}^2 - \omega_c^2) + K_d K_{PWM}\omega_c \sin(0.5T_s\omega_c)}\right). \quad (23)$$

Continuous time system in equation (1) could be described in discrete time with ZOH as follows:

$$X(k+1) = A_d X(k) + B_d u_1(k) + D_d v_g(k), \quad (24)$$

where  $A_d = e^{AT_s}$ ,  $B_d = A^{-1}(A_d - I_3)B$ , and  $D_d = A^{-1}(A_d - I_3)D$ .

The system is observable by measuring grid current  $i_g$  since  $\text{rank}(O) = 3$ , where  $O$  is the observability matrix given as follows:

$$O = \begin{bmatrix} C \\ CA_d \\ CA_d^2 \end{bmatrix}. \quad (25)$$

To achieve AD without measuring the capacitor current, capacitor current can be estimated using full state Luenberger-like observer given as follows:

$$\hat{X}(k+1) = A_o \hat{X}(k) + B_o u_1(k) + D_o v_g(k) + LC(X(k) - \hat{X}(k)), \quad (26)$$

where  $A_o$ ,  $B_o$ , and  $D_o$  are the observer matrices and  $L = [l_1 \ l_2 \ l_3]^T$  is the observer gain vector. It could be seen that the

observer in equation (26) has another benefit of providing one step prediction for current estimation since it estimates state space vector at time instance  $k+1$  using samples of time instance  $k$ , which means avoiding the delay in the AD loop, as shown in Figure 9; as seen previously, it is preferable to cancel this delay for system stabilization.

$K_d \hat{i}_c$  is taken as feedback to the input of the inverter. It is a state feedback with gain  $K$ , where  $K_d \hat{i}_c = K_d(\hat{i}_1 - \hat{i}_g) = K\hat{X}$  and the gain vector  $K = [-K_d, 0, K_d]$ .

If the observer matrices match the system matrices (i.e.,  $A_o = A_d$ ,  $B_o = B_d$ , and  $D_o = D_d$ ), then from equations (24) and (26) the dynamic of the observer error is given as follows:

$$\tilde{X}(k+1) = X(k+1) - \hat{X}(k+1) = (A_d - LC)\tilde{X}(k). \quad (27)$$

Based on separation principle, the AD loop gain and observer can be designed separately. The observer gain vector should be chosen in a way that does not affect the bandwidth of the system [24, 35]. The characteristic equation of the observer error is third-order polynomial and has three poles, which can be located arbitrary in  $z$  plan since the system is observable. The poles are chosen as follows:

$$\det(zI_3 - A_d - C_d K) = (z - e^{-\omega_o T_s}) \left( z - e^{-(\zeta - j\sqrt{1-\zeta^2})\omega_o T_s} \right) \left( z - e^{-(\zeta + j\sqrt{1-\zeta^2})\omega_o T_s} \right), \quad (28)$$

which consists of one real pole and two complex conjugated poles. The poles of the observer should be chosen at least

twice faster than the dynamic of the system. One of the poles is dominant one and the other two conjugated poles should

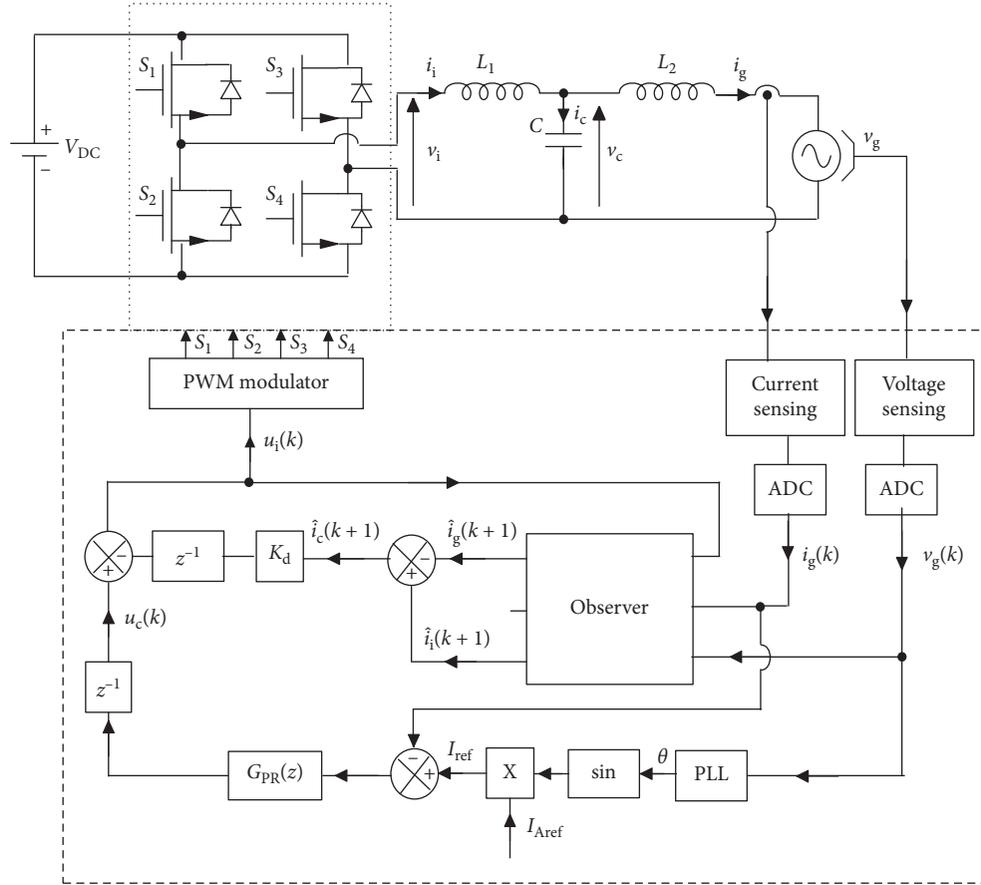


FIGURE 9: Block diagram of the system with the observer to achieve AD.

be faster than the dominant pole. These two poles are equivalent to a second order system whose characteristic are determined by  $(\zeta, \omega_{o2})$ ; the observer dynamic is determined by its dominant pole.

The proportional resonant controller is commonly discretized using Tustin transform with prewarping, since it provides good approximation for this controller around grid frequency [6, 36]:

$$G_{PR}(z) = G_{PR}(s)_{s=\omega_g/\tan(\omega_{gr}T_s/2)}((1-z)^{-1}/(1+z)^{-1}) \quad (29)$$

The control design of the system can be summarized step by step as follows:

- Determine cutoff frequency  $\omega_c$  by tuning  $k_p$  according to equation (20)
- Determine gain margin GM by solving equations (21) and (22) to find proper damping factor  $K_d$
- Determine phase margin PM by tuning  $k_r$  according to equation (23)
- Determine observer gain to place the observer poles in proper locations according to equation (28)
- Discretize the PR controller using Tustin transform with prewarping using equation (29)

## 5. Simulation and Experimental Results

Simulations and experiments were carried out to validate the proposed control scheme. The simulations are performed using Matlab/Simulink. The experiments are performed using 1 kW grid connected inverter with the LCL filter implemented in the lab. The system parameters used in simulations and experiments are listed in Table 2.

As mentioned previously, cutoff frequency  $\omega_c$  should be higher enough than grid frequency  $\omega_g$  to achieve fast dynamic response. So, it could be chosen as  $\omega_c = 10\omega_g$ . Then, from equation (20),  $k_p = 25$ . AD gain  $K_d$  and resonance gain  $k_r$  could be determined to achieve GM > 3 dB and PM > 45°. By solving equations (21)–(23) numerically using Matlab, it could be found that  $k_r = 1500$  and  $K_d = 30$  achieve GM = 4.2 and PM = 45°.

Dominant pole of the observer  $z_1 = e^{-\omega_{o1}T_s}$  is chosen to be three times faster than system dynamic  $\omega_{o1} = 3\omega_c$ , if  $(\zeta, \omega_{o2})$  are chosen as  $\omega_{o2} = 5\omega_c$  and  $\zeta = 0.7$ ; then, the equivalent part determined by the other two conjugated poles  $z_2$  and  $z_3$  is faster than the dominant pole.

Figure 10 shows the simulation results at full load condition, where inverter side current, injected current, and grid voltage are illustrated. It could be seen that

TABLE 2: LCL filter parameters and grid characteristics.

Inverter side inductance $L_1$	6 mH
Grid side inductance $L_2$	2.1 mH
Filter capacitor $C$	6 $\mu$ F
Resonant frequency $f_{res}$	1.65 kHz
Sampling frequency $f_s$	10 kHz
Grid frequency $f_g$	50 Hz
Grid voltage $v_g$	220 Vrms
DC line voltage $V_{DC}$	380 V
Power $P$	1 kW

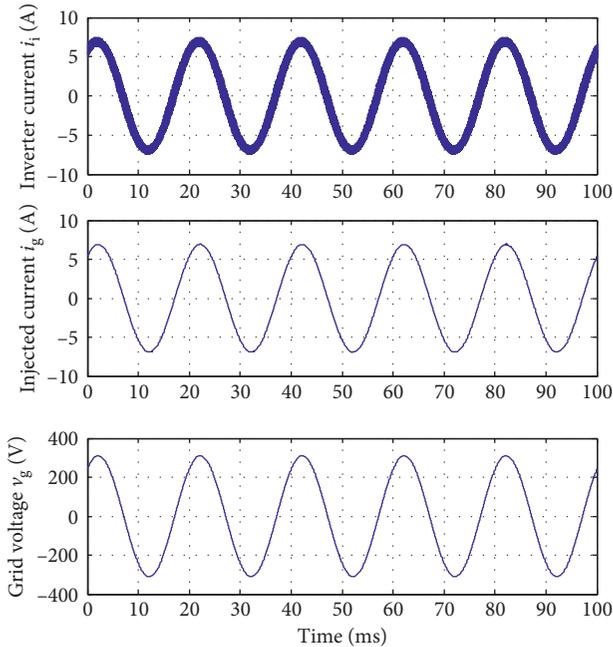


FIGURE 10: Simulation result at full load conditions.

synchronization is achieved and tracking the reference signal is performed with the neglected steady state error, and because of using the PR controller, which produces high gain at grid frequency, it eliminates the steady state error in the injected current.

The effectiveness of the control method is studied by dropping the reference current from full load condition to half load conditions. Figure 11 shows the simulation result of this case. It could be seen that, at time 55 ms, when the reference signal amplitude dropped from 7 A to 3.5 A, the resonance in the injected current is damped effectively, and the injected current has a fast dynamic response in tracking the new reference.

Figure 12 shows AD loop capability to stabilize the system and damp the resonance in the injected current. When the AD loop is disabled at time 50 ms, the resonance in the injected current appears.

To study the robustness of the proposed method against parameter uncertainties, each parameter of  $L_1$ ,  $L_2$ , and  $C$  is changed in a range  $[-20\%, 20\%]$  of its nominal value, and system stability is studied against those changes. Figure 13 shows the closed loop poles map of the system, where all

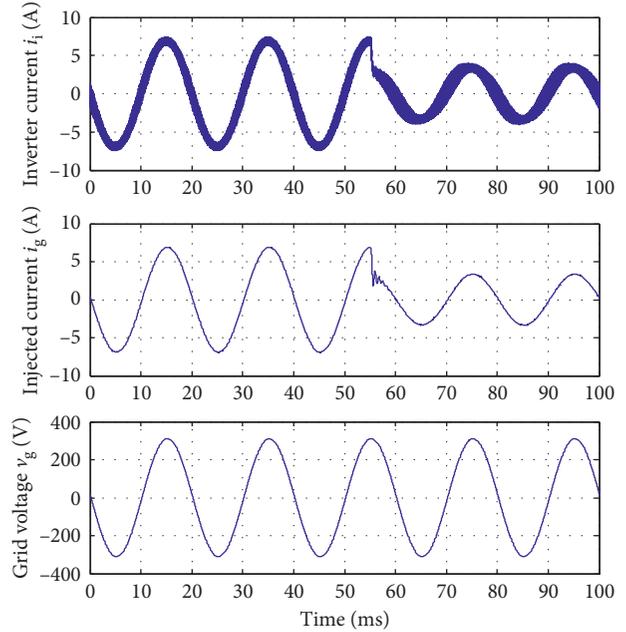


FIGURE 11: Simulation result when current reference drops to half load conditions from full load conditions.

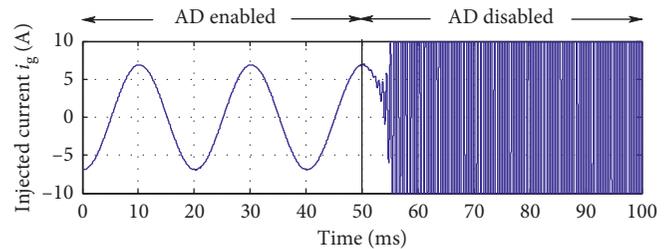


FIGURE 12: Simulation result when AD is disabled.

poles stay inside the unit circle. Simulation results show the ability of the control scheme to maintain stability despite of wide range of uncertainty.

In practice, the system with the PR current controller and AD method with the discrete time Luenberger observer is implemented using FPGA cyclone II kit, and the injected current is measured using LEM LA 55-P hall effect current sensor, and the grid voltage is measured using a transformer. Synchronous sampling technique is used, where switching frequency equals sampling frequency  $f_s = 10$  kHz. The same filter and control parameters used in simulation are used in practice. The same cases studied in simulation are applied in experiment.

The experiment results are shown in Figures 14 and 15, where Figure 14 shows the experiment result of the grid voltage, injected current, and inverter side current at full load conditions, and Figure 15 shows the experimental result of the control process when current reference dropped from full load conditions to half load conditions; it could be shown that the results of the simulation and experimental are close. The results show the powerful performance of the control method in practice.

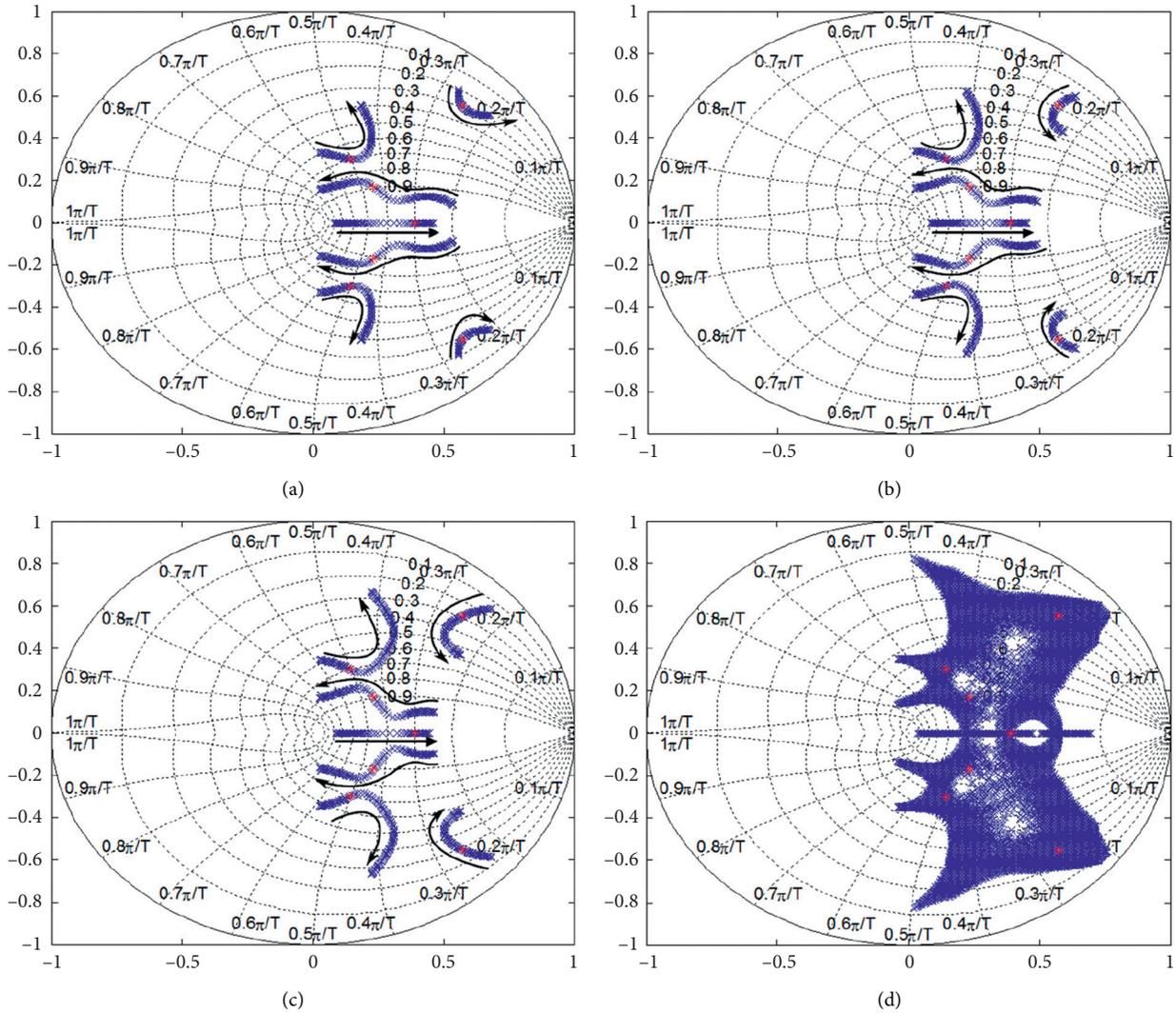


FIGURE 13: Closed loop poles' map in the  $z$ -plane of the overall system when varying the LCL elements in range  $[-20\%, 20\%]$  of their nominal values, where the red points are nominal places of the poles. (a)  $L_1$  changed in range  $[4.8, 7.2]$ mH, (b)  $L_2$  changed in range  $[1.7, 2.5]$ mH, (c)  $C$  changed in range  $[4.8, 7.2]$  $\mu$ F, and (d)  $L_1$ ,  $L_2$ , and  $C$  changed together each one in the range  $[-20\%, 20\%]$  of its nominal value.

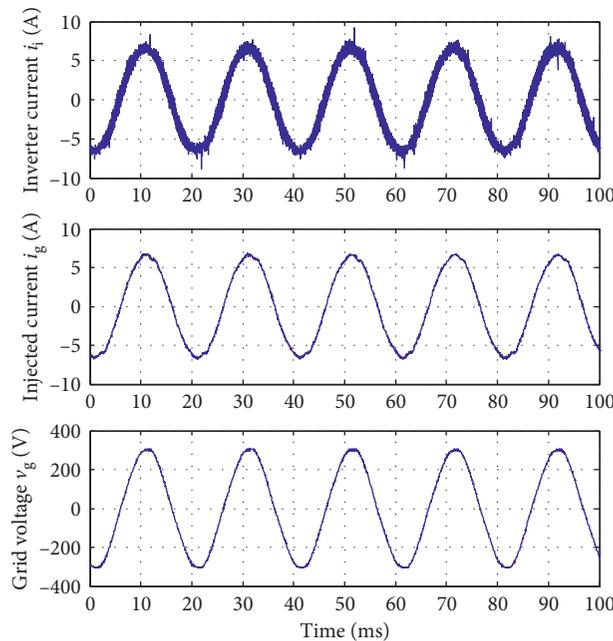


FIGURE 14: Experimental result at full load conditions.

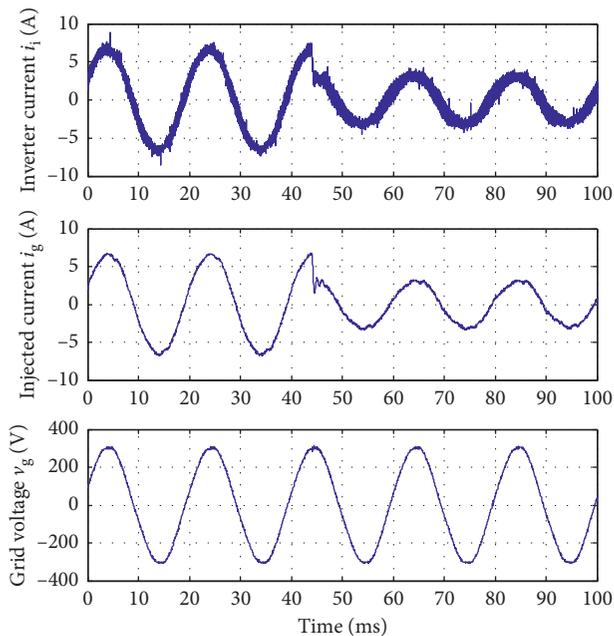


FIGURE 15: Experimental result when current reference drops to half load condition from full load condition.

## 6. Conclusion

In this paper, a control scheme for the grid connected inverter with the LCL filter is presented. The control scheme is composed of two control loops. The first control loop using the PR controller ensures the grid current control. The second loop, AD loop, eliminates the LCL resonance and ensures the stability. The AD loop is implemented using the discrete time Luenberger observer. Simulation and experimental results show the effectiveness of the proposed control scheme. The proposed control scheme eliminates the computation delay in the AD loop, which has a bad effect on system stability, reducing cost since there is no need to use the additional current sensor. The parameters of the control scheme is chosen and discussed in detail. The results show that when the inverter works in full load conditions, the injected current tracks the reference signal with the neglected steady state error; when the system is tested under hard transient in reference signal from full load condition to half load conditions, the results show the effectiveness in damping the resonant frequency and a fast dynamic response in tracking the reference signal again. In future works, extending the proposed control scheme for the three-phase inverter is planned and the robustness in the proposed control scheme against grid impedance variation and model uncertainty is studied.

## Data Availability

The data used to support the findings of this study are included within the article.

## Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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