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Research Article

Thermomechanical Impact of Polyurethane Potting on Gun Launched Electronics

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Electronics packages in precision guided munitions are used in guidance and control units, mission computers, and fuze-safe-and-arm devices. They are subjected to high *g*-loads during gun launch, pyrotechnic shocks during flight, and high *g*-loads upon impact with hard targets. To enhance survivability, many electronics packages are potted after assembly. The purpose of the potting is to provide additional structural support and shock damping. Researchers at the US Army recently completed a series of dynamic mechanical tests on a urethane-based potting material to assess its behavior in an electronics assembly during gun launch and under varying thermal launch conditions. This paper will discuss the thermomechanical properties of the potting material as well as simulation efforts to determine the suitability of this potting compound for gun launched electronics. Simulation results will compare stresses and displacements for a simplified electronics package with and without full potting. An evaluation of the advantages and consequences of potting electronics in munitions systems will also be discussed.

1. Introduction

The weapons community currently has a strong need to design and field reliable electronics for precision munitions. These electronic systems and subsystems are used in guidance and control units, mission computers, sensors, and fuze-safe-and-arm devices. While modern technology has evolved to produce high-precision and highly reliable electronic systems, they are not constructed to survive the harsh environments of gun launch. The current issues faced are high vibratory loads, high-*g*-accelerations, pyrotechnic shocks during flight, and high-impact loads through hard targets. During each phase, these electronics are expected to retain full functionality. In an effort to mitigate the severity of these loads, electronic components are often potted to enhance structural support, dampen large dynamic vibrations due to gun launch [1]. Electronic components are also potted in order to protect sensitive equipment from environmental conditions (such as moisture), as well as to insulate electrical leads in the event that other components fail [2].

Potting of electronics has become one of the most viable and cost-effective solutions to enhance electronic package survivability. It is important that engineers understand the severity of gun launch and the harsh thermal loads to which the potting material and the potted assemblies are subjected to [3]. To improve tolerance to high-shock and vibratory loads, viscoelastic materials are traditionally employed as potting compounds. This is because they possess both the ability to store and dissipate energy. The relative contribution of each component dictates the material's effectiveness as a shock dampener [4].

Projectile live-fire testing is customarily used to build reliability and optimize design. However, this testing is costly and, in many cases, impractical for defining gun-launch-induced stresses on many organic materials used in subassemblies. For this reason, structural analysts employ finite element analyses (FEAs) to predict the impact of gun launch on these subassemblies and components. Dynamic FEA helps to build reliability and provides significant insight into systems survivability for munitions designers. Moreover, it saves programs millions of dollars in testing, as multiple designs and materials can then be simulated in a matter of days and for a fraction of the cost of live-fire testing. By coupling this modeling effort with testing throughout the life of a program, both time and money can be saved in the long run.

The fidelity of a simulation is related to the fidelity of the material models that are employed. The constitutive models are based on mechanical test data, which reflect the material behavior under varying load profiles. In addition to mechanical testing, thermal characterizations of materials are also required, since projectile flight time contains thermal loading on internal and external components.

Most studies on the use of FEA to model-potted electronics focus on the thermomechanical impact of potting materials on the integrated circuits and electronic components [3, 5, 6]. It has been well documented that under high thermal loads, the potting material imparts large stresses on the electronic components. These stresses derive from coefficient of thermal expansion (CTE) mismatches between the potting material and the electronic components, as well as from variations in the potting material stiffness as operating temperatures traverse the glass transition temperature (T_g).

This paper will detail the development of finite element constitutive material models, the dynamic structural behavior of the potted materials, as well as the impact of gun launch on a potted electronic assembly. A previous study compared potted to unpotted electronics at ambient temperatures assuming that the potting did not stick to key components [7]. In the previous study, the stresses in the chips were higher for a ringed model (unpotted-ring represent elastomeric type o-ring components) compared to a fully potted model. For both models, stresses were within acceptable bounds for ambient temperature. In this study, similar comparisons are made at temperature extremes to assess differences with the potting in the glassy and rubbery phase. This study also assumes that the potting adheres to the chips, the board, and the can.

2. Potting Testing and Modelling

2.1. Material Testing. A polyurethane-based potting with a shore *D* hardness of 45 was acquired from Alchemie Ltd (trade name Alchemix). Due to the nature of the application, the formulation is proprietary. Dynamic Mechanical Analyses (DMAs) operated in 3-point-bend mode. Uniaxial tension and uniaxial compression testing were performed by the US Army ARDEC. The DMA samples were subjected to multiple frequency oscillations under varying temperatures from −101°C to 71°C. The uniaxial compression and tension tests were performed on ASTM D638 type 1 tensile bars and ASTM D695 compression prisms. These samples were conditioned and tested at −51°C, ambient, and 71°C.

2.2. Mechanical Behavior of Filled Potting. The uniaxial data collected suggests that within the strain range analyzed there is significant change in mechanical behavior as temperature varies from −51°C to 71°C. This is a consequence of testing through the materials glass transition (−10°C). As with most polymers the material exhibits glassy behavior at low temperatures below its glass transition and rubbery behavior at high temperatures above its glass transition. The strength data acquired demonstrates this: at high temperatures the material strength drops to 30% of its strength at ambient

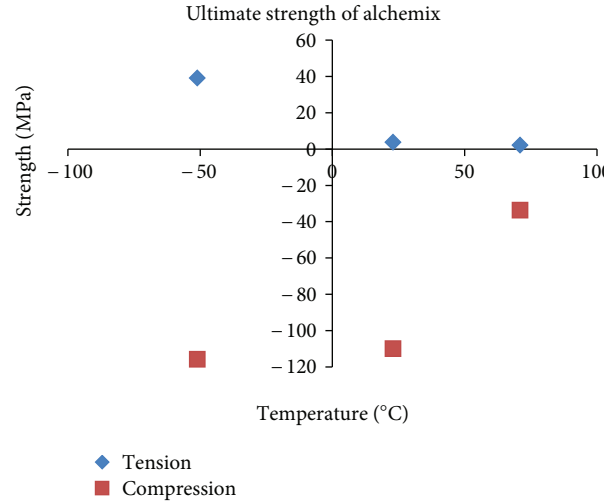


Figure 1: Ultimate strength of Alchemix in tension and compression.

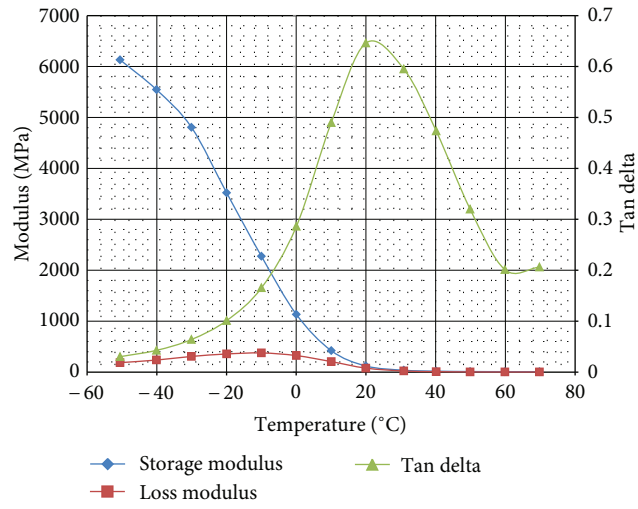


Figure 2: 3-point-bend DMA.

under compressive loading and down to 60% of its ambient strength under tensile loading. At low temperatures the strength of the material increases by 5% of its ambient strength under compressive loading and 90% of its ambient strength under tensile loading. Figure 1 displays the strength data for Alchemix in tension and compression at varying temperatures.

DMA of the potting material also reveals a significant change in mechanical behavior with temperature. Figure 2 shows that the storage modulus decreases significantly as temperature increases from −101°C to 71°C. Again, this is due to the material's phase transition from glassy to rubbery. Below the glass transition temperature molecular mobility is limited yielding an increase in material stiffness and stored energy. Close to and above the glass transition temperature polymer chains are flexible and mobile [4].

Also observed from DMA testing is that the peak of the tan delta curve occurs at 20°C. Tan delta is a measure of how the material performs as a shock dampener. The higher the

tan delta, the more effective the material is as a dampener. From this data the material will perform best at 20°C. The loss modulus is a depiction of the material's viscous behavior and ability to dissipate energy. The amplitude of the curve provides information on molecular mobility. The peak of the curve represents the temperature at which there is increased chain movement. This typically signals a phase transition in the material. The peak of the loss modulus is chosen to represent the glass transition.

2.3. Potting Constitutive Models. Linear elastic and viscoelastic models were parameterized using the mechanical test data acquired. The linear viscoelasticity model is chosen because the potting is considered confined by the electronics housing and thus will be subjected to finite strains. If the assembly had not been confined, a nonlinear elastic/viscoelastic material model would be more appropriate. Although the material is confined, the gun launch load applied in the finite element analysis (FEA) occurs within 15 ms imparting high-frequency forces on the potting material. During this dynamic event, the change in frequency will impact the molecular mobility of polymer chains and overall viscosity of material. For most materials, this essentially leads to a stiffer material at high frequencies. The viscoelastic constitutive model is expected to capture the dynamic changes in overall structural behavior. The input for time domain viscoelasticity is the normalized shear modulus data as a function of frequency which is directly inputted in the property module in tabular form. The shear modulus is determined by (1):

$$G = \frac{E}{2 \cdot (1 + \mu)}, \tag{1}$$

where μ is Poisson's ratio and E is the elastic modulus (measured using DMA). Tables 1, 2, and 3 display the data inputted into ABAQUS for calibration at cold (−40°C), ambient, and hot (60°C) temperatures, respectively.

ωg^* real, ωg^* imaginary, ωk^* real, and ωk^* imaginary represent the frequency-dependant real and imaginary components for the shear and bulk moduli. "ω" (omega) represents the circular frequency.

For this analysis, the potting material is assumed to be isotropic and incompressible ($\nu = 0.5$). Under this assumption, bulk modulus approaches infinite and ABAQUS considers it a negligible quantity. Another assumption is that the calculated shear modulus at 1 Hz represents the long-term shear modulus (G_∞). With this assumption the parameters ωk^* real, ωg^* imaginary are inputted into ABAQUS using ωg^* real $= Gl/G\infty$ and ωg^* imaginary $= 1 - G_s/G_\infty$ [8]. G_l and G_s represent the loss and storage shear moduli, respectively. The calculated parameters are used by ABAQUS to relate the shear and loss moduli to Prony series functions employed to evaluate the time-dependant volumetric and shear behavior of the potting material [8].

3. Finite Element Modeling and Simulation

3.1. General Finite Element Method. The purpose of this modeling and simulation effort is to (1) identify the impact of potting on an electronics assembly during gun launch, (2) assess differences in stresses and displacements at temperature extremes, and (3) determine if a ringed support system is adequate thereby limiting some of the deleterious effects resulting from temperature changes in fully potted electronics.

The modeling and simulation were completed using the general purpose finite element package ABAQUS, version 6.10.1 [8]. The following summarizes the analysis:

(i) general Purpose Finite Element Software: Abaqus Explicit 6.10.1;

(ii) analysis: dynamic, nonlinear materials, nonlinear geometry;

(iii) parts: All parts are representative, not actual;

(iv) elements: 8-node brick elements, reduced integration, hourglass control. The fully potted model also used 10-node tetrahedral elements;

(v) materials: elastic and elastic/plastic and visco/elastic;

(vi) friction: frictionless, all contact surfaces;

(vii) damping: no applied damping currently in the model except for what's imparted by the viscoelastic constitutive model;

(viii) initial conditions: no initial displacement or velocity; initial temperature: 60°C and −40°C, the extremes of the operating range. (The storage temperature range is larger.)

3.2. Internal Constraints, Assumptions. The following items were tied: board to solder, solder to chips, can bottom to can top, and potting parts to one another. In the potted model, the potting was tied to the chips, the board, and the can. In the ringed model, the potting was tied to the boards and can. All other contacts were applied as frictionless contact.

3.3. Applied Load and Output. Measured acceleration data was applied to the bottom of the can as a three-dimensional acceleration, Figure 3. The acceleration sequence was recorded on a live-fire shot of a precision projectile near where a critical electronics package is located. The on-board recorder assembly was design to be a rough match of the electronics package mass and stiffness. Axial G-forces in the range of 15-kgs and transverse force in the range of 3-kgs are expected, applied with different frequency content [9]. Components are typically designed for the maximum G-force which occurs in the gun tube at around 0.0038 sec. Carlucci et al. observed, however, that many electronics components fail during the muzzle exit event, around 0.011 sec in Figure 3 [10]. Contour plots of stress and strain were recorded at 98 increments of the load from Figure 3. A Python script and Fortran program were used to determine the maximum stress and the time at which it occurred for each of the chips in the model.

3.4. Potted versus Ringed Geometries. Two geometries were compared. First, a fully potted assembly was evaluated,

Table 1: Input for viscoelastic prony parameter calibration, cold.

ωg^* real	ωg^* imaginary	ωk^* real	ωk^* imaginary	Frequency (Hz)
0.0303	0.00000	0.00000	0.00000	1.0
0.03271	−0.007392	0.00000	0.00000	1.5
0.02989	−0.01671	0.00000	0.00000	2.5
0.02855	−0.02411	0.00000	0.00000	3.9
0.02761	−0.03325	0.00000	0.00000	6.3
0.02535	−0.04129	0.00000	0.00000	10.0
0.0259	−0.05033	0.00000	0.00000	15.8
0.01834	−0.05893	0.00000	0.00000	25.1
0.02134	−0.07476	0.00000	0.00000	39.8
0.009863	−0.08714	0.00000	0.00000	63.0
0.01946	−0.1178	0.0000	0.00000	100

Table 2: Input for viscoelastic prony parameter calibration, ambient.

ωg^* real	ωg^* imaginary	ωk^* real	ωk^* imaginary	Frequency (Hz)
0.64605	0.00000	0.00000	0.00000	1.0
0.74276	−0.15751	0.00000	0.00000	1.5
0.86017	−0.35639	0.00000	0.00000	2.5
0.98753	−0.58518	0.00000	0.00000	3.9
1.12523	−0.84795	0.00000	0.00000	6.3
1.26766	−1.14182	0.00000	0.00000	10.0
1.41668	−1.47368	0.00000	0.00000	15.8
1.56600	−1.84187	0.00000	0.00000	25.1
1.72882	−2.30529	0.00000	0.00000	39.8
1.89617	−2.82774	0.00000	0.00000	63.0
2.06754	−3.41998	0.00000	0.00000	100.0

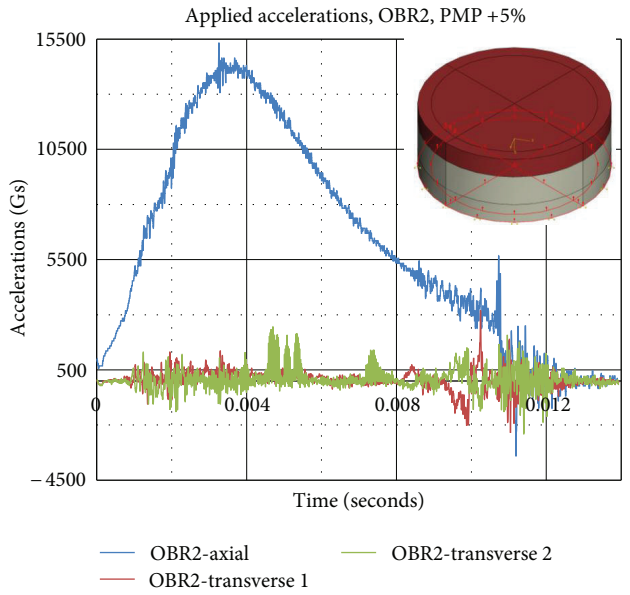


Figure 3: Example gun launch G-forces, 3-dimensional.

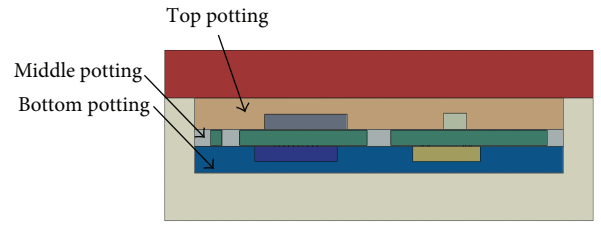


Figure 4: Geometry of potted model.

Figure 4. The model includes an aluminum supporting can, an aluminum lid, a circuit board, 8 chips with solder, and 3 tied-together sections of potting. The model has 0.127 mm (0.005 inch) thick solder loads under the chips. The can, chips, board, and solder were the same for both geometries. Second, the same potting material was modeled as rings that gripped the outside of the circuit board. In the second analysis, the chips and most of the board were free from contact with potting. Central grommets were employed to reduce the relative deflections across the chips. Figure 5 shows the geometry with ring and grommet supports. Figure 6 shows the solder geometry for the top and bottom of the board.

3.5. Material Assumptions. Figure 7 shows the material assumptions. Table 4 displays the material properties. The electronic chips on the bottom were modeled as ceramics.

Table 3: Input for viscoelastic prony parameter calibration, hot.

ωg^* real	ωg^* imaginary	ωk^* real	ωk^* imaginary	Frequency (Hz)
0.2061	0.00000	0.00000	0.00000	1.0
0.1274	−0.02513	0.00000	0.00000	1.5
0.1464	−0.04945	0.00000	0.00000	2.5
0.1723	−0.07912	0.00000	0.00000	3.9
0.2074	−0.1149	0.00000	0.00000	6.3
0.252	−0.1598	0.00000	0.00000	10.0
0.3111	−0.2163	0.00000	0.00000	15.8
0.3957	−0.2878	0.00000	0.00000	25.1
0.4926	−0.3817	0.00000	0.00000	39.8
0.6204	−0.4866	0.00000	0.00000	63.0
0.8108	−0.5726	0.00000	0.00000	100.0

Table 4: Material assumptions.

Part	Material	Young's modulus MPa	Poisson's ratio	Mass density Kg/m^3	Ref. temperature $^\circ$C	Material model
Solder	Solder-sn60-pb40	$3E+05$	0.4	8598	All	Linear elastic plastic
Chips	Ceramic_X7R	$1.05E+05$	0.3	5624	All	Linear elastic plastic
Can	Aluminum	$7E+-4$	0.3	2716	All	Linear elastic plastic
Potting	Alchemix	6131	0.49	1604	−51	Linear elastic/viscoelastic
Potting	Alchemix	120	0.49	1604	23	Linear elastic/viscoelastic
Potting	Alchemix	7.2	0.49	1604	71	Linear elastic/viscoelastic
Connectors	Plastic	$3.6E+04$	0.23	4235	All	Linear elastic plastic
Board	FR4	$2.5E+04$	0.15	1925	All	Orthotropic elasticity

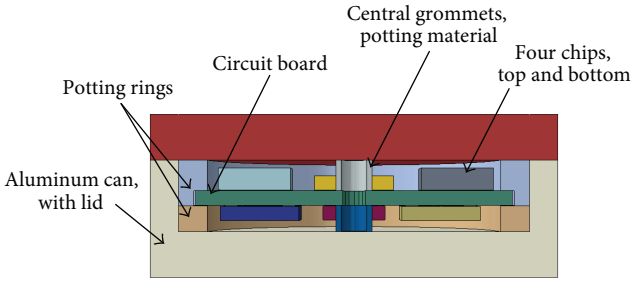


Figure 5: Geometry with potting rings supporting the circuit board.

As shown in Table 4, the Young's modulus for the potting varies by orders of magnitude over the temperature range. Analysis at the low and high ends of the temperature allows for assessing potting effects at different stiffness.

4. Finite Element Comparisons

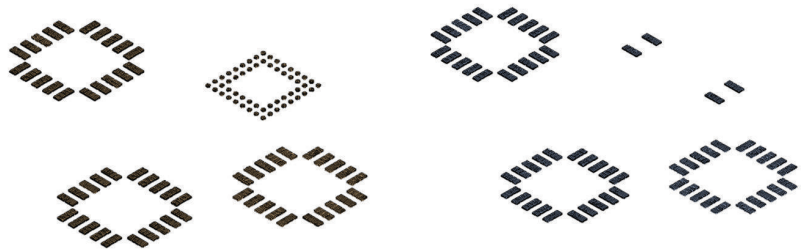
4.1. Modeling and Simulation, Cold Temperatures (−40°C). Figure 8 shows the stresses in the chips at time = 0.004 second at cold temperature. The highest stress occurs at setback, roughly coincident with the largest axial acceleration. The stresses in the unpotted design were about 30% higher in the chips compared to the potted design. Figure 9 shows the displacements at setback. The relative deflection of the center of the board in the ring model is evident. Figure 10 shows the stresses at muzzle exit, around 0.0113 second. At muzzle exit, the boards tend to flex in the direction opposite setback. Moreover, the stresses in the fully potted design are observed to be higher than in the ring-only design. For both models, stresses were within the estimated strength of the chips (76 MPa [11]). In both cases the solder yielded during gun launch.

Table 5 compares the maximum stresses and maximum relative displacement in the chips over the time span at cold for the ringed geometry. In Table 5, the second column is the maximum equivalent Von Mises stress and column 3 is the time at which it occurs. Some of the chips reached a maximum stress in the gun around set back (around 0.0038 sec) and others during muzzle exit (around 0.011 sec). The Army uses 76-MPa as the allowable stress threshold for electronic components which corresponds to about a 10% chance of failure according to [11]. The relative displacement in chips is also noted, column 6 in Table 5. The Army considers maximum relative displacement in the same chip less than 0.10 mm as surviving. At cold, all chips in the ringed model are predicted to survive based on the Army criteria. The calculations were repeated at ambient and hot conditions.

Table 6 shows summary results for the fully potted model at cold temperatures. The allowable stress was slightly exceeded by Bottom-Chip-3. All maximum values for stress occurred at muzzle exit. Relative displacements, column 6, were well below the ringed geometry model.

Table 5: Results, ringed model at cold, maximum stresses.

Chips	Svm MPa	Time Sec	S1 MPa	Time Sec	Delta disp mm	Time Sec
Top-Chip-1	46.1	0.0026	24.2	0.0048	0.069	0.0113
Top-Chip-2	61.7	0.0111	18.9	0.0116	0.078	0.0042
Top-Chip-3	61.7	0.0116	14.6	0.0112	0.069	0.004
Top-Chip-4	22.7	0.0116	20.3	0.0116	0.024	0.0125
Bottom-Chip-1	40.7	0.0032	24.9	0.0032	0.065	0.0113
Bottom-Chip-2	38.2	0.004	28.5	0.004	0.065	0.004
Bottom-Chip-3	12.2	0.0032	10.0	0.0038	0.041	0.0129
Bottom-Chip-4	47.5	0.0032	36.5	0.0032	0.061	0.0042



(a) (b)

Figure 6: Solder configurations—Top (a) and Bottom Chips (b).

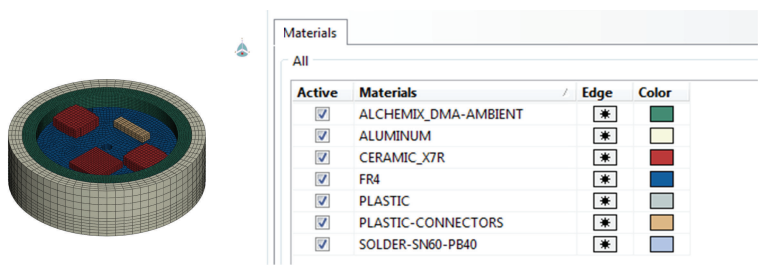
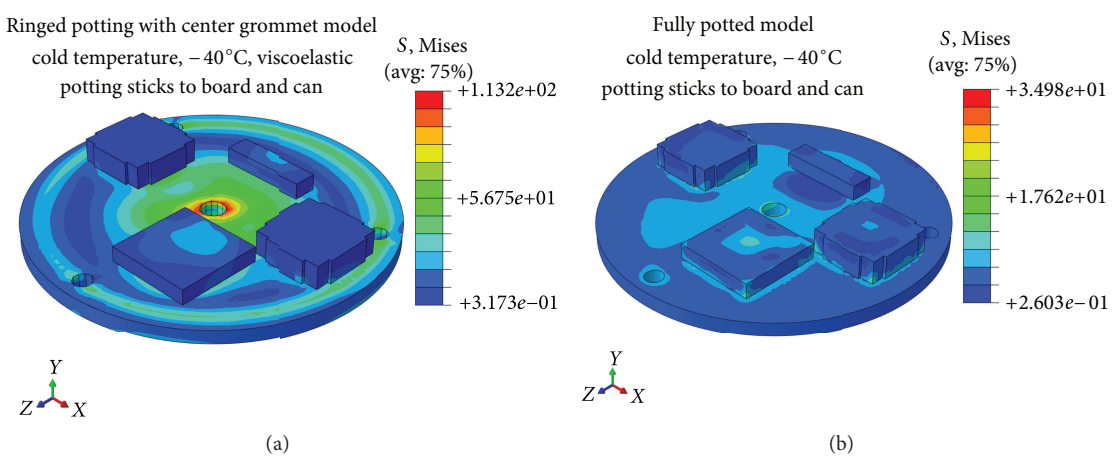


Figure 7: Material assumptions.



(a) (b)

Figure 8: Comparison of stresses in chips without potting (a) and with potting (b) at cold temperature at set back.

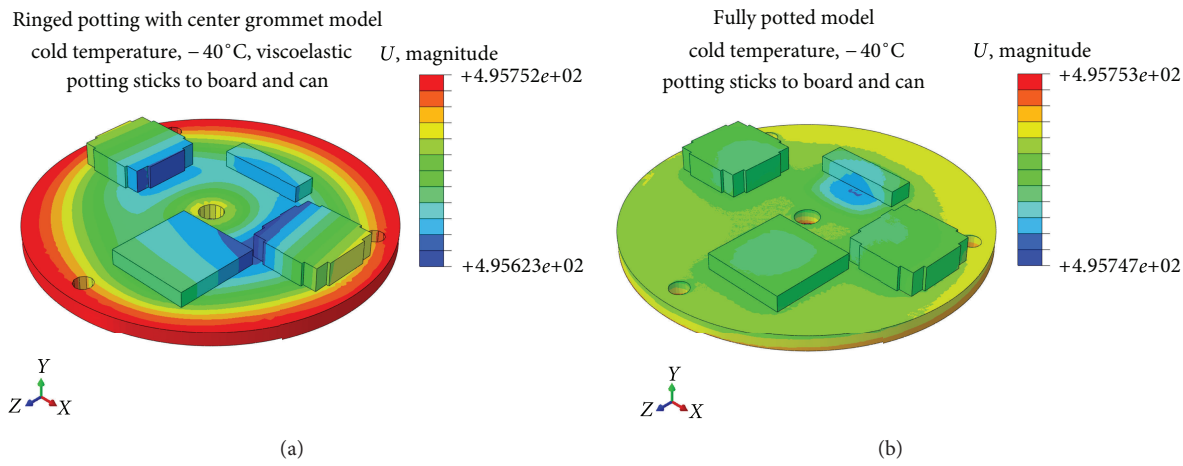


FIGURE 9: Comparison of displacement in chips without potting (a) and with potting (b) at cold temperature at setback.

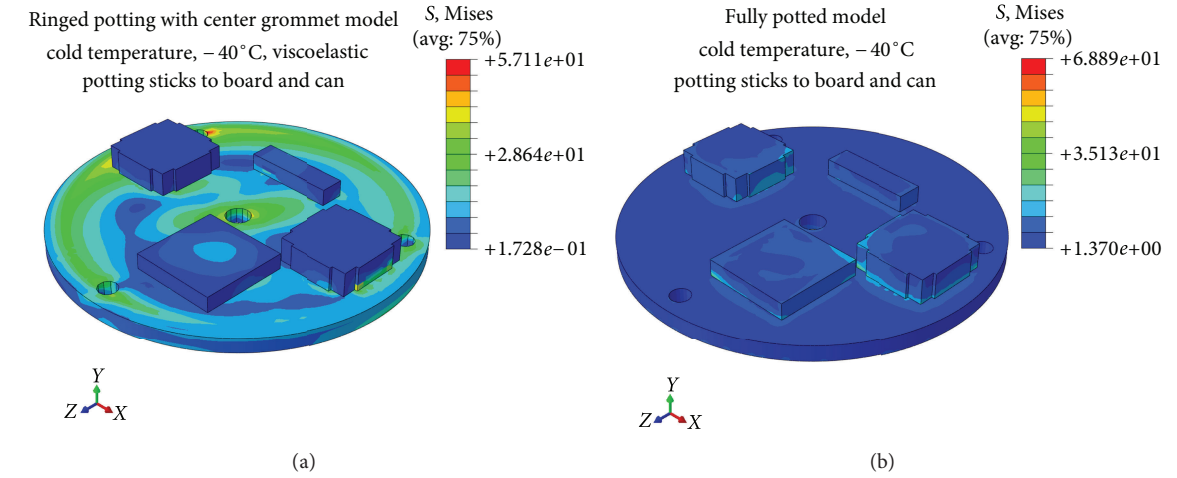


FIGURE 10: Comparison of stresses in chips without potting (a) and with potting (b) at cold temperature at muzzle exit.

The comparison between ringed potting and fully potting was repeated allowing the potting to be nonadhering in the fully potted model. In this case, Figure 11, the stresses in the fully potted model dropped below the ringed model when the potting does not adhere to chips. Stresses in nonadhering potting were lower than the sticky potting.

4.2. Modeling and Simulation, Hot Temperatures. Figure 12 compares stresses at hot conditions between the ringed and fully potted model at set back. For the ringed model, stress distributions were different and maxima were lower at hot temperatures. For the fully potted model, stresses were higher at high temperatures, and some chips exceeded allowable values.

Table 7 shows the stress in the rings-only model at high temperature. Comparing to the ringed analysis at cold in Table 5, stresses in the 1/2 of the top chips were higher than for the cold material data. Moreover, the chips on the bottom of the board are observed to have a slightly higher maximum stress under the high-temperature conditions. In the hot model, most of the chips reached a maximum at set back. In the cold model, the bottom chips also reached maximum stress at set back. In the hot model, the relative displacement of the chips and the stresses were within acceptable values.

Table 8 shows results for the fully potted model at high temperatures. The stresses at the bottom of the board are roughly twice as high than for the ringed model. As with the ringed model, the stresses on the bottom of the board were higher than for the fully potted cold model.

5. Discussion and Comparisons

5.1. Errors and Omissions. The geometry in the finite element analysis was much simpler than actual electronics. It should be emphasized that the simplified models were used for comparisons to assess the effects of potting.

Solder configurations were simplified since (1) the study compares stresses in the chips, and (2) the solder serves as a nonlinear spring. If stress and fatigue within the solder joints are required, detailed solder models such as presented

Table 6: Results, fully potted model at cold, sticky potting, maximum stresses.

Chips	Svm MPa	Time Sec	S1 MPa	Time Sec	Delta disp mm	Time Sec
Top-Chip-1	26.3	0.0117	17.8	0.0113	0.002	0.0038
Top-Chip-2	33.8	0.0117	21.0	0.0113	0.002	0.0118
Top-Chip-3	25.0	0.0113	17.2	0.0118	0.003	0.0113
Top-Chip-4	16.9	0.0113	9.6	0.0115	0.002	0.0115
Bottom-Chip-1	61.8	0.0113	39.6	0.0115	0.002	0.0118
Bottom-Chip-2	61.7	0.0113	33.9	0.0115	0.002	0.0113
Bottom-Chip-3	77.6	0.0113	48.3	0.0118	0.002	0.0038
Bottom-Chip-4	60.3	0.0113	39.4	0.0112	0.002	0.0136

Table 7: Results, ringed model at hot, maximum stresses.

Chips	Svm MPa	Time Sec	S1 MPa	Time Sec	Delta disp mm	Time Sec
Top-Chip-1	51.0	0.0036	27.4	0.0036	0.046	0.0123
Top-Chip-2	44.7	0.0028	14.7	0.0132	0.096	0.0034
Top-Chip-3	41.5	0.0112	12.4	0.012	0.088	0.0038
Top-Chip-4	24.5	0.0034	16.1	0.0032	0.026	0.0038
Bottom-Chip-1	43.1	0.004	25.9	0.0048	0.056	0.0034
Bottom-Chip-2	41.6	0.0038	30.1	0.0038	0.088	0.0038
Bottom-Chip-3	12.2	0.0021	9.0	0.0034	0.043	0.0108
Bottom-Chip-4	54.1	0.0034	40.4	0.0034	0.074	0.0034

Table 8: Results, fully potted model at hot, sticky potting, maximum stresses.

Part	Svm MPa	Time Sec	S1 MPa	Time Sec	Delta disp mm	Time Sec
Top-Chip-1	16.4	0.0142	8.4	0.0124	0.024	0.0116
Top-Chip-2	24.3	0.0121	15.9	0.0122	0.021	0.0119
Top-Chip-3	38.0	0.012	23.7	0.012	0.019	0.0117
Top-Chip-4	22.1	0.0034	12.1	0.0112	0.015	0.0127
Bottom-Chip-1	107.5	0.0119	41.5	0.0124	0.022	0.0119
Bottom-Chip-2	82.6	0.0116	40.9	0.0127	0.020	0.0117
Bottom-Chip-3	80.6	0.0119	55.4	0.0121	0.017	0.0127
Bottom-Chip-4	77.7	0.0128	34.5	0.0128	0.021	0.0116

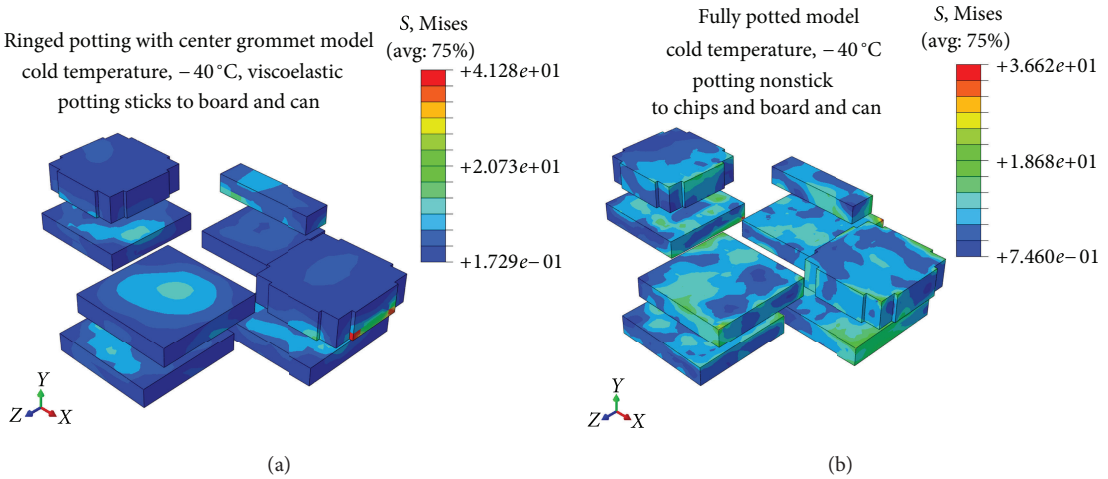


Figure 11: Comparison of stresses in chips with potting (a) and without potting (b) at cold temperature at set back, non-adhering potting.

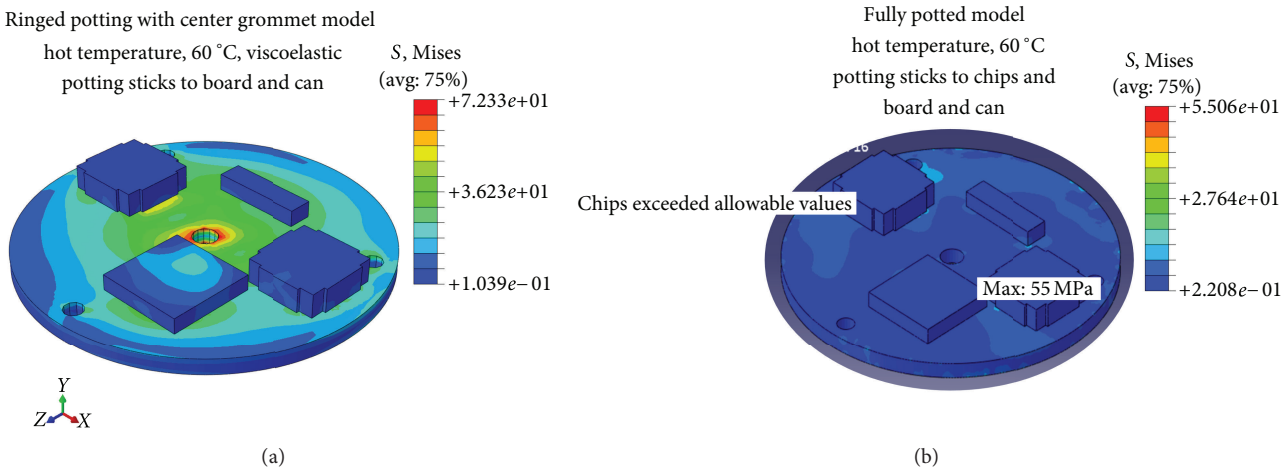


Figure 12: Comparison of stresses in chips with potting (a) and without potting (b) at hot temperature at set back, sticky potting.

by authors in [12] may be employed. Of course, high fidelity solder models would greatly increase the degrees of freedom of the finite element model. For these relative studies on chip behavior, detailed solder modeling was not required.

Like the solder, the boards and chips have been greatly simplified. The Army does model details of chips when failures occur. For this study, relative stresses and displacements were required for comparisons.

One drawback of this study is that the viscoelastic model employed is limited to a frequency range that falls below the vibratory frequencies the potted assembly is subjected to during gun launch (10–20 KHz). Further studies into the high-frequency material behavior are underway to determine the impact on the material behavior and structural stability of the electronic assembly. High-frequency viscoelastic properties should be incorporated into future models.

5.2. Estimating Failure in Chips and Electronic Components. It is recognized that the failure conditions for chips vary from chip to chip. Blattau et al. [11] described variations in the failure stress of capacitors with different materials for solder support. The reference also provides probability of failure as a function of calculated stress in chips. Failure is based on the stress required to cause cracking in capacitors, a well documented failure in capacitors [11, 13, 14]. The 76-MPa strength criterion is used by the Army as a rough guide for failure strength and should not be considered a hard failure condition. Modeling and simulation have predicted stresses as high as 101-MPa in chips that do not fail.

The relative deflection as another failure point is also a rough estimate. Flex failures have also been documented, by Prymak et al. [15]. The Army's use of 0.1 mm as a failure criterion on relative displacement within chips has worked well and is comparable to flexing magnitudes in the Prymak report.

5.3. Comparisons Computing Times. The current work was completed on a super computer at Picatinny Arsenal. The computer has 84 Total Cores and is a Linux-Based OS system with 84 Cores on 7 Nodes/12 Cores per Node/48 GB RAM per Node Intel Xeon 5650, 2.67 GHz CPU, 6 Cores per CPU.

Analysis with full potting, Figure 4, was completed using 12 parallel processors. The cold temperature case took approximately 57 hours with the following statistics:

(i) number of elements is 376143,

(ii) number of nodes is 765110;

(iii) total number of variables in the model is 2295330.

The hot case analysis ran with three times the processors and took longer due to the smaller time step required. Because of the complexity of the potting geometrically, some of the elements were small. The element size coupled with the density/stiffness ratio at hot required a small time step.

In contrast, the ringed potting model, Figure 5, was completed using 12 parallel processors. The cold temperature case took approximately 5.7 hours with the following degrees of freedom:

(i) number of elements is 89246;

(ii) number of nodes is 119596;

(iii) total number of variables in the model 358788.

The hot and ambient cases took similar time because the finite elements were of reasonably uniform size. All elements were 8-node brick elements. The enhanced hourglass controls limited convergence and numerical difficulties. If multiple load cases need to be run, a simpler ringed design is easier to evaluate.

6. Recommendations

6.1. Stresses and Displacements at Different Temperatures. This study was conducted under multiple thermal mechanical loading conditions to identify the structural impact of potted electronics for gun launch applications. The mechanical test data acquired suggests that the material undergoes very large changes in strength and stiffness in the temperature range

studied. Due to these changes, the stresses imparted by the potted vary in the temperature range from −40°C to 60°C. For reliability, small changes in a proven design are desirable. If potting is used, it is strongly suggested that a material should be selected with the glass transition temperature higher than the electronics operating range.

6.2. Thermal Effects. Effect of coefficient of thermal expansion mismatches between potting and electronic components was not addressed in this study. The expansion coefficient for potting in this study varies by a factor of two over the temperature range. The specific heat varies by about 50%. Chao et al. have shown that the potting would be expected to have significant thermal mismatch issues based on the coefficients of thermal expansion for the potting and the ceramic chips [16]. For thermal expansion issues, ringed potting should be considered over fully potted models.

The operating and storage range for munitions is −42°C to 63°C and −51°C to 71°C, respectively. It is important to note that while the potted electronics assembly may protect the electronic components from large vibratory and shock loads; the material chosen must retain stable mechanical properties through the operating and storage temperature regimes. Material testing reveals that the mechanical properties of the potting material employed for this analysis change significantly with temperature. Because of this and as supported by [3, 6, 7, 16–18] the potting material potentially imposes additional risks to the mechanical stability of the electronics assembly. The material evaluated in this study is not an ideal potting solution because of its thermomechanical issues.

6.3. Interface Effects. Studies on the impact of interaction properties between potting and the electronics housing, solder connections, and electronic chips showed that sticky potting (potting tied to all surfaces) results in higher stresses than contact-only potting (nonadhering). Sticky potting can also lead to stress risers between components and the board and possible breaking of leads/wires. For this reason, nonsticky potting should be considered if fully potted electronics are required.

6.4. Ringed Geometry as Opposed to Fully Potted Model. As a result of this study and due to the thermal effects described by Chao et al. [16], a ringed assembly or similar is recommended over a fully potted design. The ringed design with a center support resulted in stresses and deflections in the acceptable range over the full temperature range.

7. Conclusion

Summarizing, although the stresses and displacements occurring during gun launch are adequately supported by a material with the hot and cold stiffness of the potting material, this type of potting is not recommended for gun-fired electronics. This is primarily because the glass transition temperature falls within the operating range and the material's structural integrity degrades with increasing temperature. Further studies on the impact of high glass (>71°C) transition and low glass transition (< −51°C) materials are underway.

A comparison of a fully potted assembly to a rings-only-supported assembly indicated that full potting may not be required when adequate support is otherwise available. As discussed, ringed supports may add several other reliability benefits that relate to thermal, storage, and adhesion effects.

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