Research Article

Impact of Split Gate in a Novel SOI MOSFET (SPG SOI) for Reduction of Short-Channel Effects: Analytical Modeling and Simulation

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In this paper a comprehensive investigation of a novel device called split-gate silicon-on-insulator MOSFET (SPG SOI MOSFET) is proposed to reduce short-channel effects (SCEs). Studying the device has been done by analytical approach and simulation. In the proposed structure the gate is split into two parts. A voltage difference exists between the two parts. It is demonstrated that the surface potential in the channel region exhibits a step function. Some improvements are obtained on parameters such as SCEs, hot-carrier effect (HCE), and drain-induced barrier lowering (DIBL). The accuracy of the results obtained by use of the analytical model is verified by ATLAS device simulation software. The obtained results of the model are compared with those of the single-gate (SG) SOI MOSFET. The simulation results show that the SPG SOI MOSFET performance is superior.

1. Introduction

In recent years the silicon-on-insulator metal oxide semiconductor field effect transistors (SOI MOSFETs) have been regarded as good counterpart with respect to other semiconductor devices in VLSI/ULSI technology. With progress in semiconductor device technology, the device scales shrink to submicrometer regime. When channel length shrinks to submicrometer, undesirable effects which are named short-channel effects (SCEs) will be explored. These effects occur because controllability of the gate over-channel is reduced by shrinking the channel length.

Thin-film fully depleted SOI MOSFETs have superior electrical characteristics than the bulk MOS devices, such as reduced junction capacitances, excellent latchup immunity, increased channel mobility, and reduced short-channel effects (SCEs) [1]. However, when the channel length becomes smaller than 100 nm, SCEs will occur [2]. By using structures such as dual material gates, multiple gates, and fin field-effect transistors (FINFETs), short-channel effects decrease [3–5]. The scaling of SOI MOSFETs has been investigated, and several SOI structures have been studied in

terms of a natural length scale [6]. An analytical model for the threshold voltage of short-channel single-gate SOI MOSFETs has been derived with considering the two-dimensional (2D) effects in both SOI and buried-oxide layers [7]. The potential distribution has been investigated in multiple-gate SOI MOSFETs [8]. A threshold voltage model of a mesa-isolated SOI MOSFET based on an analytical solution of the three-dimensional (3D) Poisson's equation has been presented [9]. The separation of variables technique is used to analytically solve the 3D Poisson's equation with appropriate boundary conditions. The SCEs can be reduced using an inversion layer as an ultrashallow source/drain (S/D) in the sub-50 nm regime [10–16]. An analytical model of the surface potential and threshold voltage of a SOI MOSFET with electrically induced shallow S/D junctions has been presented to investigate the SCEs [17]. The effectiveness of the dual-material-gate (DMG) structure in fully depleted SOI MOSFETs has been investigated to suppress SCEs by developing a 2D analytical model of surface potential and threshold voltage [18]. Also references such as [19–21] have presented new devices to suppress the short-channel effect well.

In this paper the split-gate transistor is proposed to reduce SCEs. In this structure the gate is split into two parts with a small gap between them. Indeed the proposed structure is like the DMG-SOI [18] but by a new idea. In our structure, the voltage difference between the gates will control the channel well. In this study, a SPG SOI transistor with different gate biases is considered and also an analytical model is developed to investigate the transistor performance. The model is used to calculate the surface potential distribution in the lower SOI thin film of two the gates and to investigate the exclusive characteristics of the SPG structure in suppressing SCEs such as the hot-carrier effect, DIBL, and threshold voltage (V_{TH}) roll-off in SOI MOSFETs. Also this model provides an efficient tool for design and characterization of the novel SPG MOSFETs. The obtained results of analytical model are verified by ATLAS software [22]. Two-dimensional numerical simulations of the proposed structure are done with ATLAS simulator. In addition to Poissons, and drift/diffusion equations, SRH (Shockley-Read-Hall) and Auger models are considered for generation/recombination, and also IMPACT SELB for impact ionization. These simulation methods allow taking into account carrier velocity saturation, carrier-carrier scattering in the high doping concentration, and constant mobility.

2. Analytical Model

A cross-section view of a fully depleted SPG SOI MOSFET is illustrated in Figure 1 with two gates, G_1 and G_2 , of lengths L_1 and L_2 , respectively. There is a small gap of length Z between the gates. We assume that the impurity density in the channel region is uniform, and the effects of charge carriers and fixed oxide charges on the electrostatics of the channel can be neglected. With these assumptions the potential distribution in the silicon thin film before the onset of strong inversion can be written as

$$\frac{d^2\phi(x, y)}{dx^2} + \frac{d^2\phi(x, y)}{dy^2} = \frac{qN_A}{\epsilon_{Si}}, \quad \text{for } 0 \leq x \leq L, \quad (1)$$

$$0 \leq y \leq t_{Si},$$

where N_A is the silicon film doping concentration, ϵ_{Si} is the dielectric constant of silicon, t_{Si} is the film thickness, and L is the device channel length. If the channel length, silicon thickness, and oxide gate thickness become very small, then the current analytical approach is not true, and the quantum models must be regarded. Also silicon thickness must not be very much because the structure is fully depleted. Also higher doping in source/drain is not very critical because the channel under the gate is very important for the structures usually.

The potential profile in the vertical direction, that is, the y -dependence of $\phi(x, y)$ can be approximated by a simple parabolic function as proposed by Young for fully depleted SOI MOSFETs [23]:

$$\phi(x, y) = \phi_s(x) + c_1(x)y + c_2(x)y^2, \quad (2)$$

where $\phi_s(x)$ is the surface potential and the arbitrary coefficients $c_1(x)$ and $c_2(x)$ are functions of x only. Since the gap

FIGURE 1: Cross-sectional view of an n-channel fully depleted SPG SOI MOSFET.

length (Z) is extremely small, we assume that the potential distribution in the region of $L_1 \leq x \leq L_1 + Z$ and $0 \leq y \leq t_{Si}$ (under the gap) for each y is a linear function of x . At $y = 0$, this potential distribution in region of $L_1 \leq x \leq L_1 + Z$ reads

$$\phi_3(x, 0) = a_1x + b_1, \quad (3)$$

where the coefficients a_1 and b_1 are constant values. Since we just need the potential at $y = 0$, (3) is true. Because of the same gate metals, the work functions of the two gates are equal. Therefore, the flat-band voltages for the two gates are the same:

$$V_{FB} = \phi_M - \phi_S. \quad (4)$$

The semiconductor work function can be written as

$$\phi_S = \chi_{Si} + \frac{E_g}{2q} + \phi_F. \quad (5)$$

$\phi_F = V_T \ln(N_A/n_i)$ is the Fermi potential. E_g is the silicon band gap. χ_{Si} is the electron affinity. V_T is the thermal voltage. n_i is the intrinsic carrier concentration.

In the SPG SOI structure, the potential under the gates can be written as

$$\begin{aligned} \phi_1(x, y) &= \phi_{S1}(x) + c_{11}(x)y + c_{12}(x)y^2, \quad \text{for } 0 \leq y \leq t_{Si}, \\ &\quad 0 \leq x \leq L_1, \\ \phi_2(x, y) &= \phi_{S2}(x) + c_{21}(x)y + c_{22}(x)y^2, \\ &\quad \text{for } L_1 + Z \leq x \leq L_1 + L_2 + Z, \\ &\quad 0 \leq y \leq t_{Si}. \end{aligned} \quad (6)$$

Poisson's equation is solved separately under the two gates using the following boundary conditions.

(1) The electric flux at the gate/front oxide interface is continuous for both gates:

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\phi_{S1}(x) - V'_{GS1}}{t_f}, \quad \text{for } G_1, \quad (7)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{\phi_{S2}(x) - V'_{GS2}}{t_f}, \quad \text{for } G_2, \quad (8)$$

where ϵ_{ox} is the dielectric constant of the oxide, t_f is the gate oxide thickness, $V'_{GS1} = V_{GS1} - V_{FB,f}$, and $V'_{GS2} = V_{GS2} - V_{FB,f}$.

Note that V_{GS1} is the gate (G_1)-source bias voltage, V_{GS2} is the gate (G_2)-source bias voltage, and $V_{FB,f}$ is the flat band voltage of G_1 and G_2 .

(2) The electric flux at the interface of the buried oxide and back-channel silicon is continuous for both gates:

$$\left. \frac{d\phi_1(x, y)}{dy} \right|_{y=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{V'_{SUB} - \phi_B(x)}{t_b}, \quad \text{for } L_1, \quad (9)$$

$$\left. \frac{d\phi_2(x, y)}{dy} \right|_{y=t_{Si}} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{V'_{SUB} - \phi_B(x)}{t_b}, \quad \text{for } L_2, \quad (10)$$

where t_b is the buried-oxide thickness and $\phi_B(x)$ is the potential distribution along the back-side oxide-silicon interface. $V'_{SUB} = V_{SUB} - V_{FB,b}$. V_{SUB} is the substrate bias and $V_{FB,b}$ is the back-channel flat-band voltage. V_{SUB} is set to 0 V.

(3) The surface potential at the interface of the two gates and the gap is continuous:

$$\phi_1(L_1, 0) = \phi_3(L_1, 0), \quad \phi_2(L_1 + Z, 0) = \phi_3(L_1 + Z, 0). \quad (11)$$

(4) The electric flux at the interface of the two gates and the gap is continuous:

$$\left. \frac{d\phi_1(x, 0)}{dx} \right|_{x=L_1} = \left. \frac{d\phi_3(x, 0)}{dx} \right|_{x=L_1}, \quad (12)$$

$$\left. \frac{d\phi_2(x, 0)}{dx} \right|_{x=L_1+Z} = \left. \frac{d\phi_3(x, 0)}{dx} \right|_{x=L_1+Z}.$$

(5) The potential at the source end is

$$\phi_1(0, 0) = \phi_{S1}(0) = V_{bi}. \quad (13)$$

(6) The potential at the drain end is

$$\phi_2(L_1 + L_2 + Z, 0) = \phi_{S2}(L_1 + L_2 + Z) = V_{bi} + V_{DS}. \quad (14)$$

$V_{bi} = (E_g/2) + V_T \ln(N_A/n_i)$ is the built-in potential across the body-source junction.

The constants $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$, and $c_{22}(x)$ in (6) can be obtained from the boundary conditions in (7)–(10). With substituting these values in (6) and then in (1), we obtain

$$\frac{d^2\phi_{S2}(x)}{dx^2} - \alpha\phi_{S2}(x) = \beta_2, \quad \frac{d^2\phi_{S1}(x)}{dx^2} - \alpha\phi_{S1}(x) = \beta_1, \quad (15)$$

where

$$\begin{aligned} \alpha &= 2 \frac{a_{13}}{a_{11}}, \quad \beta_1 = q \frac{N_A}{\epsilon_{Si}} - 2 \frac{a_{12}}{a_{11}}, \\ \beta_2 &= q \frac{N_A}{\epsilon_{Si}} - 2 \frac{a_{21}}{a_{11}}, \quad a_{11} = 2t_{Si} + \frac{\epsilon_{ox}}{\epsilon_{Si}t_b} t_{Si}^2, \\ a_{12} &= \frac{\epsilon_{ox}}{\epsilon_{Si}t_b} V'_{SUB} + \frac{\epsilon_{ox}}{\epsilon_{Si}t_f} \left(1 + \frac{\epsilon_{ox}t_{Si}}{\epsilon_{Si}t_b} \right) V'_{GS1}, \\ a_{13} &= \frac{\epsilon_{ox}}{\epsilon_{Si}t_b} + \frac{\epsilon_{ox}}{\epsilon_{Si}t_f} \left(1 + \frac{\epsilon_{ox}t_{Si}}{\epsilon_{Si}t_b} \right), \\ a_{21} &= \frac{\epsilon_{ox}}{\epsilon_{Si}t_b} V'_{SUB} + \frac{\epsilon_{ox}}{\epsilon_{Si}t_f} \left(1 + \frac{\epsilon_{ox}t_{Si}}{\epsilon_{Si}t_b} \right) V'_{GS2}. \end{aligned} \quad (16)$$

$\phi_{S1}(x)$ and $\phi_{S2}(x)$ are obtained by solving the differential equations in (15). Finally, the surface potential distribution is obtained as

$$\phi_{S1}(x) = A \exp(\lambda x) + B \exp(-\lambda x) - \frac{\beta_1}{\alpha}, \quad (17)$$

$$\begin{aligned} \phi_{S2}(x) &= C \exp\{\lambda[x - (L_1 + Z)]\} \\ &+ D \exp\{-\lambda[x - (L_1 + Z)]\} - \frac{\beta_2}{\alpha}, \end{aligned} \quad (18)$$

$$\phi_{S3}(x) = \phi_3(x, 0) = a_1 x + b_1, \quad (19)$$

where $\lambda = \sqrt{\alpha}$ and $\lambda_1 = -\lambda_2 = \lambda$.

By use of the boundary conditions in (11)–(14) and (17)–(19), we reach a system of six equations and unknowns.

The constant coefficients A , B , C , D , a_1 , and b_1 are calculated by solving this system of six equations and unknowns. The surface potential along the channel can be calculated with the help of these variables.

The electric field along the channel determines the electron transport velocity. The electric field components in the x -direction, under the G_1 , G_2 , and the gap, are given as

$$\begin{aligned} E_1(x) &= \left. \frac{\partial\phi_{S1}(x)}{\partial x} \right|_{y=0} \\ &= A\lambda_1 \exp(\lambda_1 x) - B\lambda_1 \exp(-\lambda_1 x), \quad 0 \leq x \leq L_1, \\ E_2(x) &= \left. \frac{\partial\phi_{S2}(x)}{\partial x} \right|_{y=0} \\ &= C\lambda_2 \exp(\lambda_2(x - (L_1 + Z))) \\ &\quad - D\lambda_2 \exp(-\lambda_2(x - (L_1 + Z))) \\ &\quad L_1 + Z \leq x \leq L_1 + L_2 + Z, \\ E_3(x) &= \left. \frac{\partial\phi_{S3}(x)}{\partial x} \right|_{y=0} = a_1, \quad L_1 \leq x \leq L_1 + Z. \end{aligned} \quad (20)$$

TABLE 1: Parameters for simulation of two transistors (SPG and SG transistors).

Parameter	Value
Gate length, L_1	100 nm
Gate length, L_2	100 nm
Front-gate oxide thickness, t_f	5 nm
Back-gate oxide thickness, t_b	5 nm
Silicon film thickness, t_{si}	12 nm
Gap length, Z	10 nm
Body doping, N_A	$6 \times 10^{16} \text{ cm}^{-3}$
Source/drain doping, N_D	$1 \times 10^{20} \text{ cm}^{-3}$
Gate metal work function, WF	4.5 eV
Voltage difference	0.75 V
Gate-(G_1 -) to source voltage, V_{GS1}	0.15 V
Gate-(G_2 -) to source voltage, V_{GS2}	0.9 V
Substrate voltage, V_{SUB}	0 V

3. Simulation Results and Comparison with Analytical Results

It is important that each analytical model applied in the devices must be verified by simulation software. Therefore in this paper the analytical model and simulation results have been brought and compared.

In all simulations, Z (gap length) is assumed to be $0.01 \mu\text{m}$ and the channel length is $L = L_1 + L_2 + Z$.

To verify our analytical model, the ATLAS device simulation software has been used to simulate the surface potential distribution within the silicon thin film. A fully depleted (FD) n-channel SPG SOI structure is implemented in ATLAS having uniformly doped source/drain and body regions.

In this study the voltage difference between the two gates is assumed to be 0.75 V, that is, $V_{GS2} - V_{GS1} = 0.75 \text{ V}$. This voltage difference can be obtained by a normal diode. In Table 1 parameters needing simulation of two transistors (SPG and SG transistors) have been listed.

In Figure 2, the surface potential profile has been plotted along the horizontal distance x in the channel for a channel length $L = 0.21 \mu\text{m}$ ($L_1 = 0.1$, $L_2 = 0.1$, and $Z = 0.01 \mu\text{m}$) at different biases. It can be seen from this figure that, in the SPG structure, there is no significant change in the potential under the gate G_1 as the drain bias is increased. Therefore the channel region under G_1 is "screened" from the changes in the drain potential, that is, the drain voltage is not absorbed under G_1 . The DIBL effect can be demonstrated by plotting the surface potential minimum as a function of the position along the channel for different drain bias conditions. It is evident from the figure that the shift in the point of the potential minimum is almost zero. This is a clear proof that the DIBL effect is considerably reduced for the SPG SOI MOSFET.

As shown in Figure 2, the ATLAS simulation results verify the accuracy of our proposed analytical model.

In Figure 3, the electric field distributions along the channel near the drain are shown for SPG and SG SOI MOSFETs with a channel length $L = 0.21 \mu\text{m}$ ($L_1 = 0.1$,

FIGURE 2: Surface channel potential profiles along the channel at channel length $L = 0.21 \mu\text{m}$.

FIGURE 3: Longitudinal electric field along the channel at channel length $L = 0.21 \mu\text{m}$.

$L_2 = 0.1$, and $Z = 0.01 \mu\text{m}$). As shown in this figure, the peak electric field at the drain end for the SPG SOI MOSFET is less than that for the SG SOI MOSFET. It is evident from this figure that the presence of a voltage difference between G_1 and G_2 reduces the peak electric field considerably. Therefore hot-carrier effect in SPG SOI MOSFET is less than that for the SG SOI MOSFET. The results of the analytical model are in close proximity with the ATLAS simulation results.

Figure 4 shows the surface potential profiles along the channel position for different gate length ratios of L_1 to L_2 (L_1/L_2). The sum of the channel length ($L_1 + L_2 + Z$) is constant. As shown in the figure, by reducing the length

FIGURE 4: Variation in surface potential with position in channel for different combinations of gate lengths L_1 and L_2 . The sum ($L_1 + L_2$) is constant.

FIGURE 5: Variation in the minimum potential with constant $L_1 = 50$ nm.

G_1 , the position of the potential minimum shifts toward the source. This causes the peak electric field in the channel to shift toward the source end and thus results in a more uniform electric field profile in the channel. This redistributes the surface potential, which results in a more uniform potential along the channel. Note that L_1 cannot be reduced to a very small value, since in the case of $L_1 \approx 0$, we have a SG transistor with a gate bias that is higher than the applied gate bias V_{GS1} . This higher gate bias reduces V_{TH} to a very small value and therefore increases the off current.

In Figure 5 the variations in potential minimum as a function of the channel length L with constant $L_1 = 50$ nm

FIGURE 6: Threshold voltage versus channel length.

for fully depleted SPG and SG SOI MOSFETs with silicon film thicknesses $t_{Si} = 12$ and 20 nm are shown. In the case of the SPG SOI MOSFET, the dependence of the potential minimum on the silicon thin-film thickness reduces with decreasing t_{Si} . This is due to the existence of a voltage difference between the two gates in SPG structure. The validity of model for the surface potential minimum under the gate for different combinations of L_1 and L_2 is verified by ATLAS simulation results.

In Figure 6 the threshold voltage V_{TH} has been shown as a function of the channel length with constant $L_1 = 25$ nm. V_{TH} was obtained for two structures SPG SOI MOSFET and SG SOI MOSFET with help of ATLAS simulator. The threshold voltage is extracted by calculating the maximum slope of the I_D/V_G curve, finding the intercept with the axis, and then subtracting half of the applied drain bias [23].

As shown in this figure, the variations in threshold voltage V_{TH} for SPG SOI MOSFET are less than, those of the SG SOI MOSFET. Therefore DIBL is reduced in SPG SOI. Also we have a desirable rollup in the threshold voltage with reducing channel length for SPG SOI MOSFET. Note that when the threshold voltage with shrinking channel length increases, off-current variations decreases, and this is a good benefit. But in the SG SOI MOSFET the threshold voltage decreases, with shrinking channel length. This results in increasing the off-current variations in the SG SOI MOSFET structure. Therefore the performance of SPG SOI MOSFET is superior to that in SG SOI MOSFET.

4. Conclusion

The impact of the split gate in fully depleted SOI MOSFETs has been examined to suppress SCEs by developing a 2-D analytical model for surface potential and by comparing the results with ATLAS device simulation software. In the proposed transistor (SPG transistor) a voltage difference is introduced between the two gates. In SPG structure, the shift in the surface channel potential minimum position is

negligible with increasing the drain bias. The electric field in the channel at the drain end is reduced. Therefore the hot-carrier effect reduces. The DIBL effect in our transistor is reduced because the voltage difference between the two gates is applied. In addition, the variation in the channel potential minimum with decreasing film thickness in our transistor is less than that in the SG SOI MOSFET. Also we obtained a desirable rollup in the threshold voltage with decreasing channel length for SPG SOI MOSFET. All obtained results of analytical model have been verified by ATLAS simulation software. These results show that the analytical model in SPG transistor is completely proper and also the SPG transistor performance is superior to that SG transistor.

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