Hindawi Publishing Corporation
Journal of Engineering
Volume 2013, Article ID 595296, 5 pages
http://dx.doi.org/10.1155/2013/595296

Research Article

ULPD and CPTL Pull-Up Stages for Differential Cascode Voltage Switch Logic

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Received 5 December 2012; Revised 5 February 2013; Accepted 24 February 2013

Academic Editor: Soliman A. Mahmoud

Two new structures for Differential Cascode Voltage Switch Logic (DCVSL) pull-up stage are proposed. In conventional DCVSL structure, low-to-high propagation delay is larger than high-to-low propagation delay this could be brought down by using DCVSL-R. Promoting resistors in DCVSL-R structure increase the parasitic effects and unavoidable delay and it also occupies more area on the chip (Turker et al., 2011). In order to minimize these problems, a new Ultra-Low-Power Diode (ULPD) structures in place of resistors have been suggested. This provides the minimum parasitic effects and reduces area on the chip. Second proposed circuit uses Complementary Pass Transistor Logic (CPTL) structure, which provides complementary outputs. This contributes an alternate circuit for conventional DCVSL structure. The performances of the proposed circuits are examined using Cadence and the model parameters of a 180 nm CMOS process. The simulation results of these two circuits are compared and presented. These circuits are found to be suitable for VLSI implementation.

1. Introduction

Differential logic was originally proposed as a logic style to eliminate static current and at the same time to provide a rail to rail swing on the output node. The cross coupling of pull-ups helps to speed-up transition. These circuits combine the concepts of differential circuits and positive feedback to provide high speed performance without the penalty of static power consumption. The key benefits of DCVSL are its low input capacitance, differential nature, and low power consumption. Heller et al. [1] proposed DCVSL that became popular due to its high speed performance over conventional static CMOS and the elimination of static current due to its cross coupled pull-up device connection. More recently, several new circuit styles based on the differential circuit concept have been proposed [2–5].

DCVSL circuit can outperform complex functions with a single differential tree network, minimizing the number of stages required and shorten the propagation delay when compared with conventional CMOS static gate designs. Enhanced Differential Cascode Voltage Switch Logic (EDCVSL) simplifies the logic tree of DCVSL and dramatically reduces the number of interconnections by eliminating the complementary inputs, while maintaining the features of DCVSL [6].

To increase the performance and reduce the power consumption, many clocked versions of the DCVSL gates have been introduced. The implementation of CMOS random logic with DCVSL has many advantages over the traditional static CMOS logic approach. First of all, DCVSL has the speed advantage of domino circuit. The reduction of the parasitic capacitances at the output nodes provides a faster response where in static power consumption is eliminated. Secondly, this logic style allows both inverting and noninverting logic gate implementation, while standard domino logic cannot implement inverting logic gates [1]. Thirdly, DCVSL saves area by sharing the common transistors in the logic network for both the outputs, when a complex logic gate is designed. Several techniques have been proposed to minimize DCVSL trees such as an algebraic technique [7], an approach utilizing the Karnaugh maps and a modified method by adopting Quine-McCluskey method [8].

In the DCVSL circuit shown in Figure 1, the drain node of NMOS transistor (gate of PMOS) drops slowly. Due to this, the low-to-high switching propagation delay (T_{PLH}) (the delay from the input falling from logic high to low to the

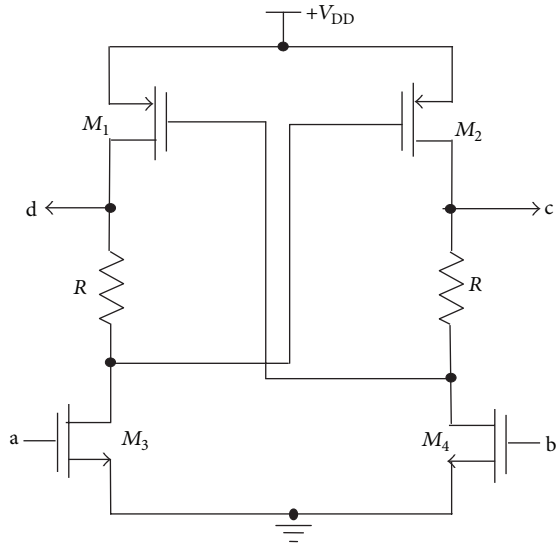

Figure 1: Conventional DCVSL-R structure.

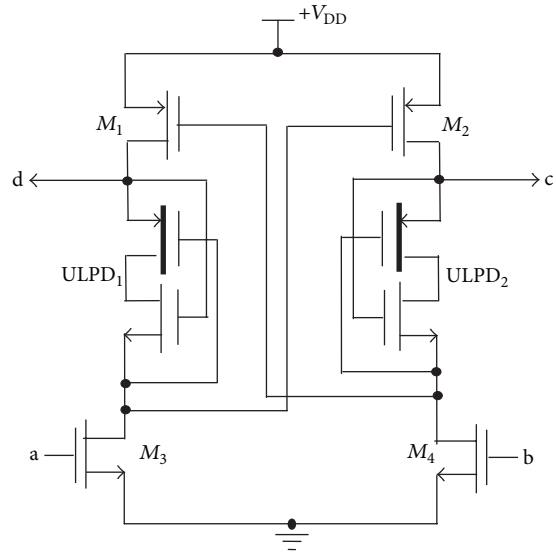

Figure 2: Proposed ULPD-DCVSL structure.

output rising from logic low to high) is higher than the high-to-low switching propagation delay (T_{PHL}). Due to this, asymmetric nature outputs are reported at the output side and also delay is displayed into the picture. To drop quickly across drain of NMOS, that is, to increase gate driving capability (i.e., to reduce the $T_{PLH} > T_{PHL}$), different techniques are adopted [9]. These increase the number of transistors. To reduce this factor in DCVSL-R [10], a DCVSL circuit was proposed with resistive enhancement. In DCVSL-R circuit, resistors R increase the gate driving capability that amounts to adding extra load to the drain of NMOS transistor. Combining drain node of NMOS and gate of PMOS, voltage drops quickly and asymmetric outputs are resolved. Due to the presence of resistors in DCVSL-R circuit, leakage currents are also to be taken into consideration. On observation of the above circuit, we may conclude that the placing of resistors has specific advantages as well as disadvantages. Resistors occupy more area on the chip and increase the parasitic effects. To eliminate this problem a new Ultra-Low-Power Diode- (ULPD-) based DCVSL circuit is brought into light [11].

In this paper, two DCVSL circuits using ULPD and CPTL structures are proposed. The proposed DCVSL circuit based on ULPD structure occupies less area on the chip and avoids low-high-transition propagation delay (T_{PLH}) and is inherently larger than the high-to-low transition propagation delay (T_{PHL}), thus achieving faster operation.

The organization of the remaining sections is as follows. Section 2 proposed DCVSL structures implementation. Section 3 explained simulation results and finally Section 4 ended up with conclusion.

2. Proposed DCVSL Circuit Implementation and Description

2.1. DCVSL Implementation Using ULPD. A new Ultra-Low-Power Diode- (ULPD-) based DCVSL circuit is shown in Figure 2. ULPD is a combination of PMOS and NMOS transistors where in PMOS transistor gate is connected to the NMOS source and NMOS gate is connected to the PMOS source by using depletion mode type MOSFETS [12]. By replacing a resistor with a ULPD [10], we can eliminate the condition $T_{PLH} > T_{PHL}$ and parasitic effects. ULPD offers a strongly reduced leakage current when compared to the standard diode connected MOSFET while maintaining similar forward current drive capability. When ULPD is reverse biased, both transistors operate with negative V_{gs} voltages. This leads to minimum leakage current compared to the standard diodes. Depending on the threshold voltages the ULPD can also be used in moderate or strong inversion regions. In this circuit, ULPD acts as a resistor. To operate the ULPD as a resistor, the transistors operate in linear region.

If we consider the switching conditions of the ULPD, while applying the complementary inputs to the pull-down network, one of the pull-down networks is put in ON condition. Thus pull-down network establishes a path to ground. When logic "1" is applied to the M_3 transistor, then it turns ON and starts conducting current, and the drain of the M_3 transistor quickly drops because of the additional load to PMOS gate. The output voltage of M_3 transistor quickly reaches the M_2 and then M_2 transistor reaches ON condition and output "c" is connected to the V_{DD}. As the other input of the pull-down network of M_4 transistor is logic "0" that means it does not establish a path to ground then M_1 transistor is set to OFF condition.

By adding the ULPD as a load to the drain of the NMOS transistors and increase the voltage drop at the gates of PMOS to turn on the PMOS transistors operate faster and minimize the waiting time. So $T_{PLH} = T_{PHL}$ and it results in symmetrical output waveforms. More importantly, due to the reduced T_{PLH}, the total delay of the DCVSL circuit comes down.

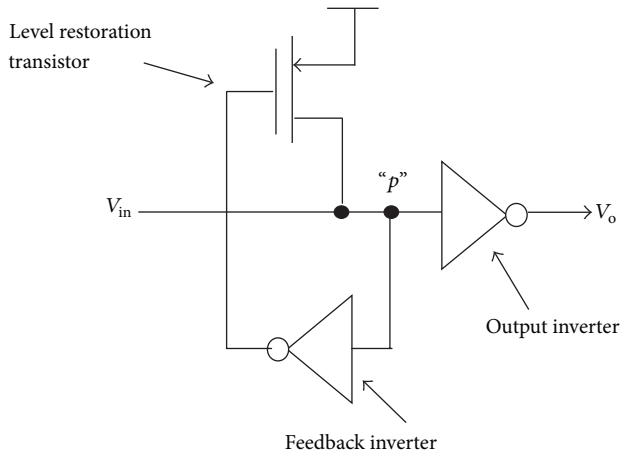

Figure 3: CPTL inverter.

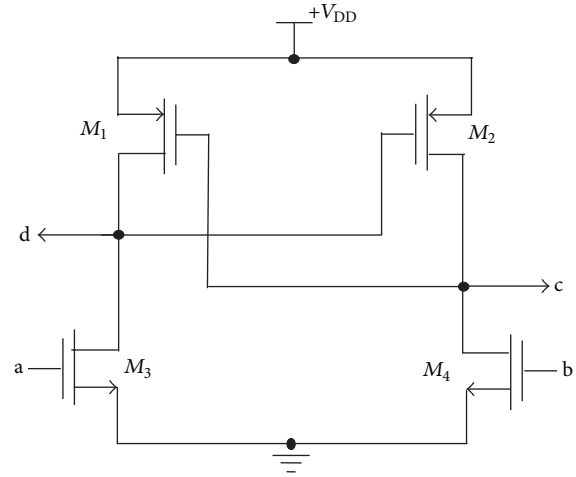

Figure 4: Conventional DCVSL structure.

2.2. DCVSL Implementation Using CPTL Structure. Figure 3 depicts the schematic diagram of CPTL inverter circuit. The CPTL uses series of transistors to select between possible inverted output values of the logic, the output of which drives an inverter to generate the non-inverted output signal. Inverted and non-inverted inputs are needed to drive the gates of the pass-transistors. The main advantages are full swing, elimination of static power in the inverter through level restorer and pass transistor. Since restorer is made active while the input V_i is high, the level restoration transistor improves capacitance and takes away pull down current at point "p" strife between level restoration transistor and input transistor (slower switching). Hence level restoration transistor is also to be sized to its minimum level. Feedback inverter and level restoration transistor are also to be sized such that the voltage at node "p" drops below the threshold of the inverter, which carries function in the sizes of output inverter [13].

DCVSL is a static logic family like pseudo, NMOS logic, which does not have a complementary pull-up network, but it has very different structure. It uses a latch structure for the pull-up. Both eliminates the static power consumption and provide true and complementary outputs. The structure of general DCVSL is shown in Figure 4. There are two pull-down networks which are the replica of each other for each true/complementary output. Pull-down network has a single p-type pull-up, but the pull-ups are cross coupled. In the proposed circuit, new structure for conventional DCVSL pull-up stage using Complementary Pass Transistor Logic (CPTL) as shown in Figure 5 is designed. The CPTL structure is a combination of two cross coupled inverters and one PMOS transistor. Here, depending upon the output pull-down network, one of the inverters is operating, based on the inverter output the PMOS transistor is in ON/OFF condition.

It is therefore assumed that the input variable "a" and its complement "b" exist and complementary outputs "c" and "d" are generated. When the input is logic "1" is applied to pull-down network, one of the pull-down networks will create a path to ground. The remaining gate input changes causing the output nodes to switch to logic "0".

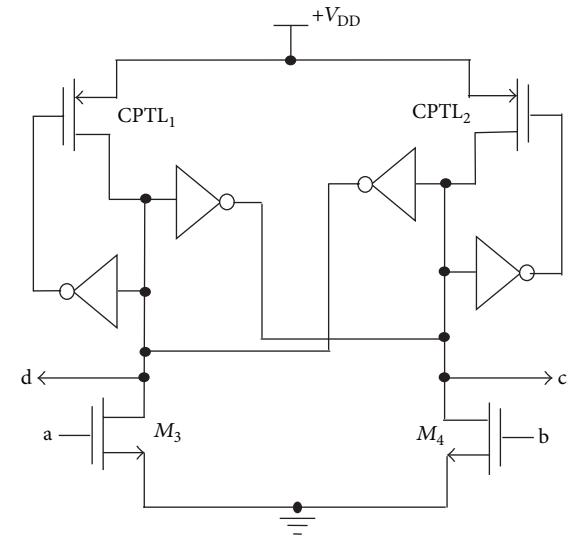

Figure 5: Proposed DCVSL structure.

When the complementary inputs are applied to the pull-down network, one of the pull-down network forms a path to ground. When logic "1" is applied to the M_3 transistor, it turns ON forming a path to ground. The output of M_3 transistor is connected to the input of $CPTL_1$ inverter, then the level restoration transistor (M_1) remains in OFF condition due to high feedback inverter output. Hence restorer remains active when the input is high. Since M_1 transistor is in OFF condition; that is, the input to the output inverter is logic "0," output is logic "1." Finally the output of $CPTL_1$ inverter is connected to the output "c". When logic "0" is applied to the pull-down network M_4, the operation is vice versa.

3. Simulation Results

The proposed DCVSL circuits Ultra-Low-Power Diode Differential Cascode Voltage Switch Logic (ULPD-DCVSL) and Complementary Pass Transistor Logic Differential Cascode

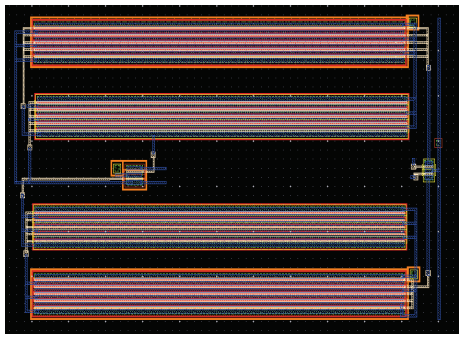

Figure 6: Layout of the proposed ULPD-DCVSL structure.

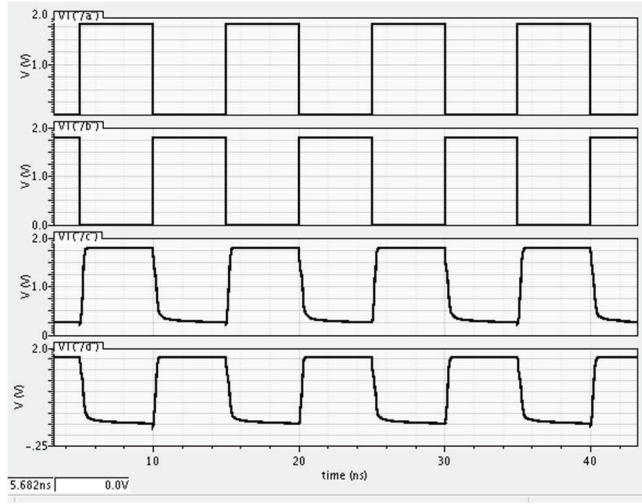

Figure 7: Simulated input and output waveforms of proposed DCVSL circuit using ULPD structure.

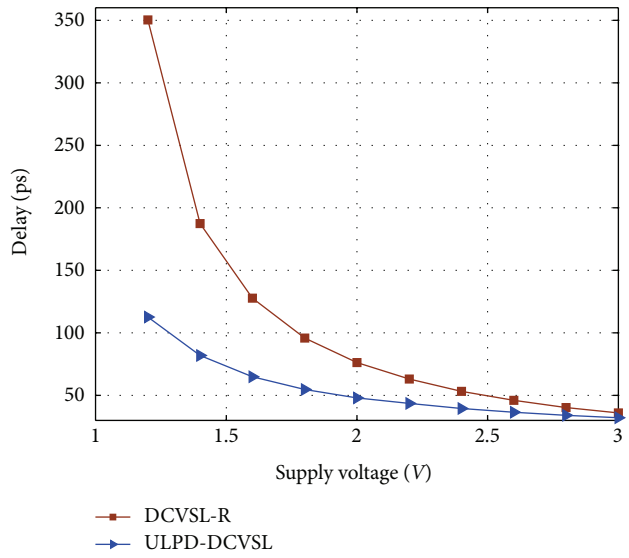

Figure 8: Delay versus supply voltage of ULPD-DCVSL and DCVSL-R structure.

Voltage Switch Logic (CPTL-DCVSL) are simulated using the Cadence and the model parameters of a 180 nm CMOS technology. The simulations were carried out with supply voltage V_{DD} = +1.8 V. In order to increase the switching speed, and thus to reduce the delay times, the W/L ratios of all transistors in the circuit are to be increased. Transistor sizes can also be of minimum sizes to achieve minimum delay. However, increase in the transistor W/L ratios also increases the gate, source and drain areas and subsequently increases the parasitic capacitances of loading the logic gates [2]. Hence, the resizing of transistors is an iterative process to improve the performance of the DCVSL circuit.

A comparison with existing or already reported designs is included, which shows the advantage of the proposed designs to have good delay performance. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. Transistor sizes can also be set to minimum sizes and to achieve minimum delay. The small silicon area of the proposed ULPD-based DCVSL circuit makes it potentially useful for building compact VLSI circuits on a smaller area of a chip.

The ULPD-DCVSL layout is presented with optimized sizing and spacing in compliance to the design rules of gpdk-180 nm CMOS process. The area occupied by the ULPD-DCVSL layout is 57.12 μm × 33.41 μm. The ULPD-DCVSL layout is shown in Figure 6.

The simulated input and output waveforms of the ULPD-DCVSL are shown in Figure 7. It may also to be noticed that the proposed ULPD-DCVSL shows the best delay performance and the results are plotted as shown in Figure 8. The proposed ones have good delay performance in its pull-up stage using ULPD DCVSL structure.

The simulated input and output waveforms of the DCVSL circuit using CPTL structure are shown in Figure 9. While optimizing the transistor sizes of DCVSL structures, it is possible to reduce the delay of all DCSVL structures, without significantly increasing the power consumption. The proposed CPTL-DCVSL structure has better delay performance compared with the DCVSL structure. The proposed DCVSL structures are potentially useful for building compact VLSI circuits.

It can also be seen that the proposed CPTL-DCVSL shows the best delay performance and the results are plotted as shown in Figure 10. Since, the proposed ones have good delay performance through pull-up stage using CPTL than DCVSL structure.

4. Conclusion

In this paper, initially a new structure for DCVSL pull-up stage using complementary transistor logic (CPTL) structure has been proposed initially, that has provided complementary outputs. And there on a new structure of ULPD-DCVSL is introduced for high performance and low power VLSI design. The results reveal the potential speed-up of differential circuits over the conventional static DCVSL circuits. The proposed ULPD-DCVSL-based delay cells reduce the propagation delay problem ($T_{PLH} > T_{PHL}$). Compared with the existing design techniques, ULPD-DCVSL is actually

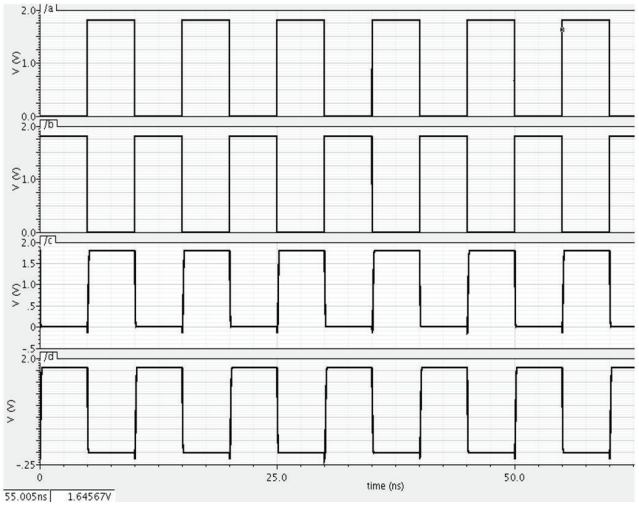

Figure 9: Simulated input and output waveforms of proposed DCVSL circuit using CPTL logic.

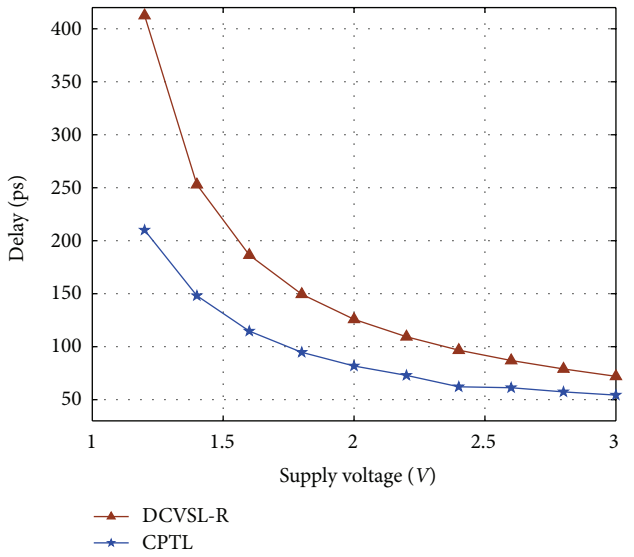

Figure 10: Delay versus supply voltage of DCVSL and CPTL structure.

considered to be the best of its kind at the different capacitive load range. For more robust design, however, ULPD-DCVSL might also be the best choice. A CPTL-DCVSL shows the possibility of using pull-up stage DCVSL to achieve a very high performance design. While sneaking into the dynamic circuit design, ULPD-DCVSL is also proved to be the best power-delay product.

References

[1] L. Heller, W. Griffin, J. Davis, and N. Thoma, "Cascode voltage switch logic: a differential CMOS logic family," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC '84)*, vol. 26, pp. 16–17, 1984.

[2] S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill, Singapore, 1999.

[3] P. Ng, P. T. Balsara, and D. Steiss, "Performance of CMOS differential circuits," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 6, pp. 841–846, 1996.

[4] D. Somasekhar and K. Roy, "Differential current switch logic: a low power DCVS logic family," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 7, pp. 981–991, 1996.

[5] M. W. Allam and M. I. Elmasry, "Dynamic current mode logic (DyCML): a new low-power high-performance logic style," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 550–558, 2001.

[6] D. Woon Kang and Y.-B. Kim, "Design of Enhanced Differential Cascode Voltage Switch Logic (EDCVSL) circuits for high fan-in gate," in *ASIC/SOC Conference*, pp. 309–313, September 2002.

[7] R. K. Bryanton and C. McMullen, "The decomposition and factorization of Boolean expressions," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '98)*, pp. 49–54, 1998.

[8] K. M. Chu and D. L. Pulfrey, "A comparison of CMOS circuit technicues: differential cascode voltage switch logic versus conventional logic," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 528–532, 1987.

[9] M. E. S. Elrabaa, "A new static differential CMOS logic with superior low power performance," in *Proceedings of the 10th IEEE International Conference on Electronics, Circuits and Systems (ICECS '03)*, vol. 2, pp. 810–813, December 2003.

[10] D. Z. Turker, S. P. Khatri, and E. Sánchez-Sinencio, "A DCVSL delay cell for fast low power frequency synthesis applications," *IEEE Transactions on Circuits and Systems I*, vol. 58, no. 6, pp. 1225–1238, 2011.

[11] I. Hassoune, D. Flandre, I. O'Connor, and J. D. Legat, "ULPFA: a new efficient design of a power-aware full adder," *IEEE Transactions on Circuits and Systems I*, vol. 57, no. 8, pp. 2066–2074, 2010.

[12] D. Levacc, C. Liber, V. Dessard, and D. Flandre, "Composite ULP diode fabrication, modelling and applications in multi-Vth FDSOI CMOS technology," *Solid State Electron*, vol. 49, no. 5, pp. 708–715, 2005.

[13] P. Sai Tejaswi and A. Srinivasulu, "A Schmitt trigger by means of complimentary pass transistor logic," *International Journal of Engineering Research and Applications*, pp. 5–7, 2012.