Research Article

Boundary Surface of 5-Valued Memory

Milan Guzan

*Department of Theoretical Electrical Engineering and Electrical Measurement, Technical University of Košice,
Park Komenského 3, 040 01 Košice, Slovakia*

Correspondence should be addressed to Milan Guzan; milan.guzan@tuke.sk

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The subject of research in this paper is multiple-valued (MV) memory cell—particularly the morphology of boundary surface of five-valued memory. By accepting the values of parasitic accumulation elements on the chip, very complicated morphology of the boundary surfaces occurs, which separates various attractors from each other. This is due to the occurrence of undesirable oscillations—a stable limit cycles, which makes it impossible to control memory. These dynamic attractors are so dominant that their regions of attraction even surround regions of attraction of static attractors—required logic levels of memory. Therefore, in the realization of the MV memory on the chip is necessary to know the values of the parasitic elements, because their presence may cause a malfunction of the memory. In this case, only calculation and displaying the boundary surface provides exact answers related to operation of the MV memory.

1. Introduction

Multiple-valued logic (MVL) compared to the binary logic has the advantage that in circuits with MVL, according to [1], are reduced the circuits providing transfer into higher orders. Thus, integration density increases and amount of arithmetic operations reduces. This advantage used the Intel corporation for development of MV ROM memory exploited in the coprocessor, but also companies such as NEC, Motorola, General Instruments, and Hitachi used up to 16-value memory [2].

While in the 80s of the last century MVL memories were designed based on MOS transistors [3–5], in the 90s of the last century they have already dominant resonant tunneling diodes (RTDs) [6–9]. To create elementary MVL memory, only two RTDs are sufficient instead of 6 transistors. This was also one of reasons why RTD broke into the MVL memory design. It should be noted that the use of transistors in the MVL is now up to date [10] thanks to a new carbon nanotube FETs [11–13]. Other advantages of using RTDs are the ability to work in the GHz region, occupying a tiny area on the chip, the design of multipeak RTD being easy, and having a time-independent I - V characteristic. Change of I - V characteristic of GaAs tunnel diodes due to ageing in the 60s of the last century resulted in malfunction of computers based on these

semiconductor devices [14]. Although at 90s of the last century the most publication activity of using RTD in MVL memories was noticed, US patent [15] proves continued recency of the problems MVL memories based on RTDs. The advantage of using RTDs lies also in the fact that if RTD is characterised by n -peaks and both elements are identical, it is possible to create a memory that will be characterised up to $2n + 1$ stable states—logical levels. So, if $n = 4$, using two RTDs only, it is possible to design such memory which has up to 9 stable states. If we had used MOS transistors, we would have needed greater than 6 MOS transistors.

In order to control any memory, not only just MVL memory, exact investigation of dynamic properties of the elementary memory is necessary. It is not possible without the knowledge of the morphological characteristics of the boundary surface (BS) that separates the regions of attraction of particular attractors. BS is used not only in memories [16–20], but also in chaos generating circuits [21–24]. Therefore, this paper presents morphology of BS in the form of 2D cross-sections for two cases of five-valued elementary memory.

2. MVL Elementary Memory

Circuit of the MV elementary memory is shown in Figure 1. Capacities C_1 , C_2 include capacity of equivalent RTD circuit

FIGURE 1: Ternary memory circuit.

or parasitic capacity of the chip. Inductance L denotes inductance of leads to diode. Resistance R expresses the resistance of conductive connections on the chip. The symbols of non-linear elements correspond to resonant tunneling diodes. Dependence $i_2(u_2)$ represents I - V characteristic of element, and dependence $i_1(u_1)$ represents I - V characteristic of load. Both characteristics are piece-wise linear (PWL) characteristics with indicated break points U_1, U_2, U_3 and conductances g_0, g_1, g_2, g_3 . Supply voltage $U = 440$ mV.

The first ternary memories consisting of RTDs were analyzed in [25]. For $L = 10$ mH, $C_1 = C_2 = 4$ μ F ternary memory was characterized by three stable states, and memory control by current source ΔI was trouble-free. Work [26] showed that if L, C_1 , and C_2 are comparable with size of parasitic accumulation elements on the chip, a problem may occur. Ternary memory will be characterised not only by three, but four attractors! Newly created attractor is a stable limit cycle (SLC), which disables the memory. Later, two SLCs were found or even three (!) SLCs [27]. Circuit was then characterized by five or even six (!) steady states. Figure 2 illustrates the distribution of singularities in the projection to the u_2, i plane and Figure 3 Monge projection of 2D cross-sections of BS through the singularity N1. Symbols S1, S2, and S3 in Figure 2 correspond to stable singularities (attractors) and symbols N1 and N2 to unstable singularities. The same marking is used also in Figure 3.

For a color distinction of particular regions of attraction in Figure 3 the following applies:

- (i) the green, gray, and red colors represent regions of attraction for stable singularities S1, S2, and S3;
- (ii) yellow, purple, and blue colors represent regions of attraction of undesired SLCs—L1, L2, and L3.

Marks on SLCs as a cross and dot in a circle represent the intersection of L1, L2, and L3 through corresponding current (plane u_2, u_1) or voltage plane (plane u_2, i) [27]. The arrows on SLC illustrate the direction of representative point movement in the state space. Time marks in Figure 3 (projection into u_2, u_1 plane) illustrate the time interval of representative point movement on SLCs. L1, L2, and L3 are special because they are not tied to an unstable limit cycle as in the cases described in [14, 22, 28, 29]. The symbol L_N denotes absolutely unstable limit cycle. It is absolutely unstable because it lies on the boundary of the four (!) regions of

FIGURE 2: I - V characteristics of RTDs and singular points projected into the plane i, u_2 .

attraction and can be calculated only by backward integration [30].

The line denoted that EG1 graphically proves if BS is calculated correctly, because element of BS passing through unstable singularity N1 is tangent plane of green and gray regions of attraction just in N1. More information on the elements of singularities can be found in [16, 27, 31]. The presence of the three SLCs in ternary memory is interesting in terms of the theory of nonlinear circuits, but in terms of implementation of the memory, SLCs represent a warning. But it is possible to find such parameters L, C_1 , and C_2 , when SLCs are not present and memory can be realised [19]. The author of this paper is interested in BS morphology for five-valued elementary memory. A sure thing should be five attractors—logic states of elementary memory. However, the question is whether they will again present undesirable SLCs also in structures described in the next section, where L, C_1 , and C_2 will be comparable with parasitic values on the chip.

3. Five-Valued Memory

Circuit in Figure 1, as for ternary memory even for five-valued memory, is described by system

$$\begin{aligned} L \left(\frac{di}{dt} \right) &= U - Ri - (u_1 + u_2) \equiv Q_1, \\ C_1 \left(\frac{du_1}{dt} \right) &= i - f_1(u_1) \equiv Q_2, \\ C_2 \left(\frac{du_2}{dt} \right) &= i - f_2(u_2) + \Delta I \equiv Q_3. \end{aligned} \quad (1)$$

The expressions (2) and (3) from work [32] have been modified to express the PWL $i_2(u_2)$ and $i_1(u_1)$ characteristics,

FIGURE 3: Monge's projection of the cross-section (in singularity N1) of the boundary surfaces, stable limit cycles, and unstable limit cycle for considered $R = 0$, $L = 1 \cdot 10^{-10}$ H, and $C_1 = C_2 = 5 \cdot 10^{-13}$ F [27].

to form

$$\begin{aligned}
 f_k(u_k) = & \frac{1}{2} ({}^k g_0 + {}^k g_8) u_k \\
 & + \frac{1}{2} [({}^k g_1 - {}^k g_0) |u_k - {}^k U_1| \\
 & + ({}^k g_2 - {}^k g_1) |u_k - {}^k U_2| + \dots \\
 & + ({}^k g_8 - {}^k g_7) |u_k - {}^k U_8|] \\
 & - \frac{1}{2} [({}^k g_1 - {}^k g_0) {}^k U_1 \\
 & + ({}^k g_2 - {}^k g_1) {}^k U_2 + \dots \\
 & + ({}^k g_8 - {}^k g_7) {}^k U_8],
 \end{aligned} \quad (2)$$

$$\begin{aligned}
 f_k(u_k) = & \frac{1}{2} ({}^k g_0 + {}^k g_4) u_k \\
 & + \frac{1}{2} [({}^k g_1 - {}^k g_0) |u_k - {}^k U_1| \\
 & + ({}^k g_2 - {}^k g_1) |u_k - {}^k U_2| \\
 & + ({}^k g_3 - {}^k g_2) |u_k - {}^k U_3| \\
 & + ({}^k g_4 - {}^k g_3) |u_k - {}^k U_4|] \\
 & - \frac{1}{2} [({}^k g_1 - {}^k g_0) {}^k U_1 \\
 & + ({}^k g_2 - {}^k g_1) {}^k U_2 \\
 & + ({}^k g_3 - {}^k g_2) {}^k U_3 \\
 & + ({}^k g_4 - {}^k g_3) {}^k U_4],
 \end{aligned} \quad (3)$$

where ${}^k g_i$ are conductances and ${}^k U_i$ are the break points I - V characteristics. If $k = 1$, it concerned load, if $k = 2$, it concerned active device.

Expression (2) and parameters (4) or expression (3) and parameters (5) correspond to such I - V characteristics in order to achieve five stable singularities S1, S2, S3, S4, and S5. As is clear from Figure 4(a), both I - V characteristics are identical—defined by the relation (2). Since one RTD is active device and the second is load, it is possible to make 5 stable singularities. A similar comment applies to Figure 5(a), with the difference that the active and the load device are defined by the relation (3). To parameters (4) corresponds Figure 4(a) and to parameters (5) corresponds Figure 5(a). From both projections to the plane u_2 , i is obvious active and load device. Singularities N1, N2, N3, and N4 regularly separate stable singularity from each other, where

$$g_0 = g_2 = g_4 = g_6 = g_8 = 0.04 \text{ S};$$

$$g_1 = g_3 = g_5 = g_7 = -0.08 \text{ S};$$

(4)

$$U_1 = 60; \quad U_2 = 90; \quad U_3 = 150; \quad U_4 = 180;$$

$$U_5 = 240; \quad U_6 = 270; \quad U_7 = 330; \quad U_8 = 360 \text{ mV};$$

$$g_0 = 0.0833; \quad g_1 = -0.07; \quad g_2 = -0.018;$$

$$g_3 = 0.005; \quad g_4 = 0.045 \text{ S}; \quad (5)$$

$$U_1 = 60; \quad U_2 = 110; \quad U_3 = 190; \quad U_4 = 300 \text{ mV}.$$

When $\Delta I = 0$, the number of singularities of the system (1) and their coordinates is given by the system of algebraic equations

$$Q_1 = 0, \quad Q_2 = 0, \quad Q_3 = 0. \quad (6)$$

As in the case of ternary memory [27], control cross-sections of BS were made through unstable singularities by

FIGURE 4: (a) Projection of the I - V characteristics and depiction of the singular points into the plane i, u_2 for $R = 0 \Omega$. Cross-sections of the BS in the plane u_2, u_1 ; (b) $i = 0.4 \text{ mA}$. Values of the parasitic elements considered in all simulations are $L = 1 \cdot 10^{-10} \text{ H}$ and $C_1 = C_2 = 2.6 \cdot 10^{-13} \text{ F}$.

FIGURE 5: Projection of the I - V characteristics and depiction of the singular points into the plane i, u_2 for $R = 0 \Omega$. Cross-sections of the BS in the plane u_2, u_1 ; (b) $i = 0.94 \text{ mA}$. Values of the parasitic elements considered in all simulations are $L = 1 \cdot 10^{-10} \text{ H}$ and $C_1 = C_2 = 2.6 \cdot 10^{-13} \text{ F}$.

the grid method (Figures 4(b) and 5(b)). The grid method was first used in [21], and its principle is based on the following procedure. Cutting plane of BS is divided into $M \times N$ points—the initial conditions of solution of system (1) by the Runge-Kutta method. Each one representative point is attracted by some of the attractors. The result is then a 2D cross-section of BS where you can see the size of the regions of attraction corresponding to individual attractors in the circuit. Color figures in this paper, illustrating BS cross-sections, consist of 440×440 points. One figure, therefore, consists of 193 600 points.

Since all unstable singularities for the RTD parameters (4) have the same current coordinate, (Figure 4(b)) the cross-section of the BS was calculated and displayed for $i = 0.4 \text{ mA}$.

This image is a color key to Figure 6. Since $R = 0$, projection of intersections I - V surfaces with the plane u_2, u_1 is line. The symbol ($\bullet$) on the line indicates stable singularities S1–S5 and symbol ($+$) unstable singularities N1–N4. The fact, that N1–N4 lie exactly on the boundary of color regions proves that the cross-section of BS is calculated correctly. Designation S1–S5 is located in the color region corresponding to the region of attraction of incident attractor. Surprising finding was that the memory was characterized by another 10 (!) SLCs.

They are labeled as L1–L10, and colored regions are symmetrically distributed around the linear projection of I - V surfaces. For example, the region of the attraction of SLC L1 is marked by yellow. In one of the two yellow regions, you can find label L1. SLC L2 is marked by light green color

FIGURE 6: The projections of cross-sections into u_2, u_1 plane for the parameters (4) and current denoted in the figure (in mA).

labeled L2 (dark green color corresponds to the region of attraction for attractor S2). Last SLC-L10 in Figure 4(b) is marked by white color. Because of the symmetry of I - V characteristics and uniform spacing of singularities, BS cross-section in Figure 4(b) evokes a chessboard. This implies relatively the same size of the regions of attraction as for S1-S5, as well as for L1-L10. Since the presence of up to 10 SLCs was surprising for the author, he proposed hypothetical parameters of RTD (5). These parameters would be difficult to realize, but for verification, BS morphology of other five-valued memory is sufficient. Because the distribution of singularities is not as uniform as in the previous case, Figure 5(b) is not characterised by approximately equal regions of attraction as shown in the Figure 4(b). Cross-section of BS was realised through current level $i = 0.94$ mA, which is current level corresponding to unstable singularities N2 and N3. Symbols of labelling S1-S5 and N1-N4 and principles of SLC marking L1-L8 are the same as in the commentary to Figure 4(b). Although this structure contains 8 SLCs, the presence of even a single SLC memory makes this MV memory unusable.

FIGURE 7: The projections of cross-sections into u_2, u_1 plane for the parameters (5) and current denoted in the figure (in mA), where ${}^{N2,N3}_i = 0.94$ mA and ${}^{N1,N4}_i = 2.65$ mA.

BS morphology of both cases is shown in Figures 6 and 7 in the plane u_2, u_1 . The key to the location of singularities and the color regions of attraction is Figures 4(b) and 5(b) to Figures 6 and 7, respectively. The number placed at the top of the figure indicates the current in mA. Labels N2, N3, or N1, N4 instead of number labels in Figure 7 indicates, that the cross-sections of BS correspond to current levels of unstable singularities N2, N3, or N1, N4. These are listed in the figure caption. If we compare Figures 6 and 7, we can conclude that the BS morphology is quite complicated. At low or high current levels are dominant regions of attraction for SLC. Regions of attraction for S1-S5 are actually “encapsulated” by regions of attraction for SLC and in 3D state space form objects like “cones.”

4. Conclusion

Since the change of L , C_1 , and C_2 can significantly affect the functionality of the newly designed prospective memory,

it is almost a necessity to know the morphology of BS. Without its knowledge, it is very difficult to find the optimal parameters of the control pulse. Otherwise, the designer of memory is forced to use inefficient method of “trial-error” that does not explain the failure of memory, for example, due to the presence of SLCs. The possibility of practical utilization of SLCs, occurring in memories, is unknown to the author. Therefore, he evaluates negatively their presence in memory structures. Given that in the ternary memory such parameters L , C_1 , and C_2 were found, leading to the extinction of SLCs, it can be assumed that even in five-valued memory the same analogy would be possible. Then, BS morphology would be much easier. Presence of virtual saddle singularity, or cases of very complex BS morphology can even happen [19]. Mentioned cases make control memory impossible, despite the absence of SLC. Even under these notes, the knowledge of BS morphology is important part in the analysis of MV memories. Other activities for examining the points mentioned earlier will continue if author will meet the interest in science public.

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