Research Article

Fault Tolerant Operation of ISOP Multicell DC-DC Converter Using Active Gate Controlled SiC Protection Switch

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An active gate controlled semiconductor protection switch using SiC-MOSFET is proposed to achieve the fault tolerant operation of ISOP (Input Series and Output Parallel) connected multicell DC-DC converter. The SiC-MOSFET with high temperature capability simplifies the configuration of the protection circuit, and its on-resistance control by the active gate controller realizes the smooth protection without the voltage and the current surges. The first laboratory prototype of the protection switch is fabricated by using a SiC-MOSFET with a high frequency buck chopper for the active gate controller. The effectiveness of the proposed protection switch is verified, taking the impact of the volume reduction into account.

1. Introduction

The next generation DC distribution system has been proposed to realize the highly electrified low carbon society [1, 2]. A lot of power electronics converters are installed for the flexible power control in the system as shown in Figure 1. To achieve the flexible power control for the effective use of the electric power and the prevalence of the power converters, the high power density (highly efficient and ultracompact) DC-DC converters are indispensable.

The multicell DC-DC converter topology is one of options to accomplish the high power density. The intensive studies have been conducted [3–7], and the ISOP (Input Series and Output Parallel) multicell DC-DC converter using sixty-four low voltage cell converters has been reported as the 384 V-384 V, 19.2 kW converter with the power density of 10 W/cm³ [8].

One of the features of the ISOP multicell DC-DC converter is the fault tolerant operation which realizes the continuous power delivery after the defect of the single cell converter. The protection methodology using a semiconductor power switch, a current limiting inductor, and a reverse blocking diode has been already proposed [9]. However, the volume of the current limiting inductor affects the total power density of the multicell DC-DC converter significantly.

In this paper, the protection circuit using the SiC protection switch with the active gate control is newly proposed to downsize the volume of the protection components. In Section 2, the configuration of the multicell DC-DC converter and the conventional protection methodology for the fault tolerant operation are shown. In Section 3, the details of the protection circuit using SiC power device with the active gate control are introduced. In Section 4, the first laboratory prototype of the protection circuit using SiC-MOSFET is fabricated and its effectiveness is verified.

2. Multicell DC-DC Converter and Protection Methodology for Fault Tolerant Operation

2.1. Configuration of Multicell DC-DC Converter

The conceptual diagram of the multicell DC-DC converter is shown in Figure 2. The multicell DC-DC converter consists of a lot of low voltage and low power DC-DC cell converter modules. The higher rated voltage at the input side of the multicell DC-DC converter \(V_{IN}\) is achieved by connecting the cell converter modules in ISOP (Input Series and Output Parallel). The higher rated voltage at the output side \(V_{OUT}\) is also accomplished by connecting the cell modules in IPOS (Input Parallel and Output Series). The features of the multicell converter are summarized as follows:
(i) The efficiency $\eta$ (%) and the power density $D_p$ (W/cm$^3$) of the multicell converter depend on the single cell converter.

(ii) The I/O (Input/Output) voltages of the multicell converter are designed arbitrarily by the number of cell converters connected in ISOP and IPOS.

(iii) The utilization of the nonregulated (the constant duty ratio) dc-dc converter for the cell converter achieves the balanced voltage and current sharing among cell converters without any complicated feedback control systems [10].

(iv) The low voltage stress of the cell converter enables employing the low voltage and ultralow loss semiconductor power devices [11].

From the aforementioned features, the design of the single cell converter plays an important role in improving the performance of the multicell dc-dc converter. Now, the 384 V-384 V, 19.2 kW multicell converter with the power density of 10 W/cm$^3$ has been already developed by using the highly integrated dc-dc cell converter modules connected in ISOP-IPOS [8].

On the other hand, the multicell converter has the following drawbacks:

(i) The reliability of the multicell converter is generally lower than the reliability of the conventional single converter because of the total count of the electronic parts.

(ii) In the case of ISOP connection topology, the defect of the single cell converter module leads directly to the system failure of the multicell converter.

The protection circuit is indispensable for each cell converter in the ISOP multicell dc-dc converter to enhance the total converter reliability and to prevent the system failure.

2.2. Protection Methodology for Fault Tolerant Operation. The input terminal has to be shorted and the output terminal has to be opened for the defective cell converter in the ISOP multicell dc-dc converter to keep supplying the electric power. The basic protection methodology for the fault tolerant operation of ISOP dc-dc converter has been already reported [9].

Figure 3 shows the circuit configuration of the ISOP multicell dc-dc converter with the conventional protection circuit. The protection circuit consists of the semiconductor power switch $Q_i$, the gate driver for the switch, the current limiting inductor $L$, and the reverse blocking diode $D$. The protection behavior in the case of the failure of the cell converter 1 is described as follows:

1. In the steady state, the input voltage $V_{IN}$ is equally divided by the total number of cell converters $N$ and the divided voltages are injected to each cell ($V_{Cik} = V_{IN}/N$, $k = 1, 2, \ldots, N$).

2. After the cell converter 1 fails and its gate control stops, the input cell voltage $V_{C1}$ increases because the input and the output terminals of the cell converter 1 are opened.

3. The switch $Q_1$ is turned on to short the input terminal of the cell converter 1 when the voltage $V_{C1}$ exceeds the threshold for the overvoltage detection.

4. The input cell voltage $V_{C1}$ approaches to 0 V, and the input voltage $V_{IN}$ is injected to the remained cell converters. Each input voltage of the remained cell converter rebounds to $V_{IN}/(N - 1)$.

The successful behavior for the fault tolerant operation has been already reported. However, the large resonant
current appears in case the switch \( Q_1 \) is turned on because of the current limiting inductor \( L_1 \) and the input capacitor \( C_{i1} \). The massive inductors are required beside all cell converters to suppress the resonant current through the switch \( Q_1 \). The inductor volume prevents the fabrication of the high power density multicell dc-dc converter.

3. Active Gate Controlled SiC Protection Switch for Fault Tolerant Operation

3.1. Protection Methodology Using Active Gate Controlled Semiconductor Power Switch. Figure 4 shows the proposed protection circuit to remove the current limiting inductor. The proposed circuit consists of the protection switch \( Q \) and the active gate controller. The active gate controller provides the variable on-resistance of the protection switch \( Q \), controlling the gate to source voltage of the switch \( Q \) linearly [12–16]. In this paper, the high frequency buck chopper circuit was applied to the achieve the variable on-resistance for the active gate control.

In Figure 4, the protection switch \( Q_k \) is turned on in the case of the defect of the dc-dc cell converter \( k \). Under the high-speed switching operation, the surge current from the capacitor \( C_{i_k} \) flows through the protection switch \( Q_k \) because of no current limiting inductors. The high resistance of the protection switch \( Q_k \) is achieved instantaneously by the active gate controller to suppress the surge current at first. Then the resistance of the switch \( Q_k \) is gradually decreased to short the input terminal of the defective cell converter.

Figure 5 shows the circuit configuration to confirm the behavior of the active gate control experimentally. The defect of the dc-dc cell converter 1 is assumed here, and the protection switch \( Q_1 \) is turned on gradually by the gate driver based on the high frequency buck chopper. Parameters for the experiment are shown in Table 1.

![Figure 3: ISOP multicell dc-dc converter and conventional protection circuit.](image-url)

<table>
<thead>
<tr>
<th>Table 1: Parameters for active gate control operation.</th>
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<tbody>
<tr>
<td>Input voltage ( V_{IN} )</td>
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<tr>
<td>Output resistance ( R_{OUT} )</td>
</tr>
<tr>
<td>Input capacitance ( C_{i1}, C_{i2} )</td>
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<tr>
<td>Dc-dc cell converters 1, 2</td>
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<tr>
<td>Protection switch ( Q_1 )</td>
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<tr>
<td>Gate transistors ( Q_{g1}, Q_{g2} )</td>
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<tr>
<td>Frequency of ( Q_{g1}, Q_{g2} )</td>
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<tr>
<td>Gate inductance ( L_g )</td>
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<tr>
<td>Gate voltage ( V_{G} )</td>
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gate controlled semiconductor protection switch enables suppressing the current surge without the current limiting inductor.

3.2. SiC Power Device for Protection Switch. The stored energy in the input capacitor $C_{ik}$ is absorbed by the protection switch in the proposed protection circuit. The semiconductor device which has large SOA (Safe Operating Area) is appropriate for the protection switch. The SiC power device with the ultralow on-resistance and the high temperature capability is one of attractive options.

Figure 7 shows the current capability of the commercially available Si and SiC MOSFETs. The maximum value for the pulsed current density of the SiC-MOSFET and three
Si SJ (Super Junction) MOSFETs are compared, taking the chip areas for the above power devices into account. In this figure, the SiC-MOSFET has the higher current density to keep the normal operation. The plateau area where the maximum current density is independent of the horizontal axis in Figure 7 represents the maximum heat dissipation density of the power devices [12]. One of features of SiC power devices with the low on-resistance and the high temperature capability is shown here. This means that the SiC power device is suitable for the protection circuit of ISOP multicell converter.

4. Experiment for Fault Tolerant Operation of ISOP Multicell Dc-Dc Converter Using Active Gate Controlled SiC Protection Switch

4.1. Fault Tolerant Operation of ISOP Multicell Converter Using Four Cell Converters. The prototype of the protection system for the ISOP multicell dc-dc converter has been fabricated by using the SiC-MOSFET (1200 V, 80 mΩ from CREE) and the 100 kHz buck chopper for the active gate control. The circuit configuration is based on Figure 4 (N = 4), and the experimental apparatus is shown in Figure 8. This consists of four dc-dc cell converter modules (V048T480T006 from Vicor) and the SiC protection switch connected to the cell converter 1 mainly. The detailed parameters for this experiment are shown in Table 2.

![Figure 6: Active gate controlled gate to source voltage and drain current of protection switch.](image)

![Figure 7: Maximum current density of Si and SiC power devices for safe operation.](image)

<table>
<thead>
<tr>
<th>Table 2: Parameters for fabricating four cell ISOP converters with protection switch.</th>
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</thead>
<tbody>
<tr>
<td>Input voltage (V_{IN})</td>
</tr>
<tr>
<td>Resistive load</td>
</tr>
<tr>
<td>Protection switch (Q_1)</td>
</tr>
<tr>
<td>Active gate controller</td>
</tr>
<tr>
<td>Output inductance (L_{g1}) for active gate control</td>
</tr>
<tr>
<td>Cell converter (V048F480T006) (48 V-48 V, 300 W from VICOR)</td>
</tr>
<tr>
<td>Input cell capacitor (C_{ik}) ((k = 1, 2, 3, 4))</td>
</tr>
<tr>
<td>Number of cell converters</td>
</tr>
<tr>
<td>FPGA</td>
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</table>

The experimental result in case the cell converter 1 failed is shown in Figure 9. The gate to source voltage \(V_{gs1}\) of SiC-MOSFET, the input cell voltages \(V_{C1}, V_{C2}, V_{C3}\), and \(V_{C4}\), the output voltage \(V_{OUT}\), and the drain current through the SiC-MOSFET \(I_{Q1}\) are shown in this figure. In the steady state, all input cell voltages are kept at 24 V (\(\approx V_{IN} 96 V/4 \) cells). After the overvoltage detection of \(V_{C1}\), the SiC-MOSFET \(Q_1\) is turned on to short the input terminal of the cell converter 1. The voltage waveform \(V_{gs1}\) means that the on-resistance of the SiC-MOSFET is controlled to decrease gradually by the active gate control. The cell voltage \(V_{C1}\) approaches 0 V and...
the input voltages of the remained cell converters rebound to 32 V (≈ $V_{IN}$ 96 V/3 cells) without any surge. The current $i_{Q1}$ also increases gradually without surges and the electric power is kept supplying to the load through the remained three cell converters.

In Figure 9, the input cell voltages $V_{C2}$, $V_{C3}$, and $V_{C4}$ had no unbalances and no surges during the transition. This was accomplished by applying both the ISOP connection topology for equal current sharing of the cell converters and the proposed active gate controlled SiC protection switch.

The behavior of the ISOP connected multicell converter has been already analyzed [10]. The input voltage of the ISOP converter is equally divided to each cell converter by the equal current sharing in the steady state. In the case of the high-speed disturbance, the input voltage unbalance among the cell converters or voltage surges appears because of the mismatch of the response speeds of the cell converters.

The transition time which was sufficiently slower than the response speed of all cell converters was achieved by the active gate controlled SiC protection switch. The influences caused by the mismatched cell converters were minimized and the characteristics of all cell converters were uniformed under the controlled smooth transition.

The voltages of 32 V which was higher than 24 V were seen for the remained three converters $V_{C2}$, $V_{C3}$, and $V_{C4}$ under the fault tolerant operation. Generally, the input voltages of remained cell converters $V_{Ck}$ ($k = 1, 2, \ldots, N$) rise to $V_{IN}/(N - 1)$ in case the single cell converter fails under the fault tolerant operation, although the input cell voltages are $V_{IN}/N$ under the steady state operation. The threshold values for the overvoltage protection $V_{OV}$ and the undervoltage protection $V_{UV}$ have to be designed as the following equations:

$$V_{OV} > \frac{V_{IN}}{N - 1}$$

$$V_{UV} < \frac{V_{IN} - V_{OV}}{N} - \frac{V_{IN}}{N - 1}.$$ (1)

In Figure 9, the input voltages of the remained cell converters were 32 V (≈ 96 V/3) under the fault tolerant operation and the threshold value $V_{OV}$ was set at 35 V. Each cell converter has to be designed taking the above voltage range for the fault tolerant operation into account.

As the number of cell converters $N$ increases, the input voltages of the remained cell converters under the fault tolerant operation approach the voltages under the steady state operation. This means that the OV and the UV protections are activated simply because the influence of the voltage overshoot caused by the fault tolerant operation becomes small.

### 4.2. Application Effect of Active Gate Controlled SiC Protection Switch for Volume Reduction

The proposed protection circuit removes the current limiting power inductor in the conventional protection circuit. On the other hand, the proposed circuit requires the output inductor of the buck chopper for the active gate control. The inductor volumes for the conventional and the proposed circuits are compared here.

The inductor volume is generally proportion to the stored energy in the inductor. In the conventional protection circuit in Figure 3, the stored energy of the current limiting inductor $L_k$ corresponds to the stored energy in the input capacitor $C_{ik}$. 
The volume of the current limiting inductor $V_{L_k}$ is expressed by the following equation:

$$V_{L_k} = f\left(\frac{1}{2} \cdot L_k \cdot i_{L_k}^2\right) = f\left(\frac{1}{2} \cdot C_{ik} \cdot v_{Cik}^2(0)\right).$$  \hspace{1cm} (2)

In this paper, the capacitance $C_{ik}$ is 22 $\mu$F from Tables 1 and 2. The voltage $v_{Cik}(0)$ means the threshold value to detect the overvoltage and this voltage was set at 35 V as shown in Figure 9. The transferred energy from the capacitor to the inductor was approximately 13.5 mJ.

In the proposed circuit in Figure 4, the inductance of the active gate controller depends on the switching frequency of the buck chopper. The inductor volume $V_{L_g}$ is expressed as follows:

$$V_{L_g} = f\left(\frac{1}{2} \cdot L_g \cdot i_{g}^2\right).$$  \hspace{1cm} (3)

From Table 2, the inductance for the active gate control was 330 $\mu$H here. This inductance was designed to suppress the ripple current through the inductor within 10% for the rated gate current $i_g$ of 1 A under 100 kHz switching operation. The rated current of 1 A is enough for the gate drive circuit because the switching speed of the protection switch is not fast. The stored energy of the inductance for the active gate drive circuit was approximately 170 $\mu$J.

Figure 10 shows the relationship between the volume and the stored energy of the commercially available power inductor. The gradient of this graph means the function $f$ in (2) and (3). The inductor volumes for the conventional and the proposed circuits are obtained from this figure. The volume of 90 cm$^3$ is required for the conventional protection circuit and the volume of 3.5 cm$^3$ is necessary for the proposed protection circuit. The inductor volume for the active gate controller can be reduced by increasing the switching frequency of the buck chopper.

Figure 11 shows the application effect of the proposed protection circuit to reduce the total volume of the multicell dc-dc converter. The volume of the single cell converter V048F480T006 in Table 2 was 4.8 cm$^3$ for the rated output power of 300 W. The volume of the current limiting inductor for each cell converter was 90 cm$^3$ from Figure 10. This means that the power density of the multicell dc-dc converter is determined by the inductor in the case of the conventional protection circuit. In the case of the proposed protection circuit, the volume of the inductor for the active gate driver was 3.5 cm$^3$ under the switching frequency of 100 kHz. The inductor volume was smaller than the volume of the cell converter, and the proposed circuit has the potential to achieve smaller inductor volume by increasing the switching frequency of the active gate driver. This means that the high power density and the highly reliable multicell dc-dc converter will be developed by using the proposed protection methodology.

5. Conclusions

The SiC protection switch with the active gate control was proposed for the fault tolerant operation of ISOP multicell dc-dc converter. The first laboratory prototype of the protection switch using SiC-MOSFET (1200 V, 80 m$\Omega$ from CREE) with the 100 kHz buck chopper was fabricated to confirm the effectiveness of the active gate control. The experiment using four dc-dc cell converters and the SiC protection switch verified the fault tolerant operation without the voltage and the current surges in transient.

The inductor for the active gate control will be downsized by operating the buck chopper under higher switching frequency operation. The proposed approach solves the key issue in the ISOP multicell converter and this contributes to realizing the low carbon society using high power density and highly reliable converters.
Competing Interests
The authors declare that there is no conflict of interests regarding the publication of this paper.

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