Hindawi Publishing Corporation
Journal of Engineering
Volume 2016, Article ID 9206124, 11 pages
http://dx.doi.org/10.1155/2016/9206124

Research Article

Microcontroller Based Flexible Modulation Scheme of MLI Operation for Selective Lower Levels: A Knowledge Based Approach

R. K. Dhatrak,[1] R. K. Nema,[1] and D. M. Deshpande[2]

[1]*Department of Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal 462051, India*
[2]*Department of Electrical and Electronics Engineering, Sagar Institute of Research Technology and Science, Bhopal 462051, India*

Correspondence should be addressed to R. K. Dhatrak; rkdhatrak@gmail.com

Received 30 November 2015; Revised 7 April 2016; Accepted 13 April 2016

Academic Editor: Jiun-Wei Horng

In today's industrial world multilevel inverter (MLI) got a significant importance in medium voltage application and also a very potential topic for researchers. It is experienced that studying and comparing results of multilevel inverter (MLI) at distinct levels are a costlier and time consuming issue for any researcher if he fabricate different inverters for each level, as designing power modules simultaneously for different level is a cumbersome task. In this paper a flexible quotient has been proposed to recognize possible conversion of available MLI to few lower level inverters by appropriately changing microcontroller programming. This is an attempt to obtain such change in levels through simulation using MATLAB Simulink on inductive load which may also be applied to induction motor. Experimental results of pulse generation using dsPIC33EP256MC202 demonstrate the feasibility of proposed scheme. Proposed flexible quotient successfully demonstrates that a five-level inverter may be operated as three and two levels also. The paper focuses on odd levels only as common mode voltage (CMV) can be reduced to zero and performance of drives is better than even level. Simulated and experimental results are given in paper.

1. Introduction

It is a laborious and costlier work to design different level inverter modules to investigate any particular issue. To obtain different level operations from a single power module is a better solution to this issue. In this paper an attempt has been done to address this issue. This method makes it possible to design at least three different level inverters from any higher (more than five) odd level inverter. Two- and three-level inverter can be designed from any odd level inverter having levels more than five by properly programming microcontroller. A flexible quotient proposed will help researchers to forecast possible inverter operations at few lower levels using the available higher MLI.

A five-level inverter can be used as two- as well as five-level inverter using sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) technique [1, 2]. It is possible to design a controller programming for SVPWM and SPWM. In this paper SPWM technique has been implemented. The same scheme can be extended to cascade H-bridge and flying capacitor MLI, by properly selecting the switching states of inverter. As the number of switches used in these basic topologies is same, for predicting the possible conversion of MLI same technique may be used but modulation scheme is different for different topologies. Modulation scheme in H-bridge is quiet similar to diode clamped inverter but in flying capacitor it has to be properly modified.

Investigation on total harmonic distortion (THD) in line voltage, phase voltage, and line current as well as CMV has been done. As the level of inverter increases percentage THD and CMV also reduce without using extra circuitry like filters. Application of such flexible inverter level adjustment using available inverter in generalized manner is not reported in literature. DSP 2812 is used to develop the pulses in the available literature. Instead of using a costlier

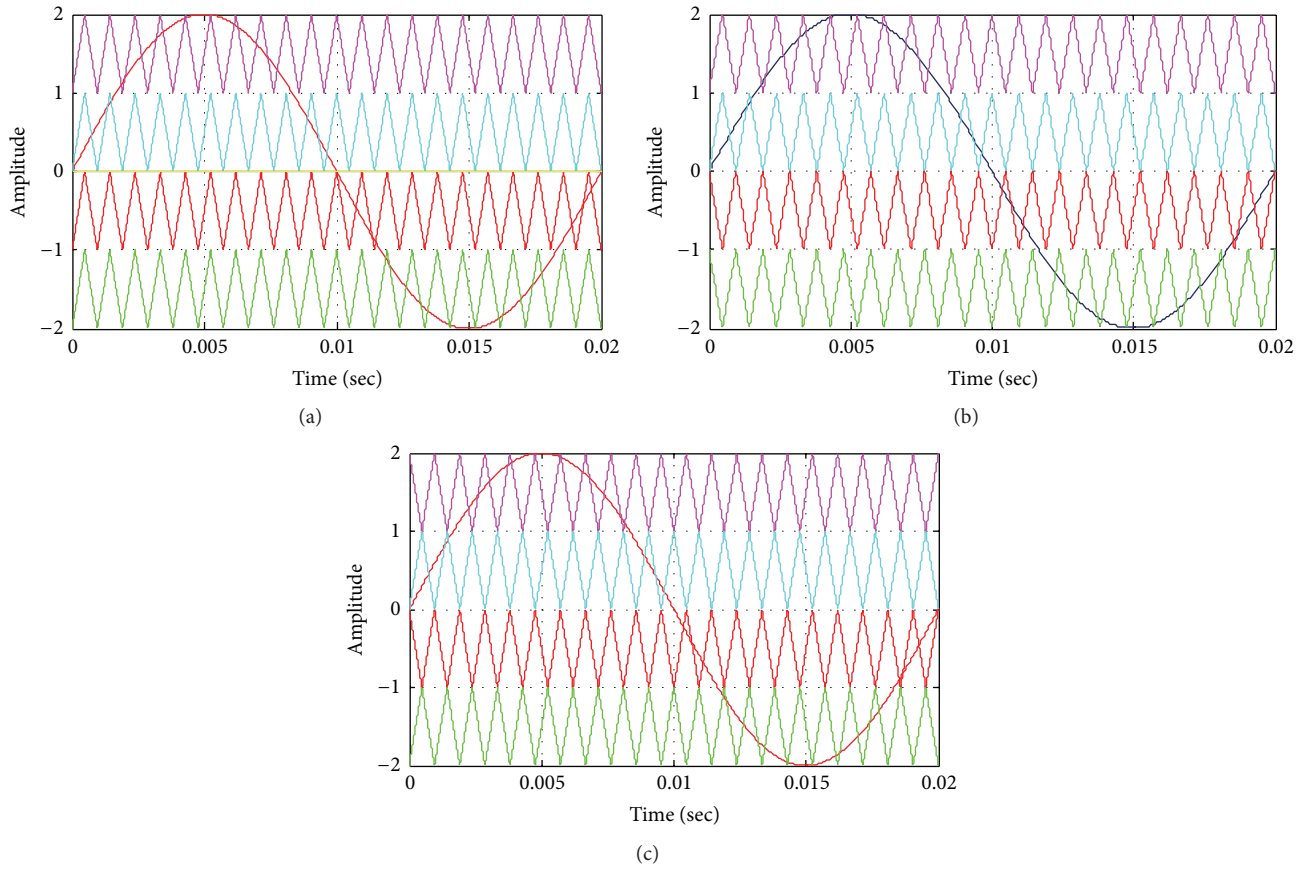


Figure 1: Carrier wave and modulating waveform: (a) PD, (b) POD, and (c) APOD.

and complicated DSP controller a very cheap and simple programming dsPIC33EP256MC202 microcontroller is used to develop pulses of five-level inverter in this work.

This paper is organized as follows. Basic modulation techniques are reviewed in Section 2. Importance of diode clamped multilevel inverter for industrial application is discussed in Section 3. Section 4 gives the basic theme to explain the principle of this scheme. The development of modulation scheme is discussed in Section 5. Some experimental results, necessary microcontroller circuit, and proper voltage regulation circuit for microcontroller are explained in Section 6. Simulation results and their comparisons are discussed in Section 7. Some conclusions are drawn in Section 8.

2. Modulation Techniques

The main modulation techniques used for multilevel inverters are summarized as follows [3, 4]:

(1) Sinusoidal pulse width modulation (SPWM).

(2) Space vector pulse width modulation (SVPWM).

(3) Selective harmonic elimination pulse width modulation (SHEPWM).

First technique can be easily applicable to multilevel inverter by digital controller as it does not require any complex computation. Second and third techniques are complicated as they need some extra computations [3, 4]. In this paper focus is on the first method. The number of carrier signals required for N level inverter is $(N - 1)$. Frequency and peak to peak amplitude of all carrier waves should be the same. SPWM can be again classified according to the phase position of the triangular carrier waveforms [1, 3, 4] as follows:

(1) Phase disposition (PD): all carriers are in phase with one another (Figure 1(a)).

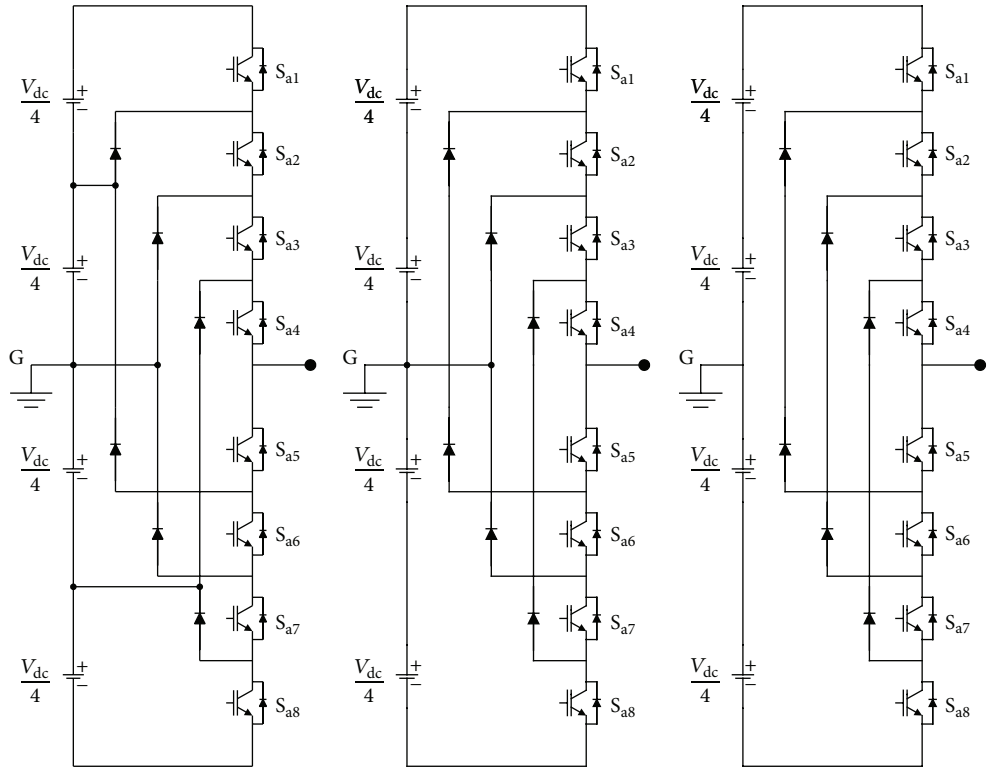
(2) Phase opposite disposition (POD): carriers above zero reference are in phase but in antiphase to those below zero reference (Figure 1(b)).

(3) Alternate phase opposite disposition (APOD): as the name indicates carriers in alternate layers are in phase opposition (Figure 1(c)).

Above three techniques can be applied with new modulation scheme. Simulation results using PD technique are provided to validate the scheme. This scheme may also be used with SVPWM and SHEPWM modulation technique.

3. Multilevel Inverter

One leg of a five-level inverter which is considered for this study is as shown in Figure 2(a). A diode clamped multilevel



(a) Five-level inverter (b) Three-level inverter (c) Two-level inverter

Figure 2: Various inverter configurations.

inverter topology has been used since it requires only one dc source and can be easily used for medium voltage applications in industries. One of the serious issues of diode clamped multilevel inverter is dc-bus voltage unbalancing [5]. Since voltage balancing is not concerned with this study, separate dc sources have been considered for dc buses. The same inverter may function as three-level inverter (Figure 2(b)) and two-level inverter (Figure 2(c)) by changing the gating signals of the switches.

4. Methodology

At first one has to decide the maximum level up to which study has to be carried out. Then we may find how many different levels may be possible to obtain from the same power module. The total number of switches used in N level inverter in one limb of the polyphase circuit is $2 * (N - 1)$. If series connected switches are used then they should be equally divided in $(N - 1)$ groups and each group of switches is turned on simultaneously by controlling circuit. Suppose that N level inverter has to be converted into two-level inverter; then $2 * (N - 1)/2$ switches are turned on simultaneously. If the same inverter is used for three-level inverter then the total number of switches which turned on simultaneously is $2 * (N - 1)/4$. In general if M is the level to which the available N level inverter is to be converted then the number of switches required to be turned on simultaneously is $2*(N-1)/2*(M-1)$, that is, $(N-1)/(M-1)$, where $M \leq N$. The ratio $(N - 1)/(M - 1)$ is called flexibility quotient. If this flexibility quotient is an integer number then that level inverter can be designed. Suppose that we have 5-level inverter which is to be converted to 3-level inverter; then the number of switches turned on simultaneously is $2 * (5 - 1)/2 * (3 - 1) = 8/4 = 2$ or $(5-1)/(3-1) = 2$ and for two-level $2 * (5-1)/2 * (2-1) = 8/2 = 4$ or $(5 - 1)/(2 - 1) = 4$. If the quotient is fraction then the inverter cannot be designed. Let the 7-level inverter be converted; then it can be converted to two- and three-level inverter but cannot be converted to five-level inverter as $(7 - 1)/(5 - 1) = 1.5$, which is a fraction. In this paper to illustrate the above rule five-level inverter is considered and operates it as two- and three-level inverter. A modulation scheme for the same is discussed in next section. Table 1 shows possible conversion of inverter levels from available inverters up to 29 level.

5. Modulation Scheme

This scheme may be applied to PD, POD, and APOD, SPWM modulation techniques. To validate the scheme it is applied to PD technique in this study. The modulation scheme for five-, three-, and two-level inverters of phase A is shown in Figures 3(a), 3(b), and 3(c). Modulation scheme for phase B and phase C is similar to this except there is a phase difference of 120 and 240 electrical degrees in reference sinusoidal wave. Carrier signals are the same for all the three phases. In five-level inverter four carrier signals are used. The firing signals

Table 1: Possible converted level from available inverter.

Available level	Converted level														
	2	3	5	7	9	11	13	15	17	19	21	23	25	27	29
Twenty-nine	√	√	√					√							√
Twenty-seven	√	√												√	
Twenty-five	√	√	√	√	√		√						√		
Twenty-three	√	√										√			
Twenty-one	√	√	√			√					√				
Nineteen	√	√		√						√					
Seventeen	√	√	√		√				√						
Fifteen	√	√						√							
Thirteen	√	√	√	√			√								
Eleven	√	√				√									
Nine	√	√	√		√										
Seven	√	√		√											
Five	√	√	√												
Three	√	√													

Table 2: Switching states of five-level inverter.

Output pole voltage	Switching state								Switching function
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	
$V_{dc}/2$	1	1	1	1	0	0	0	0	2
$V_{dc}/4$	0	1	1	1	1	0	0	0	1
0	0	0	1	1	1	1	0	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0	−1
$-V_{dc}/2$	0	0	0	0	1	1	1	1	−2

Table 3: Switching states of three-level inverter.

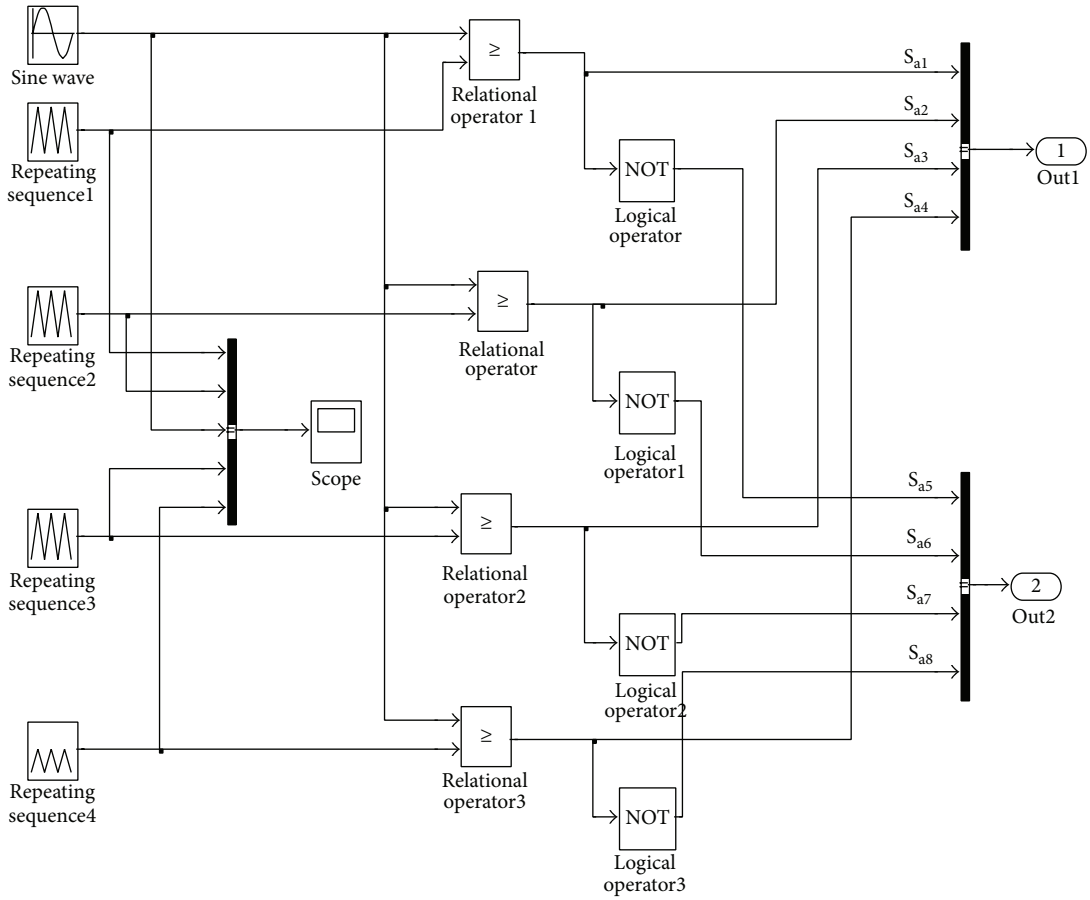
Output pole voltage	Switching state								Switching function
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	
$V_{dc}/2$	1	1	1	1	0	0	0	0	1
0	0	0	1	1	1	1	0	0	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1	−1

Table 4: Switching states of two-level inverter.

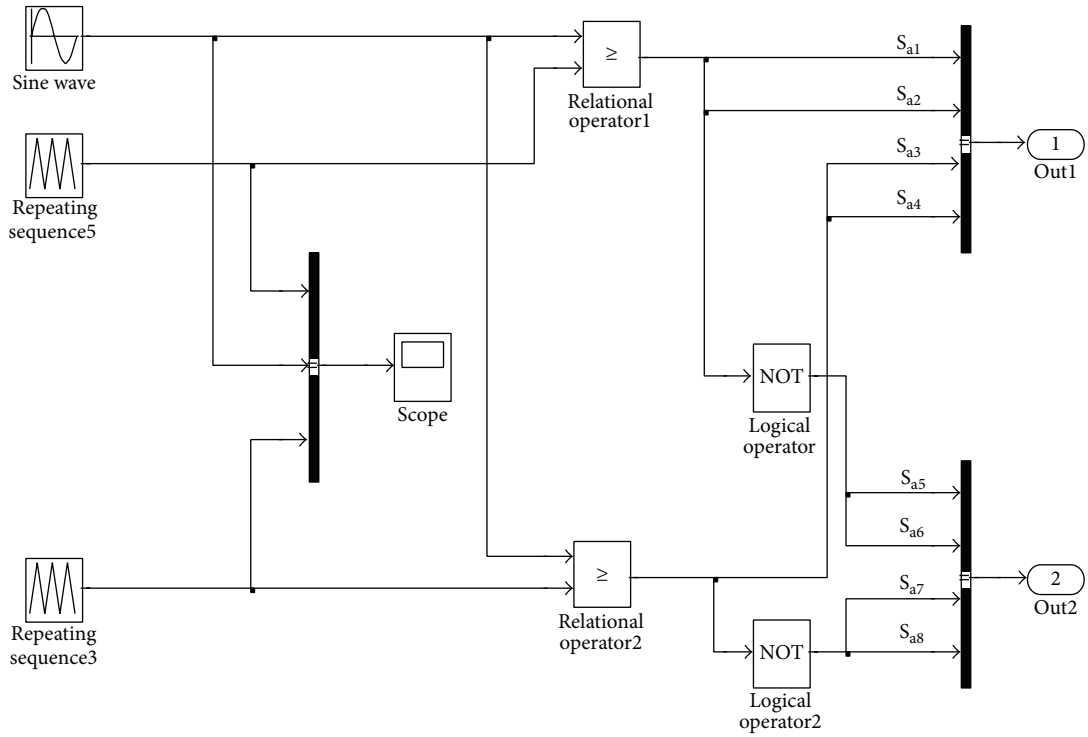
Output pole voltage	Switching state								Switching function
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	
$V_{dc}/2$	1	1	1	1	0	0	0	0	1
$-V_{dc}/2$	0	0	0	0	1	1	1	1	−1

are given to S_{a1} to S_{a4} after comparing carrier and reference wave; other four switches S_{a5} to S_{a8} act complementary to them. The switching states are given in Table 2. In three-level modulation schemes only two carrier signals are used. The signals are given to two switches simultaneously. S_{a1} and S_{a2} are turned on at the same time, and S_{a5} and S_{a6} act complementary to them. S_{a3} and S_{a4} are turned on at the same time, and S_{a7} and S_{a8} act complementary to them. The switching states are clearly mentioned in Table 3. In two-level inverter only one carrier signal is used. Four switches S_{a1} to S_{a4} are turned on and off simultaneously. Other four switches S_{a5} to S_{a8} act complementary to them as per the switching states in Table 4. It is observed that performance characteristics of inverter using this modulation scheme and conventional modulation scheme are exactly matched with each other.

According to this modulation scheme the pulses of five-, three-, and two-level inverter are shown in Figures 4(a), 4(b), and 4(c). From Figures 4(b) and 4(c) it is observed that these pulses are exactly matched with conventional two- and three-level inverter as shown in Figures 5(a) and 5(b). If the pulses of Figure 4(a) are connected properly it will become the output of five-level inverter. If the pulses of Figure 4(b) are connected properly then these pulses match exactly with

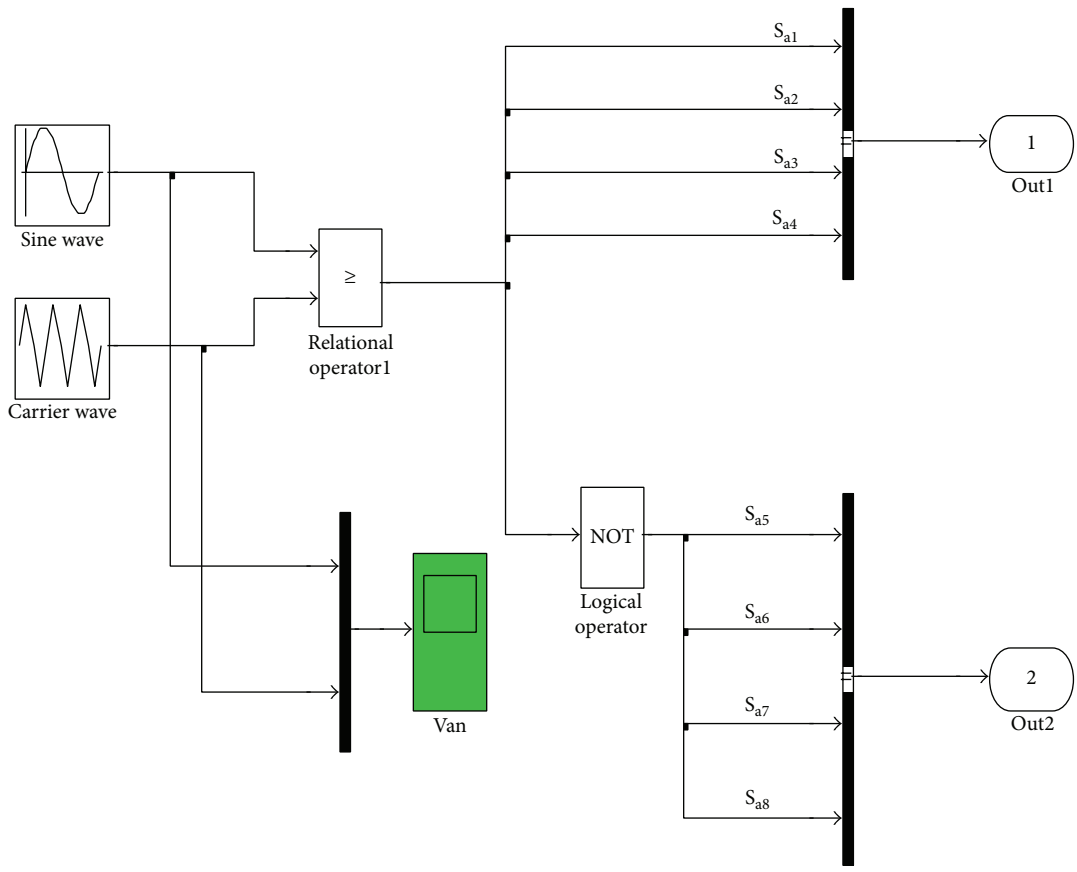


(a)



(b)

Figure 3: Continued.



(c)

Figure 3: Modulation schemes: (a) five-level inverter, (b) five-level inverter as three-level inverter, and (c) five-level inverter as two-level inverter.

conventional three-level inverter as shown in Figure 5(a). Similarly if pulses of Figure 4(c) are connected properly it will become the pulses of conventional two-level inverter as shown in Figure 5(b). Magnitude of each triangular carrier signal is 1, such that four signals are used in five-level inverter; hence pulses height varies from 0 to 4. The height in Figures 4(b) and 4(c) also proves that the pulses in corresponding switches are in phase; that is, they take place exactly at the same time. In conventional three-level inverter, two carrier signals are used and hence pulse height varies from 0 to 2 as shown in Figure 5(a). In two-level inverter only one carrier signal is used and hence pulses height varies from 0 to 1. The results are observed to be correct as per theoretical knowledge which validate the scheme.

6. Experimental Pulses Generation

Figures 4 and 5 pulses can be generated using dsPIC33EP256MC202 microcontroller. Regulated power supply required to drive this controller is as shown in Figure 6. The necessary 3.3 voltage is obtained using regulator IC 33CV. The minimum circuitry required to drive this controller is shown in Figure 7 [6]. The complete experimental setup is shown in Figure 8. The regulated supply of 3.3 volt obtained from this power supply is fed to PIN 1 and PIN 8 of microcontroller.

The microcontroller programming is developed to generate pulses for two-, three-, and five-level inverter using eight IGBTs. The pulses are observed simultaneously in four IGBTs when they are fired simultaneously for two-level inverter. In three-level inverter two IGBTs are fired simultaneously and the pulses in these IGBTs occurred at the same time. In five-level inverter each IGBT fires as per firing table given in Table 2. The experimental results observed on TPS 2024 B Tektronix DSO are shown in Figures 9(a), 9(b), and 9(c). These experimental pulses also exactly match with simulated pulses shown in Figure 4 which validate the scheme.

7. Comparison of Newly Modulated and Conventional Multilevel Inverter

Using Figure 3 modulation scheme five-level inverter can be used as two- and three-level inverter. The parameters used for the simulations are given in Table 5. The results are compared with the conventional two- and three-level inverters. It is observed that the results are nearly matched in conventional inverter and this newly modulated scheme inverter (Figures 10–14). Line voltage, phase voltage, and line current RMS,

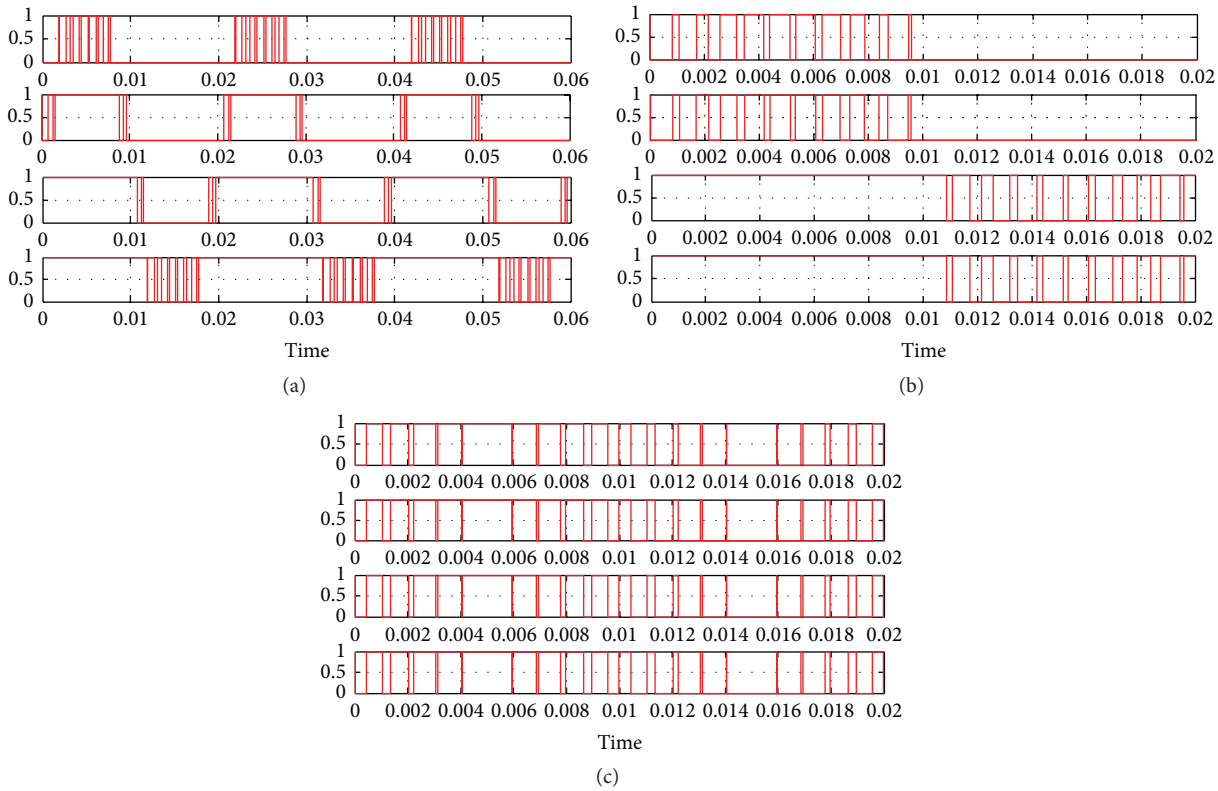


Figure 4: Simulated pulses of five-level inverter as (a) five-level inverter, (b) three-level inverter, and (c) two-level inverter.

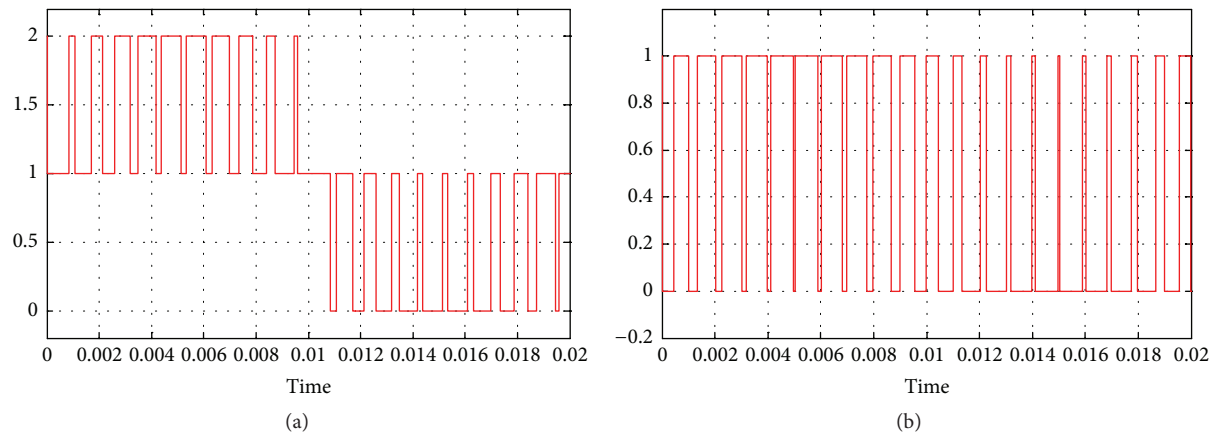


Figure 5: Pulses conventional inverter: (a) three-level inverter and (b) two-level inverter.

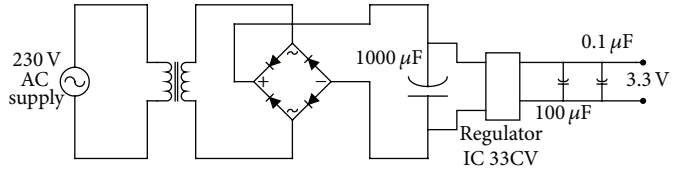


Figure 6: Power supply circuit for dsPIC33EP256MC202 controller.

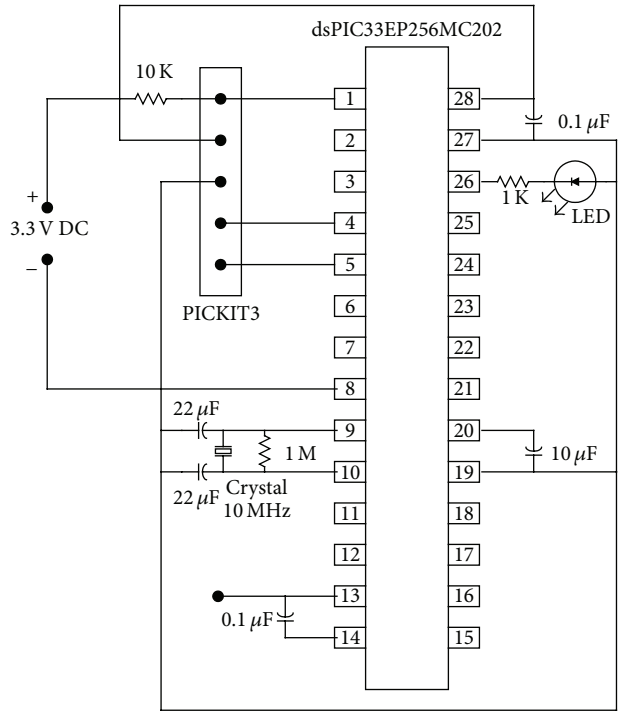


Figure 7: Minimum required circuitry to drive dsPIC33EP256MC202.

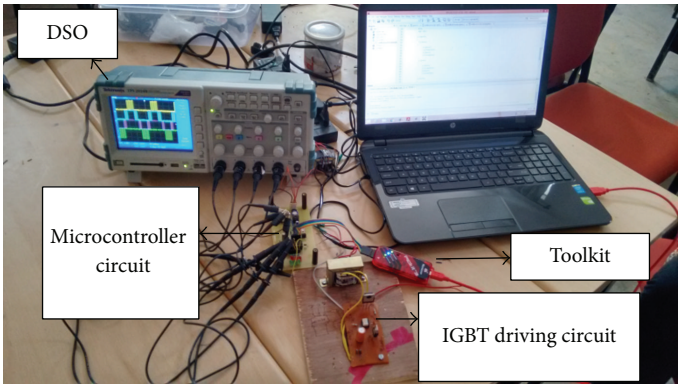


Figure 8: Photograph experimental setup.

Table 5: Simulation parameters.

Parameter	Quantity
Reference frequency	50 Hz
Carrier frequency	1050 Hz
Modulation index	0.8
V_{dc}	400 V
Load resistance	200 Ω
Load inductance	477.7 mH

peak, and their THD contents are tabulated in Table 6. This table also gives the value of CMV. It is observed that % THD of voltage and current decreases with the level of the inverter. CMV is defined as the voltage between star point of the three phases and system ground. CMV may also be defined as the arithmetic mean of the three-phase voltages. This voltage is the root cause of the shaft voltage and bearing current issue in three-phase induction motor. These bearing currents may cause premature failure of the bearing. CMV also reduces with increasing inverter level without using any filters.

8. Conclusion

The results of proposed flexible operation scheme for five-level inverter to three- and two-level inverters match exactly

Table 6: Tabular comparison of line voltage, phase voltage, and line current

Type of inverter	Line voltage (volt)			Phase voltage (volt)			Line current (amp)			CMV
	Peak value	RMS value	% THD	Peak value	RMS value	% THD	Peak value	RMS value	% THD	
Five-level as two-level	277.1	195.5	91.81	160	113.1	145.74	0.6401	0.4526	9.47	200
Conventional two-level inverter	277.1	195.9	91.81	160	113.1	145.74	0.6401	0.4526	9.47	200
Five-level as three-level	277.1	195.9	42.03	159.9	113.1	76.82	0.6398	0.4524	6.00	133.3
Conventional three-level inverter	276.9	195.8	42.12	159.8	113	76.96	0.6391	0.4521	6.01	133.33
Five-level as five-level	276.2	195.3	22.01	159.5	112.8	38.56	0.6379	0.4511	4.18	66.66

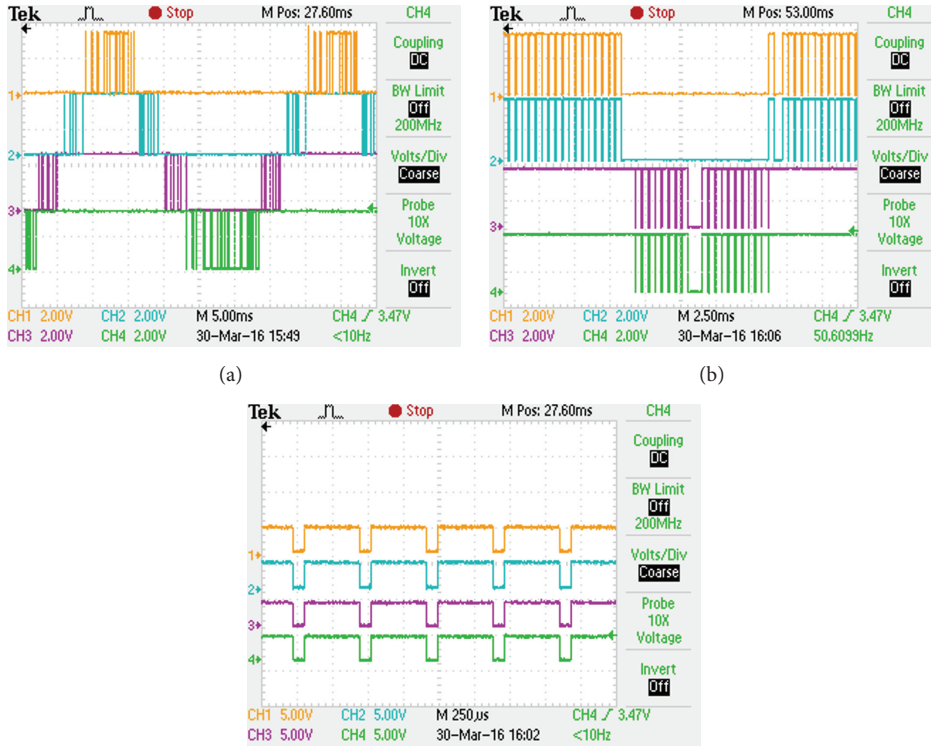


Figure 9: Experimental pulses of five-level inverter as (a) five-level inverter, (b) three-level inverter, and (c) two-level inverter.

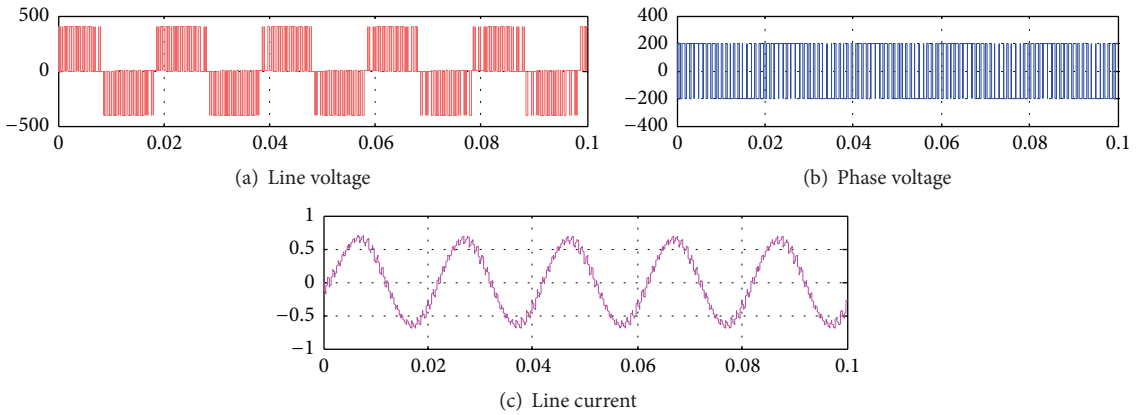
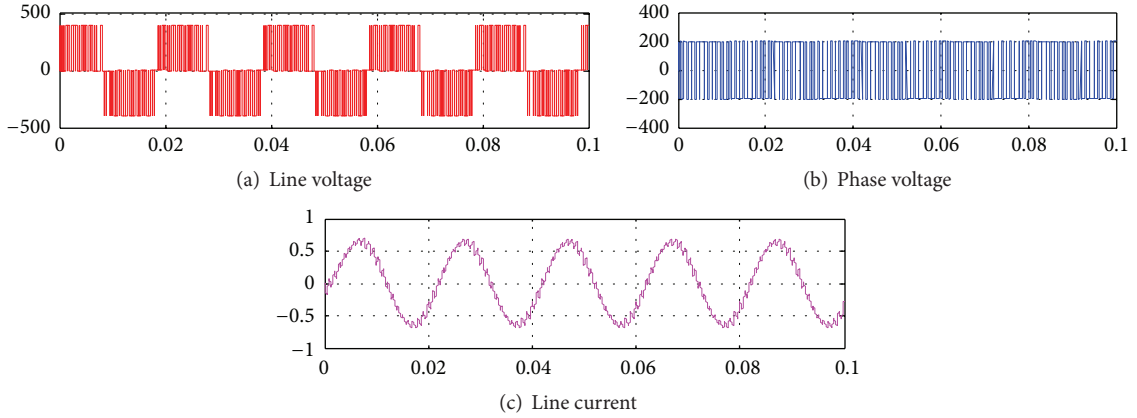


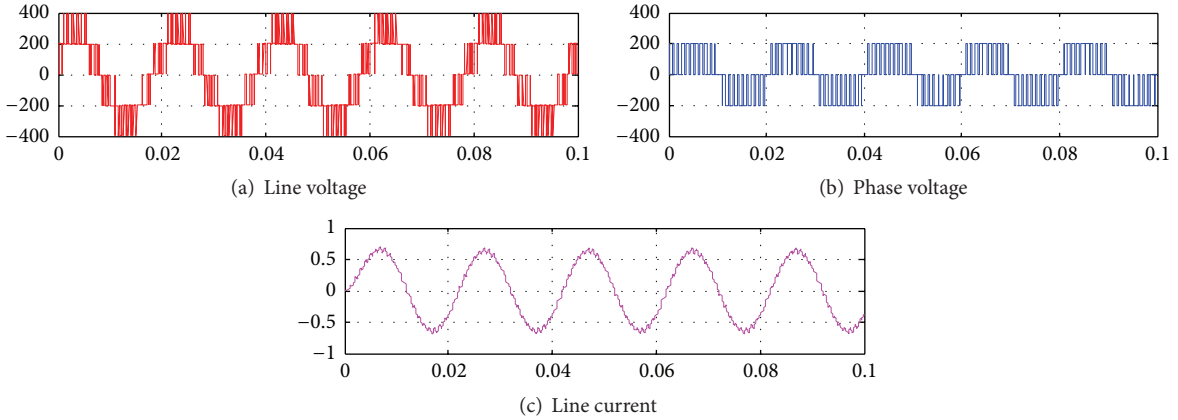
Figure 10: Five-level inverter as two-level inverter.



(a) Line voltage (b) Phase voltage

(c) Line current

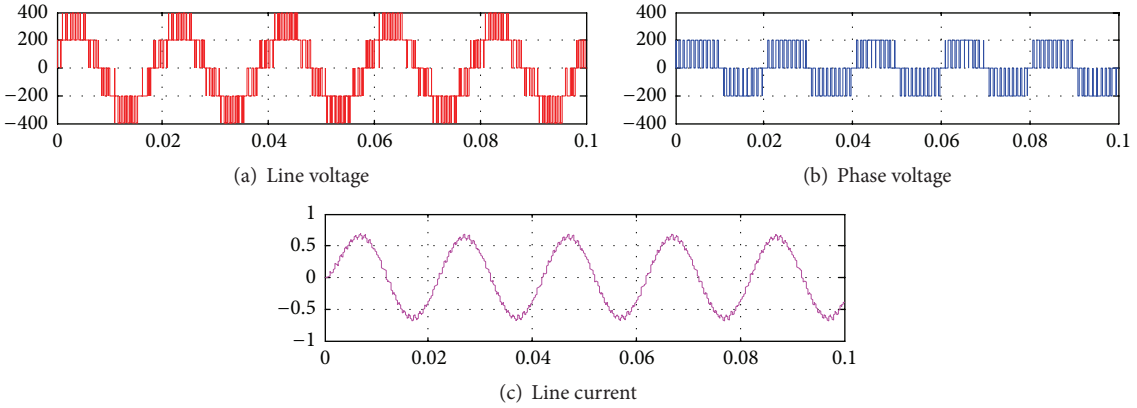
Figure 11: Conventional two-level inverter.



(a) Line voltage (b) Phase voltage

(c) Line current

Figure 12: Five-level inverter as three-level inverter.



(a) Line voltage (b) Phase voltage

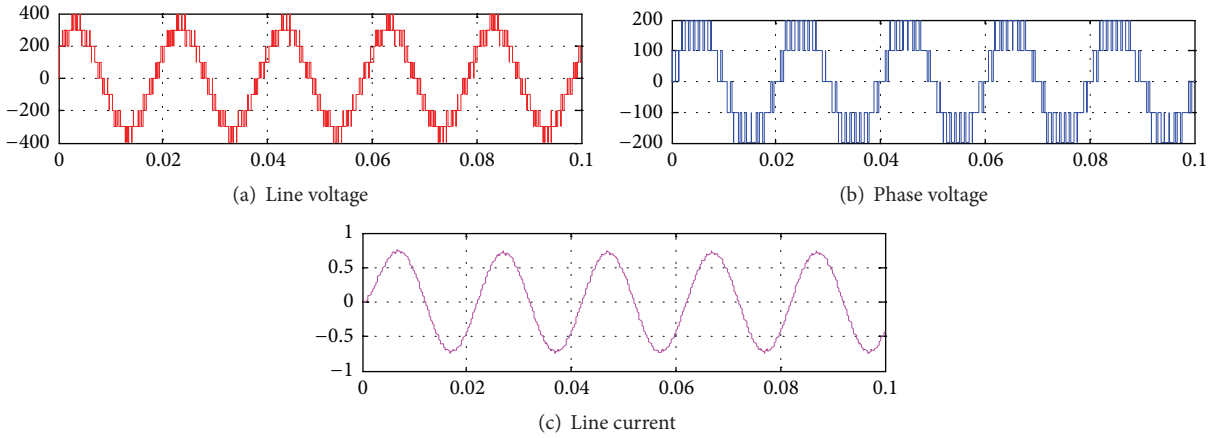
(c) Line current

Figure 13: Conventional three-level inverter.

with the results of conventional two- and three-level inverter. It is possible to obtain few lower level inverters from available MLIs. Results clearly validate the proposition.

As the level of inverter increases THD and common mode voltages also reduce. It is also observed that as the level increases THD of voltage and current decreases. CMV also reduces with the increasing level of the inverter. Due to increasing use of multilevel inverter in all fields this scheme is very much useful for the researcher as well as industrial application where different level operation is requirement. dsPIC33EP256MC202 microcontroller develops the compatible five-level pulses as that of DSP controller.

Using flexibility quotient one can forecast operation of available MLI to lower levels. The proposition kept confined to odd levels only, as CMV can be reduced to zero. Otherwise it may be applicable to even level inverter too.



(a) Line voltage

(b) Phase voltage

(c) Line current

Figure 14: Five-level inverter.

Competing Interests

The authors declare that they have no competing interests.

References

[1] M. M. Renge and H. M. Suryawanshi, "Multilevel inverter to reduce common mode voltage in AC motor drives using SPWM technique," *Journal of Power Electronics*, vol. 11, no. 1, pp. 21–27, 2011.

[2] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1598–1607, 2008.

[3] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[4] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol. 52, no. 2, pp. 1114–1128, 2011.

[5] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 242–249, 2000.

[6] Microchip Technology Inc, "16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, Op Amps and Advanced Analog, dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC 24EPXXXGP/MC20X," datasheet No. DS70000657H, 2011–2013.