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Research Article

Design Consideration for High Step-Up Nonisolated Multicellular dc-dc Converter for PV Micro Converters

Yusuke Hayashi, Yoshikatsu Matsugaki, and Tamotsu Ninomiya

Green Electronics Research Institute, Kitakyushu (GRIK), 1-8-409 Hibikino, Wakamatsu-ku, Kitakyushu, Fukuoka 808-0135, Japan

Correspondence should be addressed to Yusuke Hayashi; hayashi@grik.jp

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High step-up nonisolated multicellular dc-dc converter has been newly proposed for PV microconverters. The multicellular converter consists of the nonisolated step-up cell converters using bidirectional semiconductor switches, and these cell converters are connected in Input Parallel Output Series (IPOS). The voltage transformation ratio of the step-up converter is $N/(1-D)$ in case all the transistors in N cell converters are operated at the duty ratio of D. The proposed multicellular dc-dc converter also accomplishes high efficiency because of no magnetic coupling such as the high frequency transformer and the coupled inductor. Laboratory prototype has been fabricated to show the feasibility of the proposed converter. Design consideration for the 20 V–40 V to 384 V, 240 W nonisolated multicellular dc-dc converter has been also conducted, and the potential to achieve the efficiency of 98% has been shown. The proposed multicellular converter contributes to realizing the environmentally aware data centers for future low carbon society.

1. Introduction

Environmentally aware data centers have been proposed by NTT (Nippon Telegraph and Telephone Corporation) to realize highly electrified low carbon society [1, 2]. The environmentally aware data center reduces the conversion loss by introducing 380 V dc distribution system and minimizes the environmental impact by installing the solar PV power systems into the 380 V dc distribution system. Highly efficient and ultracompact (high-power-density) power electronics converters are necessary to utilize the renewable energy sources effectively.

Microconverter concept is one of attractive solutions for the effective use of the solar PV generations. The low input voltage and low output power dc-dc converter (microconverter) is installed into each solar module and all of microconverters are controlled to achieve MPPT (Maximum Power Point Tracking). Influence of the partially shaded or soiled solar cells on the total output power of the solar power systems is minimized because the output power of solar modules is controlled individually.

One of issues for the microconverter concept is the high step-up voltage transformation ratio (voltage gain: output voltage/input voltage) of 10–20. It is difficult to develop the high step-up microconverter by the general nonisolated boost chopper circuit because of the parasitic resistance [3]. High frequency transformers and coupled inductors based on the magnetic coupling are employed to accomplish the high step-up voltage transformation ratio [4–8]. The magnetic coupling achieves the high transformation ratio; however, this causes the nonnegligible power dissipation.

In this paper, the high step-up nonisolated dc-dc converter is newly proposed for PV microconverters. The proposed dc-dc converter is based on the multicellular converter topology, and the boost chopper circuits with the bidirectional switches for cell converters are connected in IPOS. The voltage gain is $N/(1-D)$ in case transistors in N cell converters are operated at the duty ratio of D. The number of cell converter contributes to achieving high transformation ratio.

In Section 2, the next generation dc distribution system for the data center is introduced. The circuit configuration, the control scheme, the fundamental behavior, and the feasibility of the nonisolated multicellular dc-dc converter are described in Section 3. In Section 4, design consideration for the proposed multicellular converter is

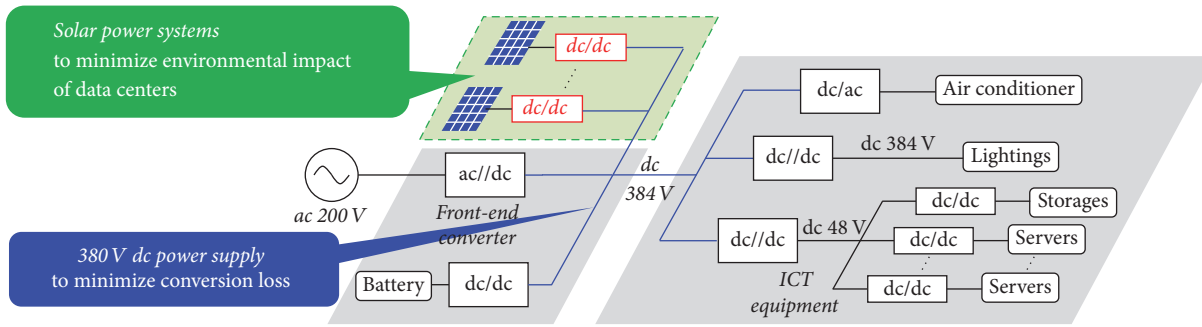

Figure 1: Configuration of next generation dc distribution system for environmentally aware data centers [9].

conducted and the potential to achieve high efficiency is presented.

2. Environmentally Aware Data Center for Low Carbon Society

2.1. Dc Distribution System in Environmentally Aware Data Center. The simplified schematic diagram of the dc distribution system for the environmentally friendly data centers is shown in Figure 1 [9, 13]. This system is based on the 380 V dc distribution system which goes beyond the conventional 48 V dc distribution system, and this achieves higher efficiency providing smaller supply current [14]. In the 380 V dc distribution system, the power factor correction (PFC) converters, the dc-dc transformers (DCX), and point-of-load (POL) converters are introduced to supply the electric power from ac 200 V to ICT (information and communication technology) equipment. Intensive studies have been conducted to realize highly efficient PFCs, DCXs, and POLs [15–18], and the potential to improve the total conversion efficiency in the dc distribution system from 80% to 94% has been discussed [9, 16].

In the dc distribution system for the environmentally aware data center, the environmental impact will be also minimized by installing the renewable energy sources such as solar PV power generations. The 380 V dc distribution system contributes smooth introduction of the solar power systems because of the dc interface. To utilize the generated electric power effectively, highly efficient and ultracompact dc-dc converters for PV generation are also indispensable.

2.2. Power Electronics Converters for PV Generation. There are mainly two solutions to connect PV cells to the dc distribution system via dc-dc converters. Figure 2 shows the schematic for two solutions. One is the centralized converter solution where low voltage PV modules are connected in series and the bundled higher voltage is applied to the single central converter. The other is the microconverter solution where the low-power dc-dc converters are placed beside PV modules and the output powers of PV modules are controlled independently. Characteristics of two solutions are summarized as follows.

(i) Highly efficient dc-dc converter can be developed in the centralized converter solution because of the low voltage transformation ratio. However, the generated electric power from PV cells is not provided to the distribution system effectively in case some solar modules are shaded or soiled.

(ii) Influence of the partially shaded or soiled solar modules on total generated electric power from PV cells can be minimized in the microconverter solution. The efficiency of the dc-dc converter in the microconverter solution is lower than the converter in the centralized solution because of the high voltage transformation ratio.

Microconverter solution is attractive for environmentally aware data centers in terms of the effective utilization of renewable energy sources. Developing highly efficient high step-up dc-dc converter is one of the key issues.

The voltage transformation ratio of, for example, 9.6 to 19.2, is required for the dc-dc converter in case the PV modules whose output voltages are, for example, 20 V to 40 V are connected to the 384 V dc distribution line. It is difficult to realize the general boost chopper circuit with the voltage transformation ratio over 10, because the parasitic resistance in the circuit causes the voltage drop [3]. Therefore, the circuit topologies based on the magnetic coupling such as the high frequency transformer and the coupled inductor are employed to realize the high voltage gain converters [4–8]. The magnetic coupling causes the significant power dissipation and prevents achieving high efficiency.

3. High Step-Up Nonisolated Multicellular dc-dc Converter

3.1. Circuit Configuration and Control System of Nonisolated Multicellular Converter. The nonisolated multicellular dc-dc converter is proposed to realize highly efficient high step-up dc-dc converter. Figure 3 shows the circuit configuration of the proposed converter. The multicellular converter consists of the nonisolated cell converters and these cell converters are connected in IPOS. Configuration of each cell converter is based on the general boost chopper circuit and the bidirectional switches substitute for the free-wheeling diode to achieve the isolation barrier. The bidirectional switches affect the converter performance significantly, and the ultralow loss GaN bidirectional transistors under the research

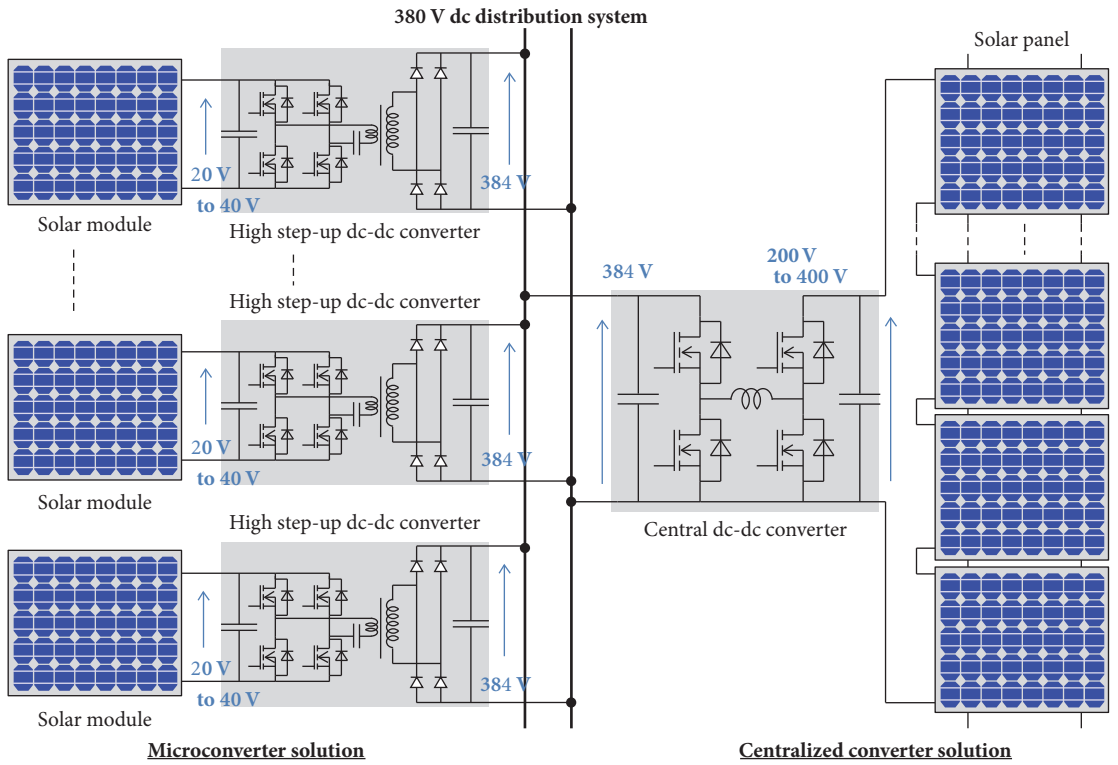

Figure 2: Centralized converter solution and microconverter solution for connecting PV modules into dc distribution system.

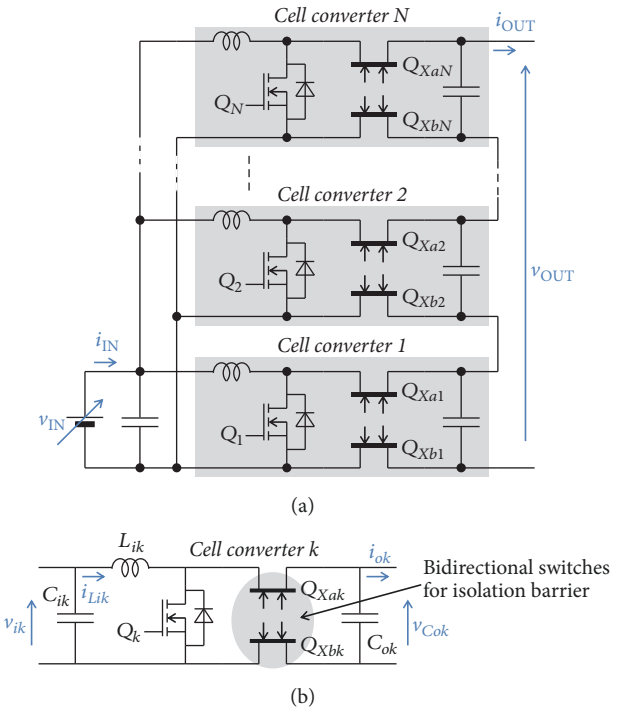

Figure 3: Configuration of high step-up non-isolated multicellular dc-dc converter. (a) IPOS connected cell converters and (b) single cell converter.

and development are attractive for the proposed converter [19].

Figure 4 shows the control system of the proposed multicellular dc-dc converter for the microconverter solution. The control system consists of the controller for the MPPT (Maximum Power Point Tracking) to adjust the duty ratio D and the controller for PWM (Pulse Width Modulation) to generate the gate signals for transistors Q_k $(k = 1, 2, \ldots, N)$ in the cell converters. The flowchart for the well-known P & O (Perturbation and Observation) algorithm is shown in Figure 4(a) and this control algorithm is generally applied to the boost converter for PV applications [10, 11, 20].

The isolated dc-dc converter with the high frequency transformers is often used to develop the IPOS multicellular converter. On the other hand, the proposed converter consists of the nonisolated dc-dc cell converters to simplify the circuit configuration. The isolation barrier has to be achieved by the intrinsic capacitances of the bidirectional switches Q_{Xak}, Q_{Xbk} $(k = 1, 2, \ldots, N)$, taking the control strategy into account. The gate signals for transistors Q_k during one cycle are shown in Figure 4(b). The duty ratio for all the transistors Q_k is D, and the bidirectional switches Q_{Xak}, Q_{Xbk} are operated complementally. In the proposed circuit, one of cell converters can provide the electric power to the load at an arbitrary time, and the remaining $N-1$ cell converters have to be isolated by turning off the bidirectional switches to prevent the short circuit among cell converters. The interleaved

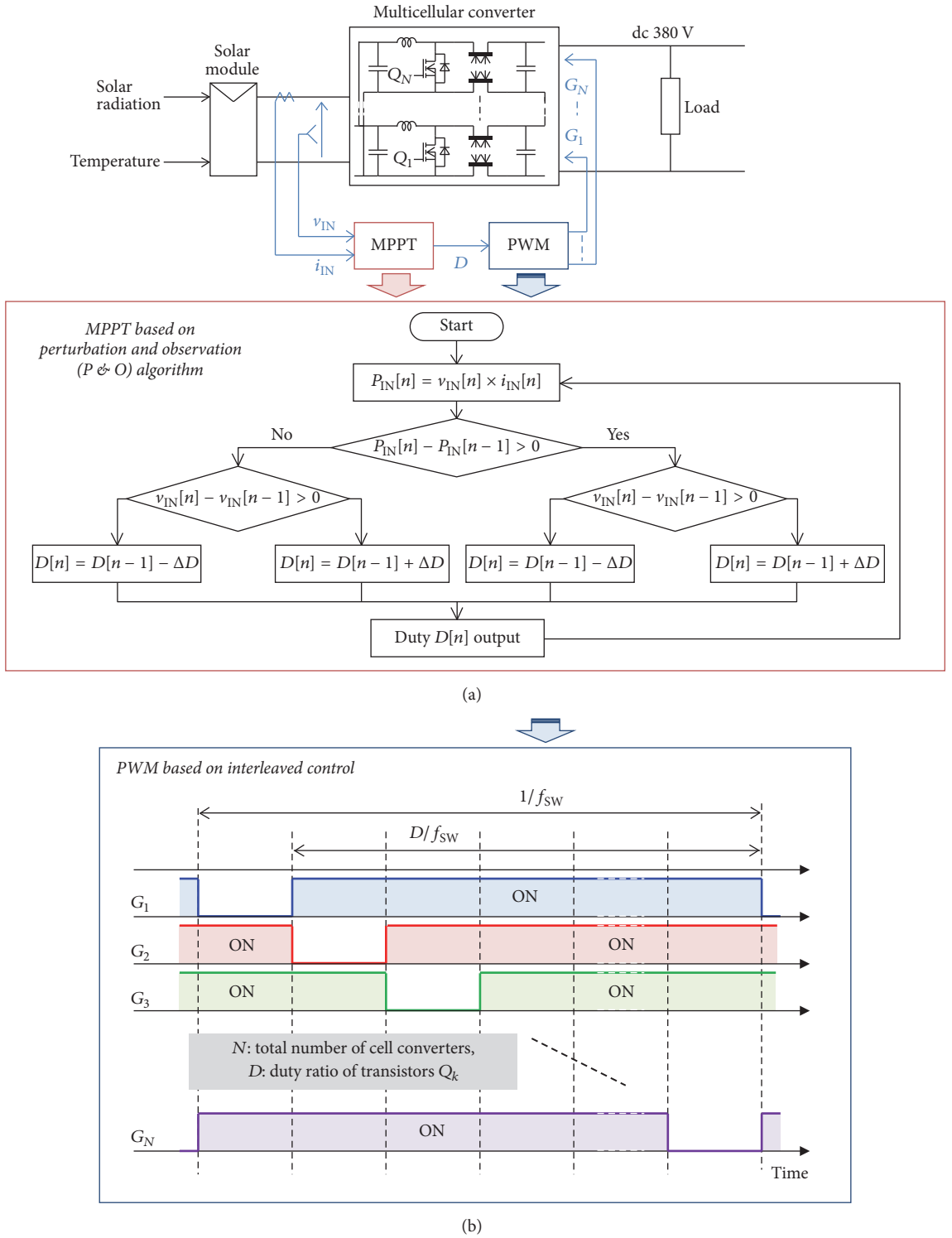

FIGURE 4: Control system of nonisolated multicellular converter for microconverter solution. (a) Control algorithm for MPPT and (b) PWM control.

control is applied to control the cell converters, and the duty ratio is limited as follows.

$$\frac{N-1}{N} \leq D \leq 1. \quad (1)$$

All the cell converters operating at the duty ratio in (1) behave as the general boost choppers independently, and the whole multicellular converter achieves high voltage gain realizing the isolation barrier among cell converters. Details of the converter characteristics are described in the next section.

3.2. Analysis for Nonisolated Multicellular Converter Based on Space-State Averaging Method. The circuit configuration of the cell converter is based on the typical boost chopper topology, and the fundamental characteristics of the proposed converter are explained by the space-state averaging method [3, 12, 21]. The transfer characteristics of each cell converter shown in Figure 3(b) are formulated as follows.

$$\frac{d}{dt}\begin{bmatrix} i_{Lik} \\ v_{Cok} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-D'}{L_{ik}} \\ \dfrac{D'}{C_{ok}} & \dfrac{-1}{RC_{ok}} \end{bmatrix} \begin{bmatrix} i_{Lik} \\ v_{Cok} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_{ik}} \\ 0 \end{bmatrix} v_{ik}. \quad (2)$$

In the above equation, the spate variables of i_{Lik}, v_{Cok} mean the current through the input inductor L_{ik} and the applied voltage to the output capacitor C_{ok}, respectively. The input voltage of the cell converter k is v_{ik} and its output current to the resistive load R is i_{ok}. The transistor Q_k is operated at the duty ratio of D ($D' = 1-D$). Here the integer k ($k = 1, 2, \ldots, N$) means the number of IPOS connected N cell converters in Figure 3(a). Parasitic resistances in the switches Q_k, Q_{Xak}, Q_{Xbk}, the inductor L_{ik}, and the capacitor C_{ok} are not considered here to simplify the analysis.

In Figure 3, the input voltage v_{IN} is applied to all cell converters and the output current i_{OUT} flows through all cell converters. In the IPOS connection topology, the following relationships are obtained.

$$\begin{aligned} v_{\mathrm{IN}} &= v_{i1} = v_{i2} = \cdots = v_{iN} \\ i_{\mathrm{IN}} &= i_{Li1} + i_{Li2} + \cdots + i_{LiN} \\ v_{\mathrm{OUT}} &= v_{Co1} + v_{Co2} + \cdots + v_{CoN} \\ i_{\mathrm{OUT}} &= i_{o1} = i_{o2} = \cdots = i_{oN}. \end{aligned} \quad (3)$$

In case that the common design methodology is applied to all cell converters, the equalized inductance and capacitance values are employed for all cell converters as follows, without taking the influence of the variation in the real products into account.

$$\begin{aligned} L_i &= L_{i1} = L_{i2} = \cdots = L_{iN} \\ C_o &= C_{o1} = C_{o2} = \cdots = C_{oN}. \end{aligned} \quad (4)$$

Based on the above relations, the transfer characteristics in (2) are summarized as follows.

$$\sum_{k=1}^{N} \frac{d}{dt}\begin{bmatrix} i_{Lik} \\ v_{Cok} \end{bmatrix} = \sum_{k=1}^{N} \begin{bmatrix} 0 & \dfrac{-D'}{L_i} \\ \dfrac{D'}{C_o} & \dfrac{-1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{Lik} \\ v_{Cok} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_i} \\ 0 \end{bmatrix} N v_{\mathrm{IN}} \quad (5)$$

$$\therefore \frac{d}{dt}\begin{bmatrix} i_{\mathrm{IN}} \\ v_{\mathrm{OUT}} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-D'}{L_i} \\ \dfrac{D'}{C_o} & \dfrac{-1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{\mathrm{IN}} \\ v_{\mathrm{OUT}} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_i} \\ 0 \end{bmatrix} N v_{\mathrm{IN}}. \quad (6)$$

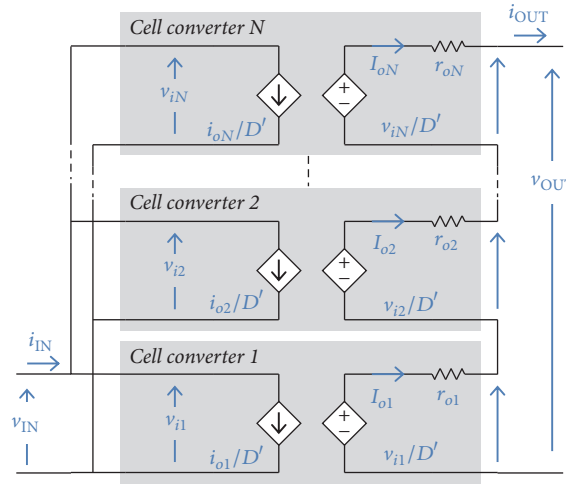

FIGURE 5: Simplified equivalent circuit of multicellular dc-dc converter based on IPOS connection topology.

Equation (6) means that the multicellular converter in Figure 3(a) behaves as the single step-up converter whose input voltage is $N \cdot v_{\mathrm{IN}}$. The relationship between the input voltage V_{IN} and the output voltage V_{OUT} of the multicellular converter is described as follows through the Laplace transformation.

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{N}{D'} \frac{1}{1 + (2\delta/\omega_0)\, s + (1/\omega_0^2)\, s^2} \quad (7)$$

$$\begin{aligned} \omega_0 &= \frac{D'}{\sqrt{L_i C_o}}, \\ \delta &= \frac{1}{2D'R}\sqrt{\frac{L}{C}} \end{aligned} \quad (8)$$

$$\lim_{s \to 0} s \cdot V_{\mathrm{OUT}} = \frac{N}{D'} \cdot V_{\mathrm{IN}}. \quad (9)$$

Equation (9) shows the voltage transformation ratio of the proposed multicellular converter under the steady state operation condition. The cycle of the output perturbation for the photovoltaics is generally at a level of several minutes. The high frequency converters achieve high-speed response and the converters accomplish the ratio in (9) during the perturbation. The obtained transformation ratio is N times higher than the ratio of the conventional step-up converter under the corresponding duty ratio D.

3.3. Output Voltage Unbalance among IPOS Connected Cell Converters. In the real circuit operation condition, the parasitic resistances in switches Q_k, Q_{Xak}, Q_{Xbk}, the inductors L_{ik}, and the capacitors C_{ok} cause the output voltage unbalance among cell converters. The influence of the parasitic resistances on the unbalanced voltage is discussed here.

The equivalent circuit of the multicellular step-up converter is shown in Figure 5. The cell converters can be regarded as the dc voltage transformer from (9), and the cell converter k ($k = 1, 2, \ldots, N$) is simply composed of the dependent voltage source, the dependent current source, and

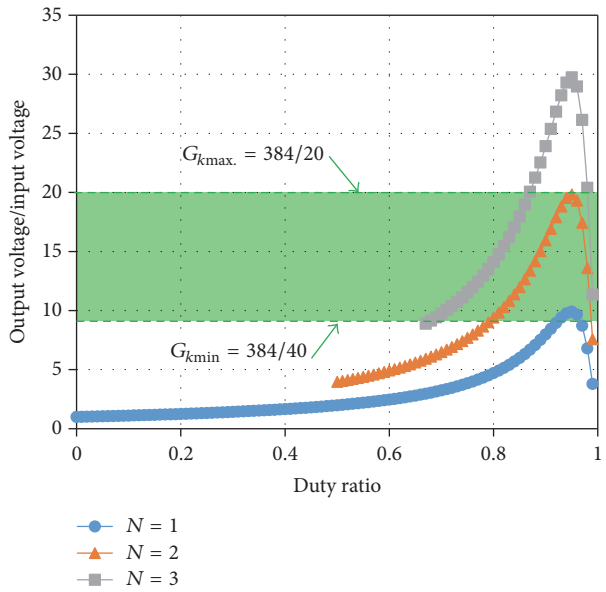

FIGURE 6: Voltage transformation ratio of nonisolated step-up multicellular dc-dc converter taking parasitic resistances into account.

the equivalent output resistance r_{ok} [18, 22]. The parasitic resistances caused by the switches and the inductors are bundled to the resistance r_{ok}. From Figure 5, the voltage and the current in each cell converter have the following relationship.

$$\frac{1}{D'}v_{ik} - r_{ok}\cdot i_{ok} = v_{ok}. \tag{10}$$

Based on (3), the output voltage v_{ok} of the cell converter k is obtained as follows.

$$\frac{N}{D'}v_{\mathrm{IN}} - \sum_{k=1}^{N} r_{ok}\cdot i_{\mathrm{OUT}} = v_{\mathrm{OUT}} = N\cdot R\cdot i_{\mathrm{OUT}} \tag{11}$$

$$i_{\mathrm{OUT}} = \frac{1}{D'}\frac{1}{R + \left(\sum_{k=1}^{N} r_{ok}\right)/N}v_{\mathrm{IN}} \tag{12}$$

$$\begin{aligned}\therefore v_{ok} &= \frac{1}{D'}v_{\mathrm{IN}} - r_{ok}\cdot i_{\mathrm{OUT}} \\ &= \frac{1}{D'}\left(1 - \frac{r_{ok}}{R + \sum_{k=1}^{N} r_{ok}/N}\right)v_{\mathrm{IN}}.\end{aligned} \tag{13}$$

From (13), the output voltages of the cell converters have the unbalance caused by the variation in the equivalent output resistances r_{ok}. However, the influence of the resistance r_{ok} is negligible in the case of highly efficient cell converter because the load resistance R is sufficiently larger than the resistance r_{ok}. This means that the output cell voltages v_{ok} converge, and the unbalanced voltage among cell converters is negligible in case all the cell converters are operated at the duty ratio D.

3.4. Voltage Transformation Ratio of Nonisolated Multicellular Converter under Real Circuit Operation Condition. Figure 6 shows the relationship between the duty ratio D of the transistor Q_k ($k = 1, 2, \ldots, N$) and the actual voltage transformation ratio G of the proposed multicellular converter, taking the parasitic resistances in the cell converters into account. As the duty ratio approaches 1.0, the transformation ratio diminishes because of the voltage drop caused by the parasitic resistances.

The calculation results of the voltage transformation ratio for three kinds of multicellular converter ($N = 1, 2, 3$ in Figure 3(a)) are shown in Figure 6. The transformation ratio G is calculated as follows based on (11) and (12).

$$v_{\mathrm{OUT}} = N\cdot R\cdot i_{\mathrm{OUT}} = \frac{N}{D'}\frac{R}{\left(R + \sum_{k=1}^{N} r_{ok}/N\right)}v_{\mathrm{IN}} \tag{14}$$

$$\begin{aligned}\therefore G = \frac{v_{\mathrm{OUT}}}{v_{\mathrm{IN}}} &= \frac{N}{D'}\frac{1}{\left(1 + \left(\sum_{k=1}^{N} r_{ok}/N\right)/R\right)} \\ &= \frac{N}{D'}\frac{1}{(1 + Z_o/R)}.\end{aligned} \tag{15}$$

In (15), the symbol of R means the output resistance based on the rated output power of the cell converter. The average parasitic resistance of all the cell converters is Z_o. The voltage gain G of the IPOS multicellular converter is simply calculated by stacking the voltage gains of the cell converters without taking the variation in the real product into account. In the steady state averaging method, the average resistance Z_o is formulated by using the resistance r_s from the main switch Q_k, the resistance r_D from the bidirectional switches Q_{xak}, Q_{xbk}, and the resistance r_L from the input inductor L_{ik} as follows [3].

$$Z_o = \frac{Dr_s + (1-D)r_D + r_L}{(1-D)^2} \cong \frac{r_L}{(1-D)^2}. \tag{16}$$

In (16), the resistances in the cell converter are bundled to r_L to simplify the calculation. Here, the parasitic resistance r_L of 0.5 Ω and the output resistance R of 205 Ω were applied to calculate the voltage transformation ratio, assuming the cell converter with the output voltage of 128 V (=384 V/3) and the output power of 80 W (240 W/3).

Figure 6 means that the nonisolated multicellular converter using 3 cell converters achieves the voltage transformation ratio of 9.6 to 19.2 for the PV microconverter.

4. Simulation Analysis and Experimental Verification of Nonisolated Multicellular Converter

4.1. Simulation Analysis for 20 V–40 V to 384 V Multicellular dc-dc Converter Using Three Nonisolated Cell Converters. Figure 7 shows the circuit configuration of the nonisolated multicellular dc-dc converter for circuit simulation analysis. Two antiseries connected power transistors Q_{Xak}, Q_{Xbk} in Figure 7 substituted for the single bidirectional switch shown in Figure 3 because of the research and development phase and no circuit simulation models for the single bidirectional switch.

Table 1 shows the parameters for the simulation. The input voltage of the multicellular converter V_{in} is from 20 V

Table 1: Parameters for circuit simulation of nonisolated multicellular converter.

Multicellular converter	
Input voltage V_{IN}	20 V to 40 V
Output voltage V_{OUT}	384 V
Output power P_{OUT}	240 W
Connection topology	Input Parallel Output Series
Number of cells	3 ($k = 1, 2, 3$)
Single cell converter	
Input voltage V_{IN}	20 V to 40 V
Output voltage V_{ok}	128 V
Output power P_{ok}	80 W
Transistor Q_k	GaN-FET (50 mΩ, 200 V) C_{oss} = 110 pF @ 100 V
Bidirectional switches Q_{Xak}, Q_{Xbk}	Two GaN-HEMTs (150 mΩ, 600 V) C_{oss} = 145 pF @ 100 V connected in antiseries
Input capacitor C_{ik}	MLCC (52.3 μF, 63 V)
Output capacitor C_{ok}	MLCC (1.37 μF, 200 V)
Input inductor L_{ik}	Mn-Zn ferrite (68.8 μH)
Switching frequency f_{SW}	100 kHz
Parasitic inductance	22.5 nH

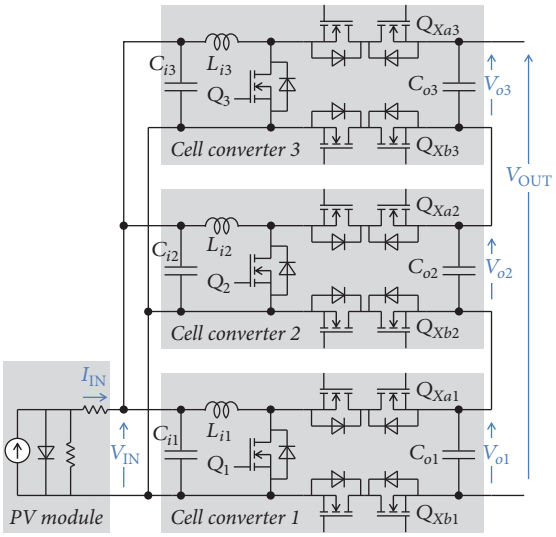

Figure 7: Circuit configuration of non-isolated multicellular dc-dc converter using three cell converters for circuit simulation.

to 40 V, taking the output perturbation of the PV module into account [4–7]. The output voltage of the multicellular converter V_{out} is nominally 384 V to connect to the 380 V dc distribution system. The rated output power of the converter P_{out} is 240 W here. The output voltage of the cell converter V_{ok} is nominally 128 V and the output power of the cell converter P_{ok} is 80 W because of three cell converters. The GaN-FET (50 mΩ, 200 V) was utilized for the main transistor Q_k and the GaN-HEMTs (150 m Ω, 650 V) were employed for the bidirectional switches Q_{Xak}, Q_{Xbk} in each cell converter. The multilayer ceramic capacitors (MLCCs) were utilized for both the input and the output capacitors C_{ik}, C_{ok}.

The capacitances C_{ik}, C_{ok} were designed to suppress the voltage ripple of the input and the output voltages within 3% of their rated voltages, respectively. The input inductance L_{ik} was designed to achieve the zero current switching (ZCS) under the critical current mode (CCM) of the boost chopper cell converter at the input voltage of 40 V and the output power of 80 W. Here, the subscript k for the symbols means the number of the cell converters and k has the integer of 1, 2, 3.

The output characteristics of the PV module are given by the published datasheet. Figure 8 shows the normalized I-V and P-V characteristics of the commercially available PV module, taking the influence of the solar radiation into account. The operation conditions to achieve the MPPT are extracted from Figure 8. In case the normalized voltage of 1.0 corresponds to 40 V and the normalized current of 1.0 means 8.0 A, the maximum output power of the PV module for the irradiation of 100% becomes 244 W under the condition that the voltage V_{IN} and the current I_{IN} are 33.2 V and 7.36 A, respectively. The maximum output power for the solar radiation of 60% becomes 140 W under the voltage V_{IN} of 32.0 V. Here, the effect of the temperature of the PV module on its I-V characteristics is not considered.

Figures 9(a) and 9(b) show the simulation results of 32.0 V–384 V, 140 W operation and 33.4 V–384 V, 240 W operation, respectively. PSIM software was utilized for the simulation. The operation conditions in Figures 9(a) and 9(b) corresponded to the conditions which achieved the maximum power points MPP2, MPP1 under the irradiations of 60% and 100%, respectively, in Figure 8. In Figure 9(a), the transistors Q_k ($k = 1, 2, 3$) were operated at the duty ratio of 0.75 to boost the input voltage V_{IN} of 32.0 V to the output voltage of the cell converter V_{ok} of 128 V. The output voltage V_{out} of 384 V was obtained because three cell converters were connected in IPOS. In Figure 9(b), the duty ratio for transistors was 0.74.

The interleaved control was applied to the proposed multicellular converter to prevent the short circuit among cell converters. The off-states of the drain to source voltages V_{Q1}, V_{Q2}, V_{Q3} for transistors Q_1, Q_2, Q_3 appeared alternately, and this meant that the electric power was provided from one cell converter to the load at an arbitrary time.

The interleaved control enables shrinking the input inductor. The input inductors L_{ik} were designed to achieve CCM at the input voltage of 40 V and the inductor currents I_{Lik} have large ripple for the average current as shown in Figure 9. These ripples caused by the inductor currents I_{Lik} were bundled and canceled at the input side and the reduced ripple was confirmed in the input current I_{IN}.

The applied voltages to the bidirectional switches Q_{Xak}, Q_{Xbk} ($k = 1, 2, 3$) were also shown in Figure 9. The bidirectional switches were utilized for the isolation barrier. Maximum applied voltage to the switches Q_{Xak}, Q_{Xbk} corresponded to the output voltage V_{out}, and the applied voltages varied for the switching conditions of transistors Q_k.

The applied voltages to the transistors and the bidirectional switches have overshoots. The voltage overshoots

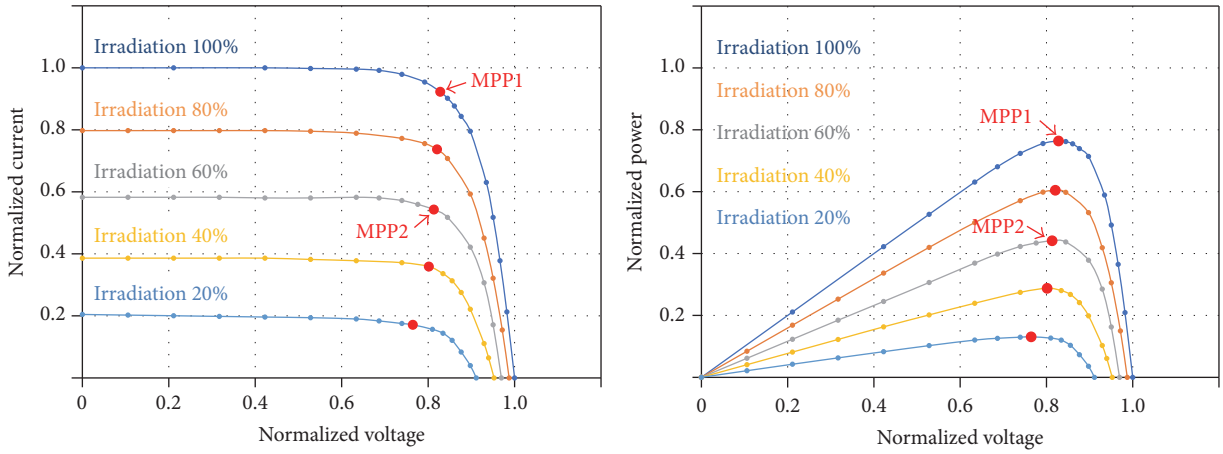

Figure 8: I-V and P-V characteristics of PV module.

Table 2: Parameters for experiment.

Multicellular converter	
Nominal input voltage V_{IN}	12 V
Nominal output voltage V_{OUT}	53 V
Resistive load R_{OUT}	20 Ω
Connection topology	Input Parallel Output Series
Number of cells N	2 ($k = 1, 2$)
Voltage gain G	4.44
Single cell converter	
Input voltage V_{ik}	12 V
Output voltage V_{ok}	26.6 V
Duty ratio D	0.55
Voltage gain G_k	2.22
Switching frequency f_{SW}	100 kHz
Main transistor Q_k	100 V, 2.8 mΩ (IRF7769 from IR)
Input inductor L_{ik}	10 μH
Output capacitor C_{ok}	44 μF

depend on the intrinsic and parasitic parameters caused by the circuit dimensions and the device structures. In this simulation, the 110 pF for GaN-FETs, 145 pF for GaN-HEMTs and 22.5 nH for the circuit parasitic inductances were considered in each cell converter.

4.2. First Laboratory Prototype of Nonisolated Multicellular Converter Using Two Cell Converters. The feasibility of the nonisolated multicellular dc-dc converter is verified in this section. Figure 10 shows the circuit configuration of the nonisolated multicellular converter for the experiment. This multicellular converter consists of two cell converters and these cell converters are connected in IPOS. The detailed circuit parameters are shown in Table 2. The nominal input voltage V_{IN} was 12 V and the input voltages of cell converters V_{i1}, V_{i2} corresponded to the input voltage V_{IN}. The voltage transformation ratio of cell converters G_k ($k = 1, 2$) was 2.22 because the duty ratio of the main switches Q_1, Q_2 was 0.55. The voltage gain G of the multicellular boost converter was 4.44 because the output terminals of two cell converters were connected in series.

In the experiment, Si-MOSFETs (100 V, 2.8 mΩ from IR) were employed for the main switches Q_1, Q_2. The body diodes of the Si-MOSFETs and the Si-SBD (Shottoky Barrier Diode) substituted for the bidirectional switches Q_{Xak}, Q_{Xbk} ($k = 1, 2$) shown in Figure 7 because the applied voltages to the switches Q_{Xak}, Q_{Xbk} were unidirectional in the case of the number of the cell converters N was 2.

Figures 11 and 12 show the experimental apparatus and the experimental result, respectively. The legends for the voltage waveforms $V_{IN}, V_{o1}, V_{o2}, V_{OUT}$ and the current waveforms I_{IN}, $I_{Li1}, I_{Li2}, I_{OUT}$ shown in Figure 12 corresponded to the legend in Figure 10. The voltages V_{Q1}, V_{Q2} in Figure 12 means the applied voltages to the main switches Q_1, Q_2.

In Figure 12, the input voltage V_{IN} was 11.1 V and the output voltages of cell converters V_{o1}, V_{o2} were approximately 24.8 V. The voltage transformation ratios of the cell converters G_1, G_2 were 2.23 (=24.8/11.1) and these ratios were nearly equal to the voltage gain of 2.22 in case the main switches Q_1, Q_2 were operated at the duty ratio of 0.55. The output voltage of the multicellular converter V_{OUT} resulted in 49.6 V because of the IPOS connection of two cell converters. The voltage transformation ratio G of 4.46 was confirmed under operating at the duty ratio of 0.55.

The inductor currents I_{Li1}, I_{Li2} had the current ripples of ±50% for the average inductor currents of 6.3 A. In the proposed converter, these current ripples were cancelled because the main switches in the cell converters were controlled alternately. The input and the output currents I_{IN}, I_{OUT} were 12.7 A and 2.6 A, respectively, and the current ripples for I_{IN}, I_{OUT} were suppressed. The off-state voltages of V_{Q1}, V_{Q2} were 24 V and corresponded to the input voltage V_{IN}. This means that the dc voltage between the input side and the output side was successfully blocked by the switches Q_{Xak}, Q_{Xbk} ($k = 1, 2$).

The fundamental circuit behavior of the proposed multicellular converter was confirmed here. The multicellular converter consisted of two cell converters because the unidirectional devices could be utilized in the case of N =

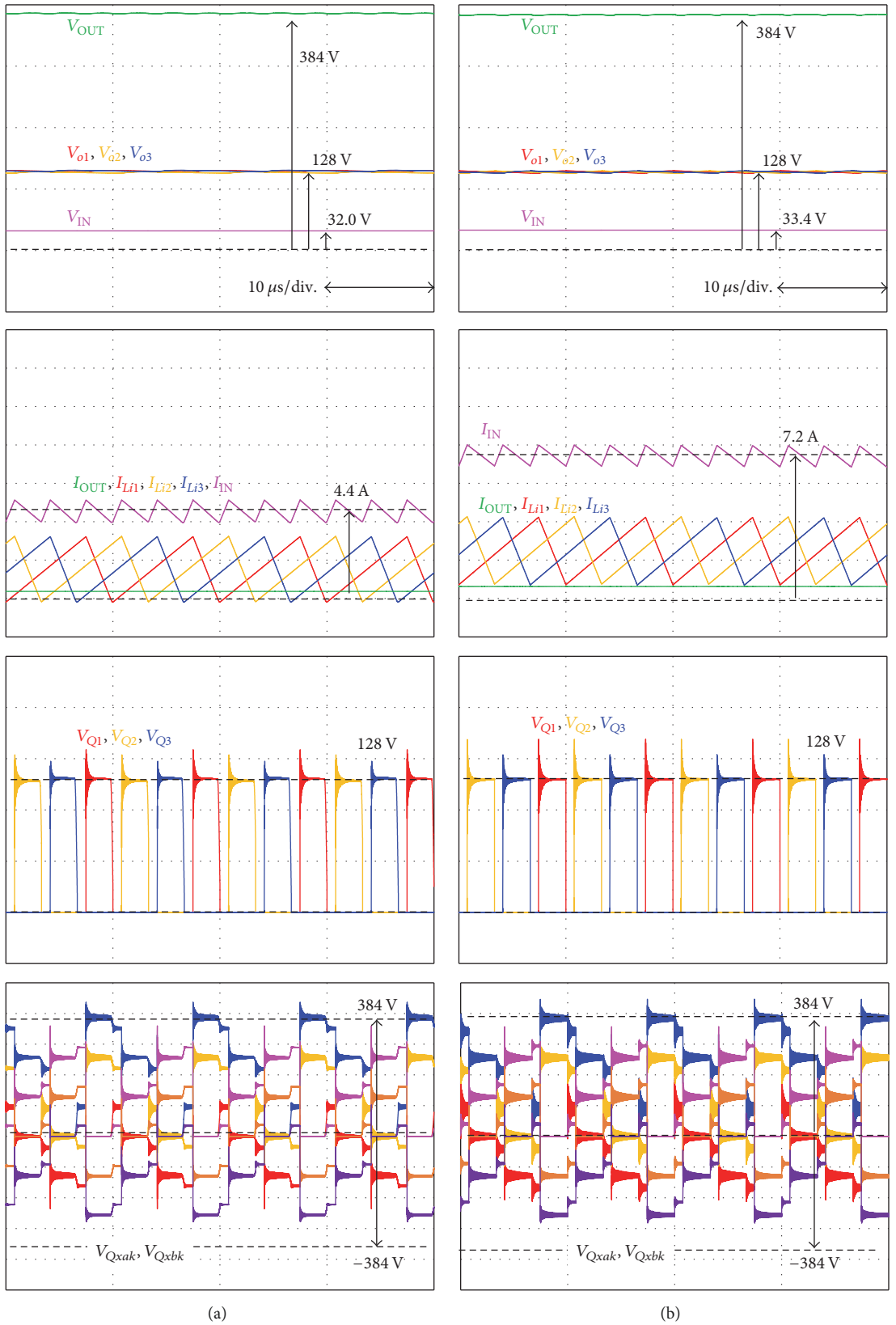

FIGURE 9: Simulation result for nonisolated multicellular dc-dc converter. (a) 32.0 V–384 V 140 W operation and (b) 33.4 V–384 V 240 W operation.

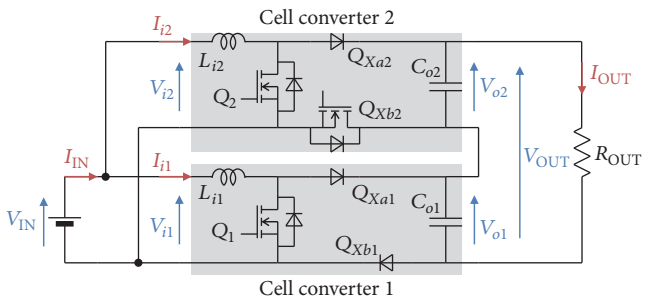

Figure 10: Circuit configuration of nonisolated multicellular boost converter for experiment.

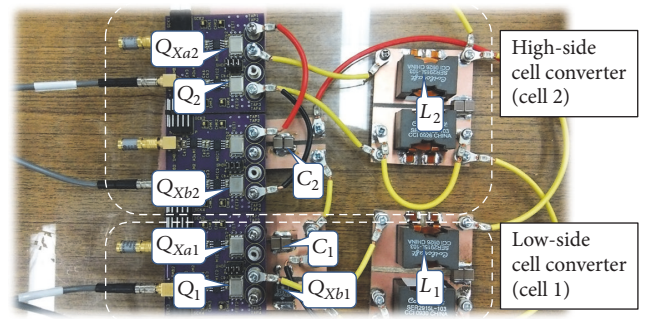

Figure 11: Experimental apparatus of nonisolated multicellular dc-dc converter using two cell converters connected in IPOS.

2. The employment of bidirectional switches enables to operate the multicellular converter with large number of cell converters as shown in the above simulation analysis.

5. Design Consideration for Nonisolated Multicellular dc-dc Converter

Design consideration for 20 V–40 V to 384 V, 240 W multicellular converter is conducted to show the possibility of the highly efficient PV microconverter. The circuit configuration corresponds to the schematic in Figure 7 and the parameters are based on Table 1. The power losses generated from the semiconductor power devices, the input inductors, and the capacitors are calculated to estimate the conversion efficiency, varying the switching frequency from 100 kHz to 1 MHz. Detailed calculation methods for the power losses are shown in the following sections.

5.1. Switching Loss Estimation Using Device Total Loss Simulator (DTLS). The power loss generated from the semiconductor power device consists of the conduction loss P_{cond} and the switching loss P_{sw}. In the proposed circuit, the cell converter is based on the boost chopper circuit topology, and the conduction loss of the transistor Q_k is simply calculated by the formula of $P_{\text{cond}} = D \cdot I_{Lik}^2$. The conduction losses generated from the bidirectional switches Q_{Xak}, Q_{Xbk} are also calculated in the same manner as the transistor Q_k.

The switching loss P_{sw} generated from Q_k is calculated by using the device total loss simulator (DTLS) [23, 24]. The DTLS was developed to estimate the switching loss

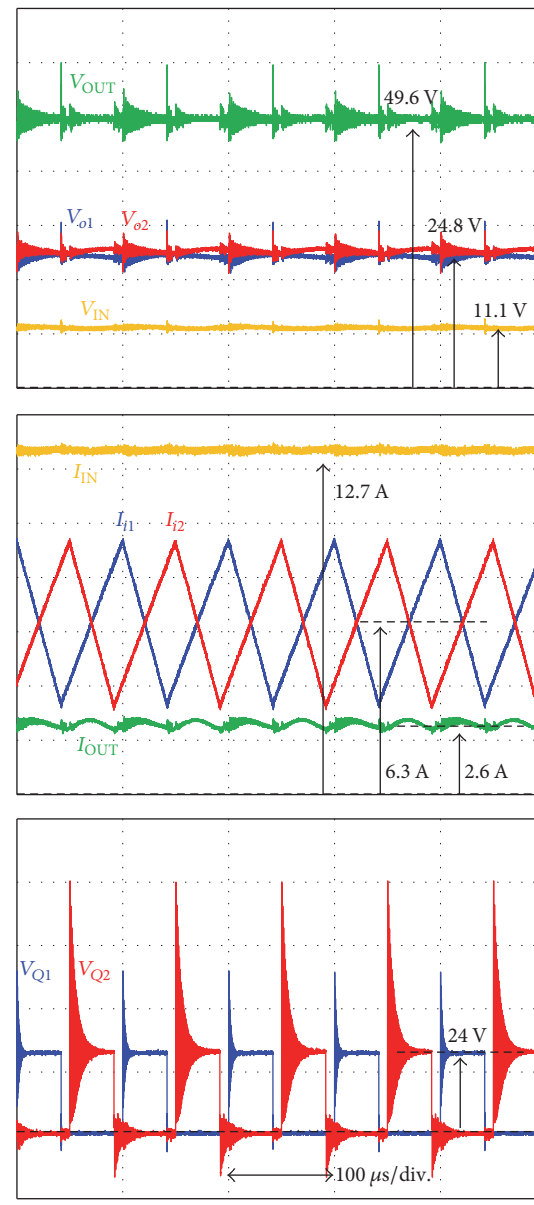

Figure 12: Experimental result for nonisolated multicellular boost converter using two cell converters.

energy exactly for high-speed and ultralow loss devices such as GaN transistors. Figure 13 shows the equivalent circuit to calculate the switching loss generated from Q_k, taking the nonlinear capacitances in power device and the circuit parasitic parameters into account. In Figure 13, the circuit parasitic inductances are L_{s1}, L_{s2}, L_{s3}, and L_{s4}, and these inductances are generally bundled to the equivalent inductor L_{st} ($=L_{s1} + L_{s2} + L_{s3} + L_{s4}$). The symbols of C_{sH} and C_{sL} mean the circuit parasitic capacitances. The gate resistance and the inductance are R_g and L_{sg}, respectively, and the common inductance which affects both the gate circuit and the main circuit is L_{sc}. Not only the device parameters but also the circuit parasitic parameters have to be designed in advance to estimate the exact switching loss.

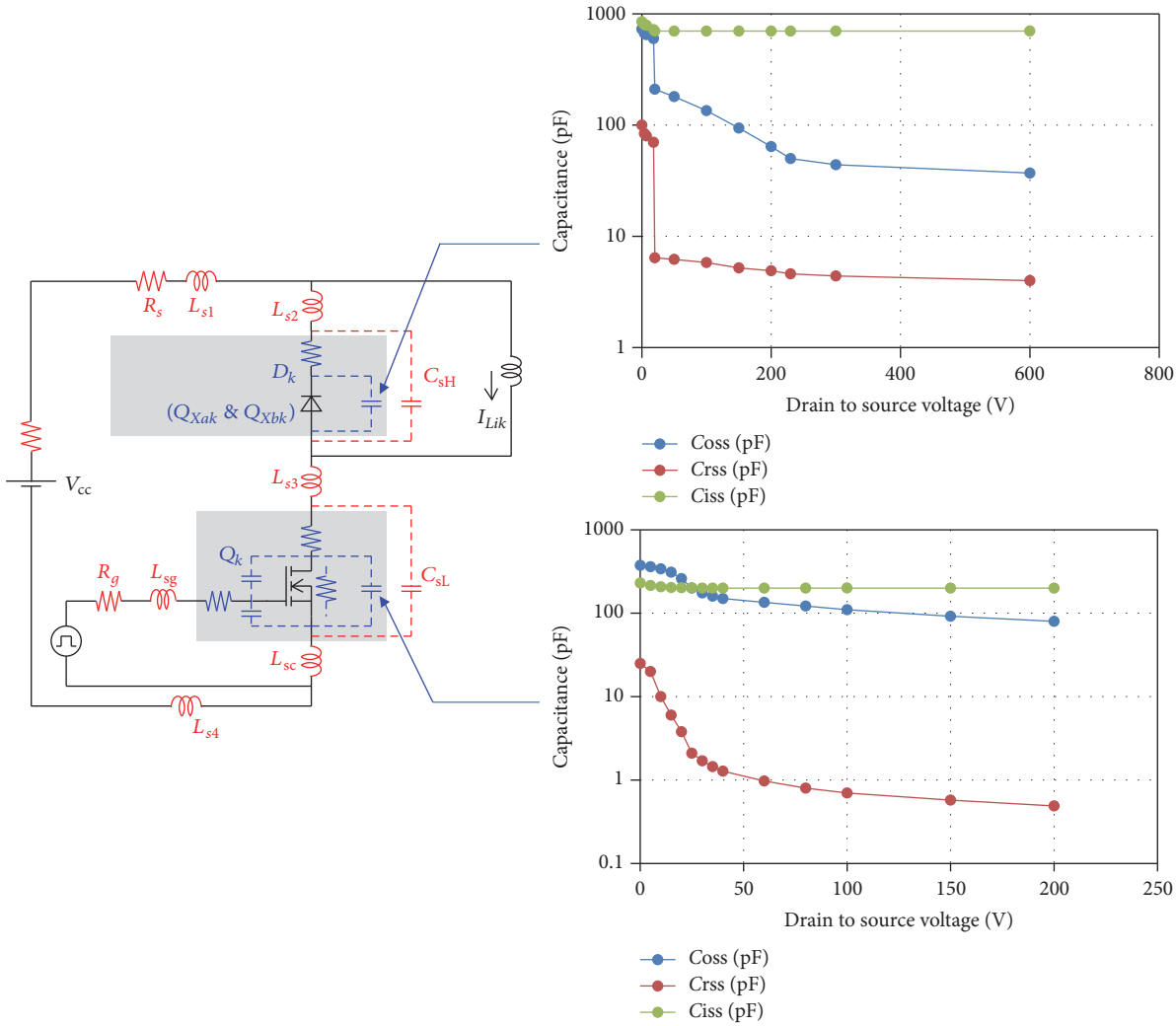

FIGURE 13: Equivalent circuit for switching loss energy calculation in device total loss simulator [10].

In DTLS, the turn-on energy E_{on} and the turn-off energy E_{off} generated from Q_k are calculated as follows.

$$E_{on} = \int i_d(t) \times v_{ds}(t)\, dt + \frac{1}{2} C_{Dk} V_{cc}^2 + \frac{1}{2} L_{st} I_{Lik}^2 \quad (17)$$

$$E_{off} = \int i_d(t) \times v_{ds}(t)\, dt + \frac{1}{2} C_{oss} V_{cc}^2. \quad (18)$$

The drain to source voltage v_{ds} and the drain current i_d of the transistor Q_k are basically calculated based on the numerical analysis, taking the nonlinearity of device capacitances into account. As shown in (17) and (18), a part of the switching loss energy is described by the stored energies in the circuit parasitic inductance and the device capacitances. The nonlinear analysis which causes the accumulated error is reduced to estimate the switching loss energies in DTLS.

To confirm the availability of DTLS, the switching loss energy of the GaN-HEMT (600 V, 150 mΩ) was measured here. Figure 14 shows the measurement setup and the measured turn-off waveforms for the drain current of 2 A to 12 A. The circuit parasitic inductance L_{st} of the setup was 22.5 nH and the gate resistance R_g of 3.0 Ω was connected externally in the experimental setup.

Both the measured switching loss energies of GaN-HEMT and the calculated energies by DTLS were compared in Figure 15. Detailed circuit parameters were shown in Table 3, and these parameters corresponded in the experimental condition in Figure 14. The circles filled in blue were the turn-on energies by the experiment and the circles filled in white were the measurement results of the turn-off energies in Figure 14. The blue solid line means the turn-on energy and the blue dashed line means the turn-off energy calculated by DTLS. The calculation results had good agreement with the experimental results. The validity for the commercially available 200 V class GaN-HFET has been already confirmed [23]; therefore, DTLS is available to estimate the switching loss of datasheet-level high-speed and ultralow loss power transistors exactly.

The switching loss energy from the GaN-FET (200 V, 50 mΩ) suitable for the cell converter was calculated and the calculation results were also shown in Figure 15. The solid and the dashed lines in green means the loss energies for

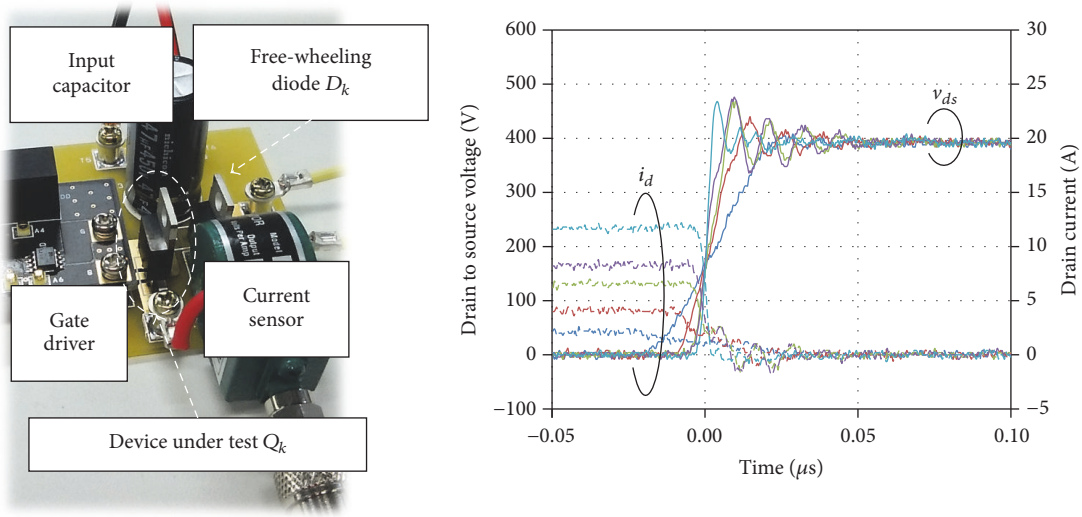

Figure 14: Measurement result of turn-off waveforms for 600 V 150 mΩ GaN-HEMT under 384 V, 2 A to 12 A operation conditions.

Table 3: Parameters for switching energy calculation.

Circuit parasitic parameters	
Total parasitic inductance L_{st}	22.5 nH
Parasitic capacitances C_{sH}, C_{sL}	10 pF, 30 pF
Common inductance L_{sc}	1 nH
Gate inductance L_{sg}	3 nH
Gate resistance R_g	3 Ω
GaN-HEMT Q_{Xak}, Q_{Xbk} for free-wheeling diode D_k	
On-resistance	150 mΩ
Output capacitance	110 pF @ 100 V
Breakdown voltage	600 V
GaN-FET Q_k	
On-resistance	50 mΩ
Output capacitance	110 pF @ 100 V
Breakdown voltage	200 V

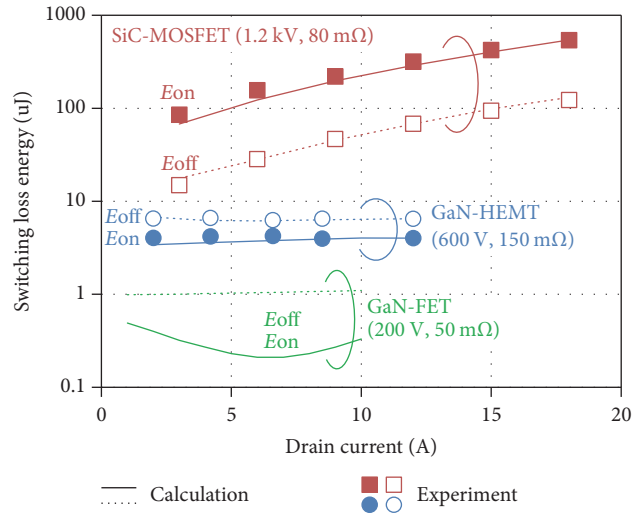

Figure 15: Turn-on and turn-off switching energies of GaN-FET in nonisolated multicellular converter calculated by DTLS.

the GaN-FET. The circuit parasitic parameters were based on Table 3 and the turn-on and the turn-off switching energies below 1 μJ are expected. The switching loss of GaN-FET for cell converter is calculated based on Figure 15, taking the turn-on and the turn-off currents obtained from the circuit simulation.

5.2. Input Inductor Design for Cell Converter. The power loss generated from the inductor consists of the copper loss P_{Cu} and the core loss P_{core}. The copper loss is generally calculated by the formula of $P_{Cu} = r_w(f_{sw}) \cdot I_{Lik}^2$. Here, r_w is the resistance of the inductor winding and the resistance r_w depends on the switching frequency f_{sw} of the converter because of the skin effect. Details to estimate the core loss is described below.

The input inductance of the cell converter L_{ik} is designed to achieve the CCM under the 40 V–128 V, 80 W operation to shrink the inductor here. The inductance value of 68.8 μH at the switching frequency of 100 kHz is obtained by the following equation.

$$V_{Lik} = L_{ik} \frac{\Delta I_{Lik}}{\Delta t}$$
$$L_{ik} = \frac{V_{in} \cdot D}{2 \cdot I_{Lik} \cdot f_{sw}} = \frac{40\,\text{V} \cdot 0.688}{2 \cdot 2\,\text{A} \cdot 100\,\text{kHz}} = 68.8\,\mu\text{H}. \quad (19)$$

The relationship between the inductance and the magnetic core shape is approximately formulated as follows.

$$L_{ik}\,(\text{H}) = \mu_0 \mu_r N^2 \frac{S_e\,(\text{m}^2)}{l_e\,(\text{m})} \quad (20)$$

$$\text{Vol}_{\text{core}}\,(\text{m}^3) \cong l_e \cdot S_e. \quad (21)$$

Table 4: Parameters for inductor design installed into cell converter.

Magnetic material	
Material	Mn-Zn ferrite
Permeability μ_r	2,300
Max. flux density B_m	0.5 T
Residual magnetization B_r	0.12 T
Coercivity H_c	14.3 A/m
Circuit specifications	
Switching frequency f_{sw}	100 kHz to 1 MHz
Inductance L_{ik}	68.8 μH to 6.88 μH
Magnetic core dimensions	
Core shape	PQ core
Width X	10 mm to 35 mm
Depth Y	6.7 mm to 23.4 mm
Height Z	8.6 mm to 30.2 mm
Gap length l_g	0 mm to 25 mm

Here, the permeability of vacuum is μ_0, and the relative permeability of the magnetic material is μ_r. The turn number of the inductor winding is N. The magnetic length and the cross section area of the magnetic core are l_e and S_e, respectively. The magnetic core volume $\mathrm{Vol}_{\mathrm{core}}$ is approximately calculated as (21). The core loss P_{core} is generally estimated as follows.

$$P_{\mathrm{core}}\,(\mathrm{W}) = f_{\mathrm{sw}}\,(\mathrm{Hz}) \cdot E_{\mathrm{core}}\left(\mathrm{J/m^3}\right) \cdot \mathrm{Vol}_{\mathrm{core}}\left(\mathrm{m^3}\right). \quad (22)$$

As shown in the above equation, the core loss depends on the dimensions of the magnetic core $\mathrm{Vol}_{\mathrm{core}}$. There are various solutions to realize the designated inductor L_{ik}. To extract the suitable core dimension to realize the compact and low loss inductor, design consideration for the inductor is necessary.

Table 4 shows the parameters for the input inductor design. The Mn-Zn ferrite with the permeability of 2,300 was assumed for the magnetic core material of the inductor [25]. This is based on the commercially available magnetic material. The maximum magnetic flux density B_m, residual magnetization B_r, and the coercivity H_c in Table 4 are extracted from the published datasheet. Figure 16 shows the core loss energy E_{core} of the magnetic core material.

The PQ core was also assumed for the dimensions of the magnetic core. The core width was varied from 10 mm to 35 mm to design the inductors which were operated at 100 kHz to 1 MHz. The core depth Y and the core height Z are proportion to the core width X, keeping the dimensions of existing PQ core shape. The magnetic length l_e and the cross section area of the core S_e are found by the dimensions X, Y, Z.

Figure 17 shows the calculation result of the efficiency and the power density of the inductor for 80 W cell converter. The power loss from the inductor and the inductor volume were translated to the efficiency and the power density to normalize the performance of the inductor. The copper loss P_{Cu} and the core loss P_{core} were considered to calculate the inductor loss, and the envelope volume determined by the core dimensions X, Y, Z was also taken into account for the inductor volume. The heat sink volume is not considered here.

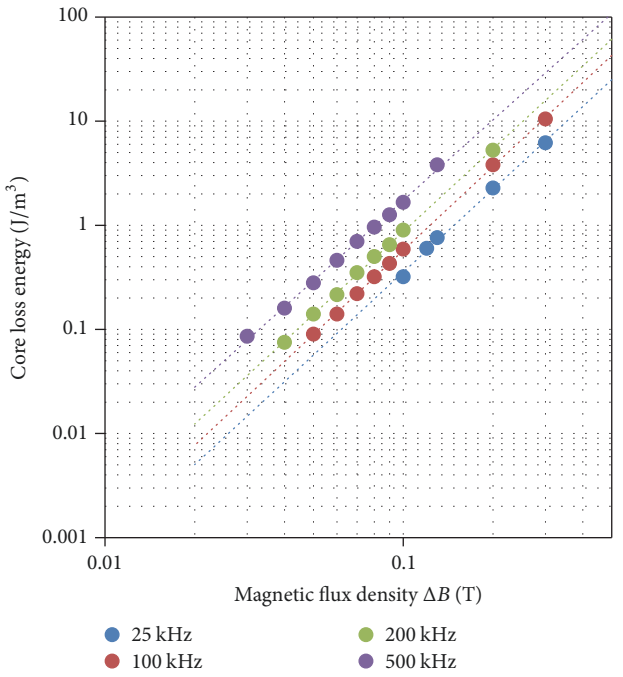

Figure 16: Core loss energy of magnetic core material [11].

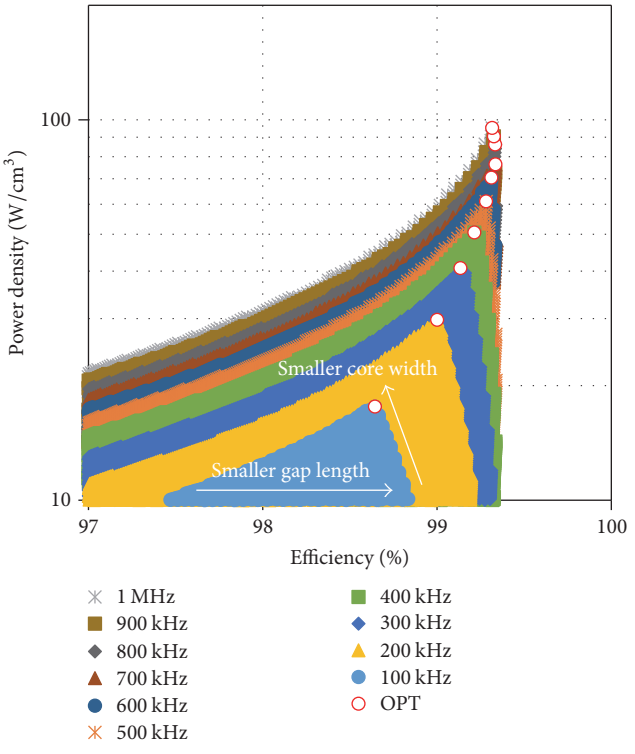

Figure 17: Calculated efficiency and power density of inductor.

As the gap length l_g becomes shorter, the inductor loss decreases. The material characteristics for the saturation determine the minimum gap length. As the core width X becomes shorter, the core volume shrinks. The turn number

of the inductor winding N increases, and the efficiency decreases because of the copper loss. Based on the aforementioned trend, the inductor has the operation condition to maximize its power density for each switching frequency. The symbol of OPT in Figure 17 means the conditions to achieve the highest power density for each frequency. The efficiency of the inductor at OPT is improved in case the switching frequency increases from 100 kHz to 700 kHz. The smaller inductance and the smaller core volume contribute to achieving higher efficiency. The core loss over 700 kHz operation affects the inductor loss significantly and the efficiency at OPT decreases. In this study, the operating condition to achieve the highest power density for each switching frequency is applied to the converter design.

5.3. Input and Output Capacitor Design for Cell Converter. The capacitance values for the input and the output capacitors C_{ik}, C_{ok} are designed to suppress the voltage ripples within 3% of the rated input and output voltages V_{in}, V_{ok}. The capacitances of 56.3 μF and 1.37 μF under 100 kHz operation are calculated as follows.

$$C_{ik} = \frac{I_{Lik} \cdot D}{\Delta V_{ik} \cdot f_{\text{sw}}} = \frac{4\,\text{A} \cdot 0.844}{0.03 \cdot 20\,\text{V} \cdot 100\,\text{kHz}} = 56.3\,\mu\text{F}$$
$$C_{ok} = \frac{I_{\text{out}} \cdot D}{\Delta V_{ok} \cdot f_{\text{sw}}} = \frac{0.625\,\text{A} \cdot 0.844}{0.03 \cdot 128\,\text{V} \cdot 100\,\text{kHz}} \quad (23)$$
$$= 1.37\,\mu\text{F}.$$

The multilayer ceramic capacitors (MLCC) are assumed to develop the input and the output capacitors to reduce the loss caused by the equivalent series resistance (ESR).

Figure 18 shows the relationship between the ESR and the capacitance value of the MLCC for the various rated voltages. The ESRs of the capacitors were obtained from the design tool provided by the manufacturer [26]. The ESRs were plotted for the capacitances of 0.1 μF to 100 μF whose rated voltages were 6.3 V to 1 kV. As the capacitance increases, the ESR decreases because the capacitor volume is generally proportional to the capacitance and the electrode area depends on the capacitance. The influence of the rated voltage of the capacitor on its ESR is not clear from Figure 18, and the capacitor loss caused by the ESR is calculated by using the fitted curve in this figure.

5.4. Efficiency Calculation for Cell Converter. Figure 19 shows the conversion efficiency of 32.0 V–128 V, 47 W cell converter in the case of the irradiation of 60% and the efficiency of 33.2 V–128 V, 80 W cell converter for the irradiation of 100%, taking the operation condition to achieve MPPT in Section 4. The conduction loss P_{cond} and the switching loss P_{sw} were considered for the transistor Q_k. The symbol of P_{sr} means the conduction loss generated from the bidirectional switch Q_{Xak}, Q_{Xbk}. The copper loss P_{Cu} and the core loss P_{core} were also considered for the inductor L_{ik}. The losses generated by ESR in the input and the output capacitors were P_{Ci}, P_{Co}.

From Figure 19, the maximum efficiency over 98.0% was expected for the 32.0 V–128 V converter under the 60% irradiation in case the switching frequency was smaller than

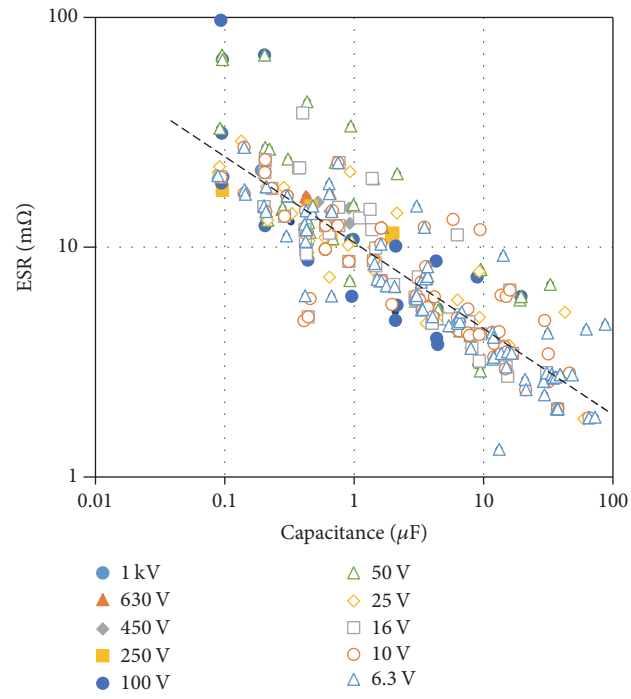

Figure 18: Equivalent series resistance of multilayer ceramic capacitor [12].

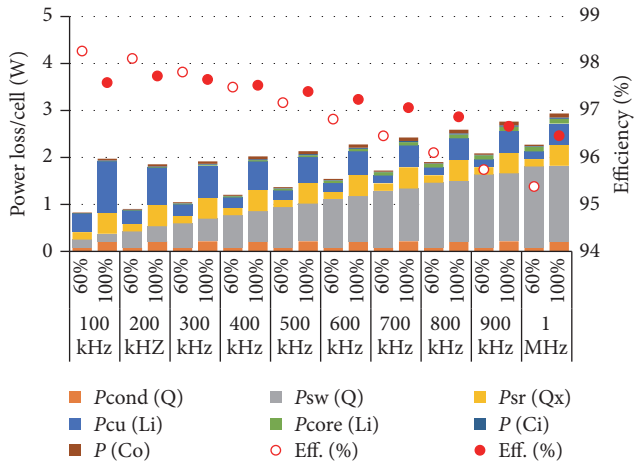

Figure 19: Calculated power loss and efficiency for cell converter. (a) 32.0 V–128 V, 47 W operation with 60% irradiation and (b) 33.2 V–128 V, 80 W operation with 100% radiation.

200 kHz. The switching loss from the power devices was dominant over 300 kHz. The maximum efficiency of 97.8% was also observed around 200 kHz for the 33.2 V–128 V cell converter with 100% irradiation.

The performance of the cell converter ideally corresponds to the performance of the multicellular converter [22]. Based on the multicellular converter topology, the maximum efficiency of 98% is expected to the nonisolated multicellular dc-dc converter. Now, the efficiencies of 93% to 97.5% have been reported for the microconverter [4–8]. This means that the proposed converter topology has the potential to achieve

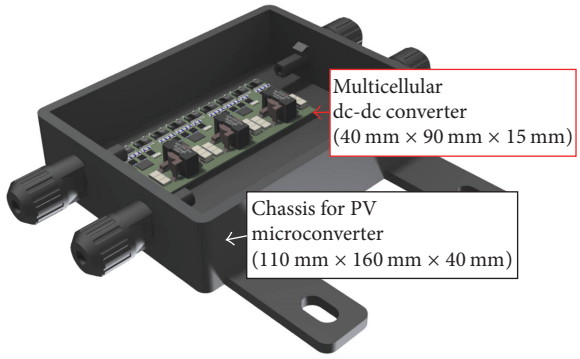

Figure 20: Illustration for PV microconverter based on multicellular converter topology.

higher efficiency and has the possibility to contribute to realizing low carbon society.

Figure 20 shows the illustration of the PV microconverter based on the proposed multicellular dc-dc converter. The electric components designed in the previous sections were arranged in the chassis for the microconverter. In Figure 20, the converter volume was small enough to house it into the chassis, taking the noise filter and microcontroller into account. The details of the thermal design, the noise analysis, and the experimental verification will be operated in near future.

6. Conclusions

High step-up nonisolated multicellular dc-dc converter was proposed to realize the highly efficient PV microconverter. The circuit configuration and the control scheme were introduced and the fundamental behavior of the proposed converter was also confirmed by the circuit simulation. Laboratory prototype using two cell converters was fabricated and the feasibility of the proposed multicellular converter was also confirmed. Design consideration for the 20 V–40 V to 384 V, 240 W multicellular converter was carried out and the potential to achieve the efficiency of 98% was observed.

Feasibility of the proposed converter topology using three cell converters with the bidirectional switches will be verified in near future. The detailed thermal design and the noise analysis will be also operated.

The proposed topology contributes to realizing the low carbon society through the smooth introduction of PV modules to dc distribution network.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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