

Research Article

New Low-Power Tristate Circuits in Positive Feedback Source-Coupled Logic

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Two new design techniques to implement tristate circuits in positive feedback source-coupled logic (PFSCl) have been proposed. The first one is a switch-based technique while the second is based on the concept of sleep transistor. Different tristate circuits based on both techniques have been developed and simulated using 0.18 μm CMOS technology parameters. A performance comparison indicates that the tristate PFSCl circuits based on sleep transistor technique are more power efficient and achieve the lowest power delay product in comparison to CMOS-based and the switch-based PFSCl circuits.

1. Introduction

Nowadays, due to the remarkable growth in portable consumer electronics, the demand for low power and high speed computing circuits is on the rise. High speed microprocessors are the key elements used for data processing in these devices. An increase in the processor speed leads to an excessive power dissipation in portable devices which use batteries as the power sources. So, it is necessary to explore design techniques that reduce power consumption in such systems at high operating speeds. At the circuit level, the traditional CMOS logic style fails to simultaneously satisfy the speed and power requirements of these applications [1] and a different logic style is required [2–8].

Among the possible topologies, PFSCl is the most suitable logic style for designing systems with optimum balance between speed and power dissipation [8–12]. A PFSCl style is derived from the single-ended source-coupled logic in which a positive feedback is introduced that significantly increases the speed as compared to traditional SCL circuits [8]. This improvement in speed can be traded off to reduce the power consumption of the circuits [9–11]. Thus, this logic style can be easily adopted in the design of high speed and high computing circuits for portable devices.

In this paper, PFSCl has been used to develop different tristate circuits that are extensively used in high speed

microprocessors and clock/data recovery systems to implement multiplexers, phase detectors, and buses [13, 14]. Two different design techniques have been used to implement tristate circuits in PFSCl. The first one is a switched based technique while the second one uses the concept of sleep transistor.

This paper is organized as follows. The architecture and the operation of PFSCl gates are described in Section 2. The design techniques to develop PFSCl-based tristate circuits are presented in Section 3. In the subsequent Section 4, the proposed tristate circuits are implemented and simulated using 0.18 μm CMOS technology parameters. Finally, the conclusions are drawn in the last section

2. PFSCl Circuits

The basic circuit of a PFSCl inverter is shown in Figure 1. It consists of a source-coupled nMOS transistor pair, M1-M2 biased by the constant current source, I_{ss} and a pMOS load transistor M3 [8–12]. The output of the gate is taken from the drain of pMOS active load, M3. A positive feedback is introduced in PFSCl by connecting the output of the gate to the input to transistor M2. This circuit works on the current steering principle. For a high input voltage V_{in} , the bias current I_{ss} is steered to M1 that produces a low

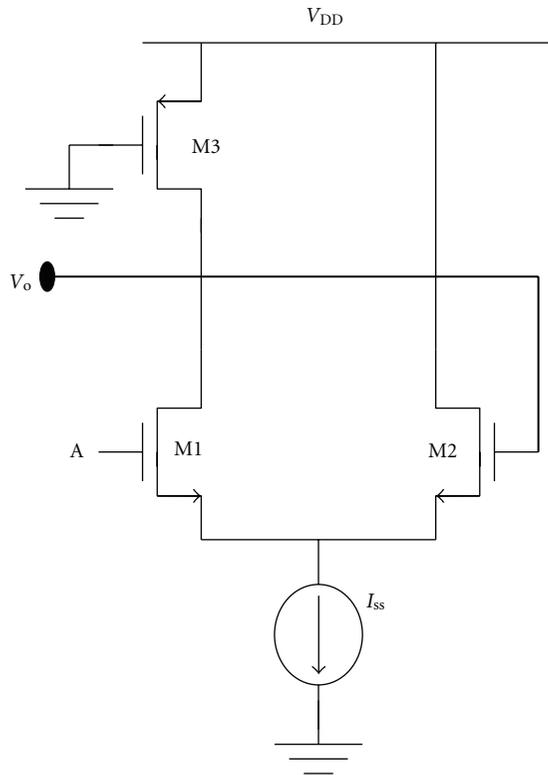


FIGURE 1: Basic PFSCl inverter/buffer.

output at the gate and at the same time makes the transistor M2 off. Similarly, a low input voltage V_{in} makes M1 off such that it gives a high gate output and turns M2 on. The positive feedback in these circuits reduces the aspect ratio of the nMOS transistor significantly in comparison to traditional single-ended SCL gates for similar values of design constraints. This results in reduced nMOS parasitic capacitances and allows significant speed improvement, which can be traded off to achieve a low power design [10].

Figure 2 shows different PFSCl-based basic gates, namely, NOR and NAND. The circuit for a NOR gate Figure 2(a) consists of two nMOS transistors M1 and M2, coupled to the current source I_{ss} along with the positive feedback transistor M3. When both or either of the two inputs A and B is high, M1 or M2 or both together conduct such that the bias current is steered through them and a low gate output is produced. The low gate output turns off transistor M3 through positive feedback. The (optional) pMOS transistor M5 is inserted to generate the complement of the output, and is substituted by a short circuit when it is not needed [9]. The above NOR gate topology has low transistor count as compared to source-coupled gates. The NOR gate topology can be extended to implement NAND gate by using De Morgan law and then taking the output from the drain of optional pMOS transistor (M5) [9] as shown in Figure 2(b).

3. Proposed PFSCl Tristate Circuits

A tristate gate is a type of logic gate that produces either high or low voltage level when enabled or have high impedance

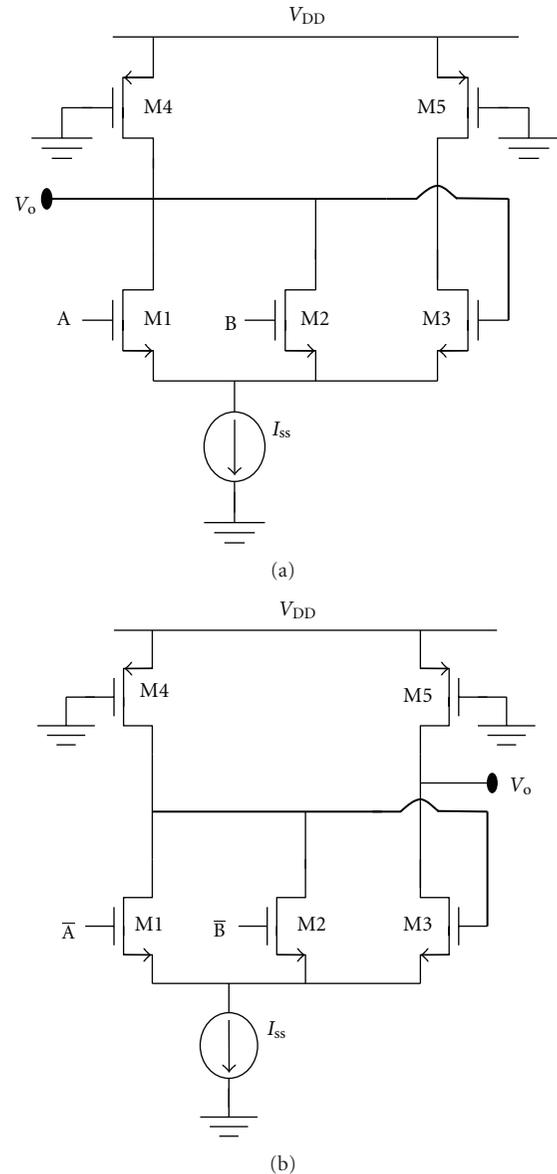


FIGURE 2: Different PFSCl gates; (a) 2-input NOR, (b) 2-input NAND.

state when disabled. A tristate buffer implemented in CMOS logic style [15] is shown in Figure 3. A high output level indicates that the output is sourcing current from the positive power terminal while a low output denotes the output is sinking current to the negative power terminal (or zero voltage). High impedance implies that the output is effectively disconnected from the circuit. These CMOS-based circuits are not efficient at high speeds. So two different techniques based on switch transistor and sleep transistor have been used to develop PFSCl tristate circuits for high speed operations.

3.1. Switch-Based PFSCl Tristate Circuits. In a basic PFSCl gate, there is a direct path from the outputs to the positive supply which cannot be turned off. That is why, it is necessary

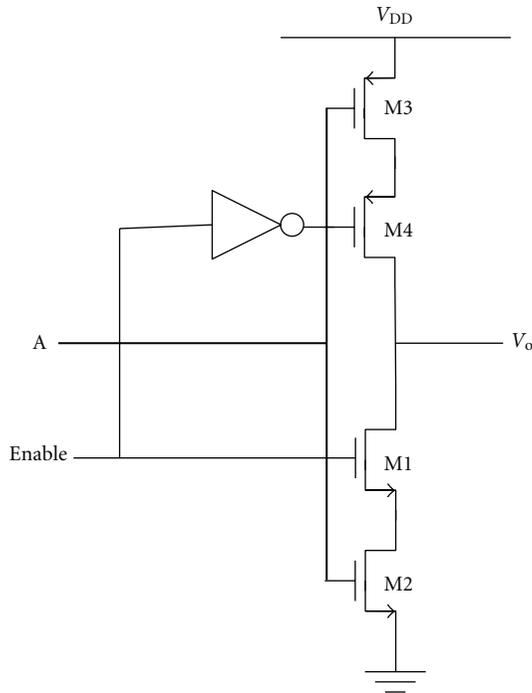


FIGURE 3: Tristate CMOS buffer.

to isolate the output from the power supply so as to produce a high impedance state for tristate logic. An effective way is to add a MOS transistor switch in series with the output node. The circuit for a tristate buffer/inverter is shown in Figure 4(a). The circuit consists of the basic PFSCl gate (M1–M4) and an additional pMOS switch (M5) connected in series with the output. The circuit behaves as a regular buffer/inverter for low value of Enable whereas its output is driven into high impedance for high Enable value. The circuit has the same static power dissipation as that of the basic PFSCl buffer/inverter. Similarly, the circuit diagrams of switch-based PFSCl NOR and NAND tristate circuits have been developed which is shown in Figures 4(b) and 4(c), respectively.

3.2. Sleep Transistor-Based PFSCl Circuits. In this technique, the basic concept of sleep transistor has been extended to obtain a low-power tristate PFSCl gate. The gate output has been isolated from the positive supply by inserting a sleep transistor [15] in series with the power supply of the circuit. The circuit diagram of a tristate PFSCl buffer/inverter is shown in Figure 5(a), wherein the source and gate of the sleep transistor, M5, is connected to power supply and the Enable input, respectively. The drain of M5 is connected to the basic PFSCl buffer/inverter such that it acts as a virtual supply voltage terminal. For low value of enable, the sleep transistor M5 is on so that power supply is connected to the PFSCl buffer/inverter and the circuit behaves as a regular buffer/inverter. For high voltage level, sleep transistor M5 is off and in turn disconnects the power supply so that no current flows in the circuit and high impedance state is produced at the output. In this case, the proposed

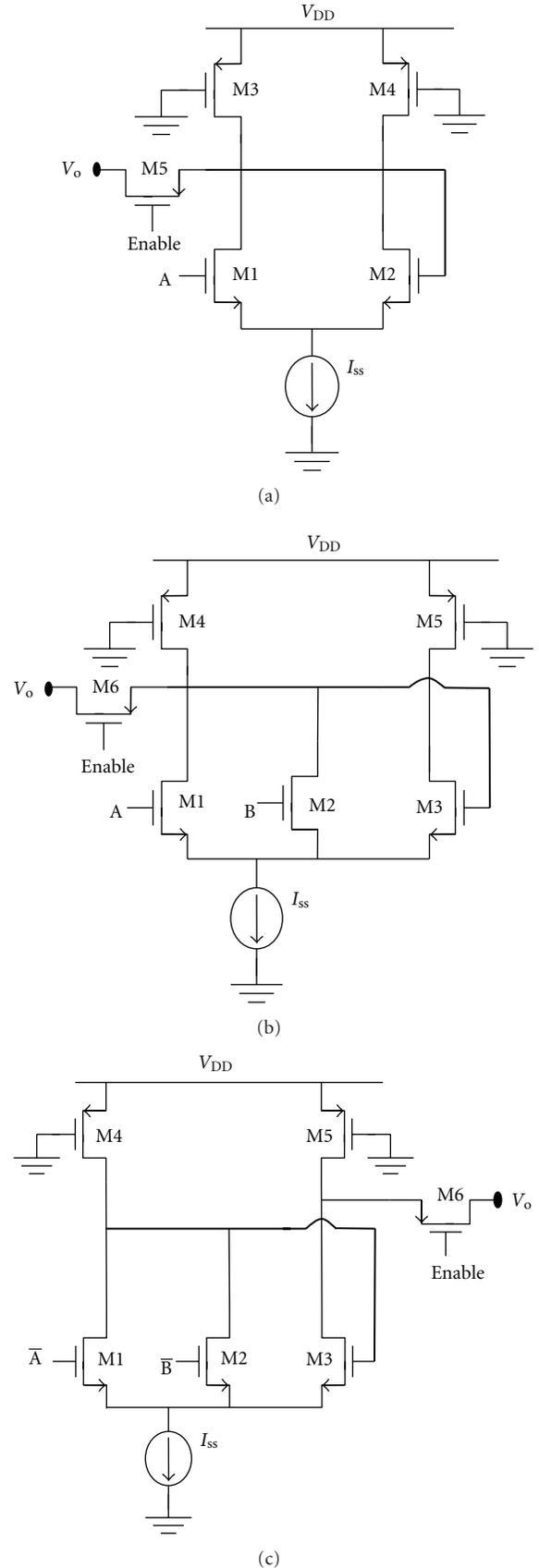


FIGURE 4: Switch-based PFSCl tristate circuits; (a) buffer/inverter (b) 2-input NOR, (c) 2-input NAND.

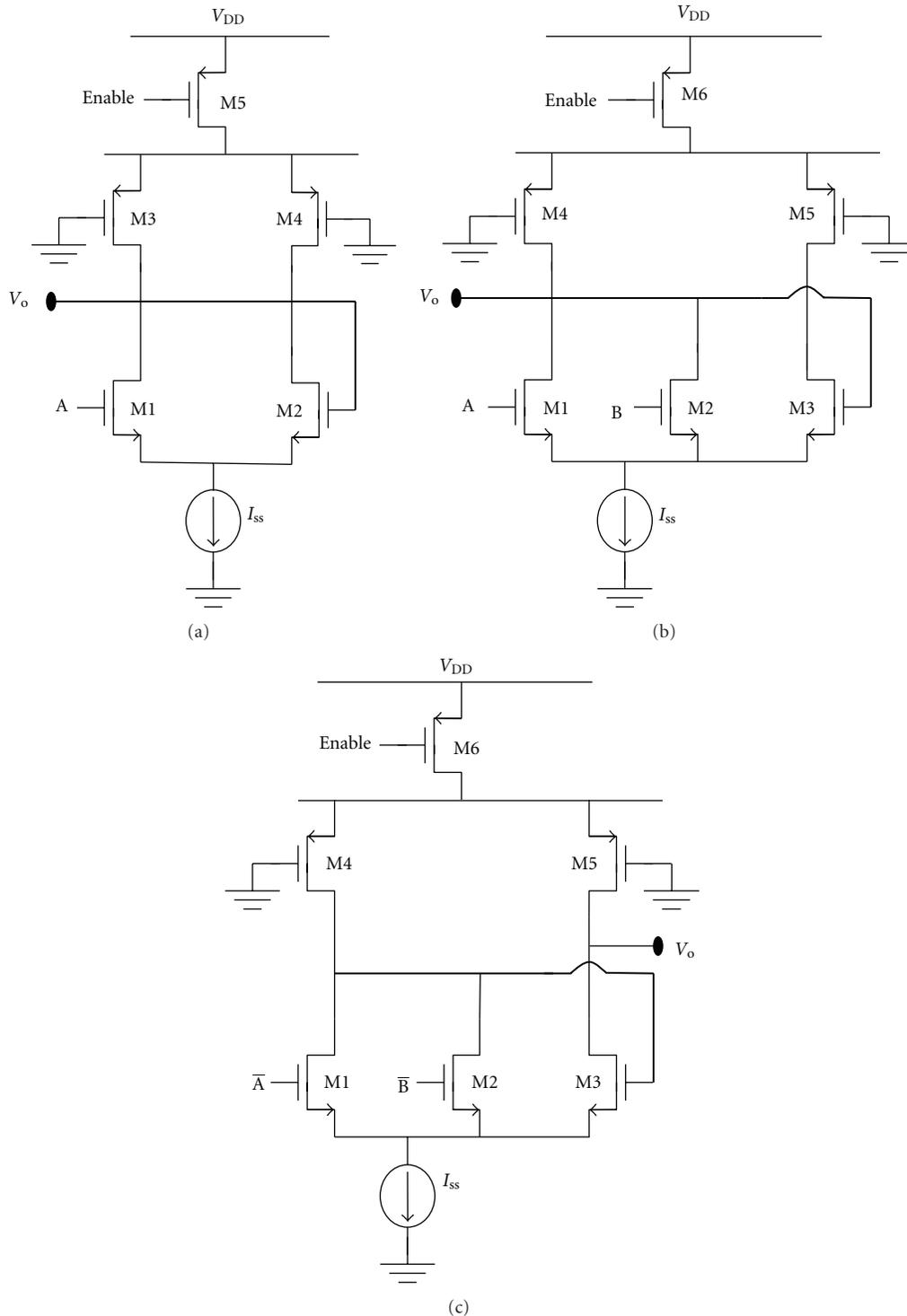


FIGURE 5: Sleep transistor based PFSCl tristate circuits, (a) buffer/inverter, (b) 2-input NOR, and (c) 2-input NAND.

circuit has less static power dissipation than the basic PFSCl buffer/inverter and basically depends on the time duration for which the sleep transistor is on.

Thus, the proposed technique provides low power PFSCl tristate circuits. Similarly, the circuit diagrams of sleep transistor based PFSCl NOR and NAND tristate circuits are shown in Figures 5(b) and 5(c).

4. Simulation Results

Different PFSCl tristate logic gates such as buffer, NOR, and NAND gates have been implemented by using switch-based and sleep transistor techniques. All the gates are simulated using $0.18\ \mu\text{m}$ CMOS technology parameters. The design have been targeted for high speed as it consumes substantial

TABLE 1: CMOS Tristate gates.

Gate	τ_{PD} (ns)	Power dissipation (μW)	Power delay product (fj)
Inverter	0.065	16.2	1.053
NAND	0.078	16.2	1.2636
NOR	0.087	16.2	1.4094

TABLE 2: PFSCl Tristate gates based on switch transistor technique.

Gate	τ_{PD} (ns)	Power dissipation (μW)	Power delay product (fj)
Inverter	0.145	16.2	2.349
NAND	0.575	16.2	9.315
NOR	0.395	16.2	6.399

TABLE 3: PFSCl Tristate gates based on sleep transistor technique.

Gate	τ_{PD} (ns)	Power Dissipation (μW)	Power delay product (fj)
Inverter	0.105	8.1	0.85
NAND	0.148	8.1	1.199
NOR	0.107	8.1	0.867

power. Under this condition, the design parameters such as the voltage swing, the bias current, and the power supply for the gate have been taken as 400 mV, 90 μA , and 1.8 V, respectively, as outlined in [11]. The performance of the circuits obtained by the two techniques is compared with CMOS circuits in terms of power delay through simulations. The simulation results of the circuits in Figures 3, 4 and 5 are listed in Tables 1, 2 and 3 respectively.

It may be observed from Tables 1–3 that the power delay product values for PFSCl tristate circuit based on sleep transistor are better as compared to CMOS and switch-based PFSCl tristate circuits. Further, the overall power dissipation decreases by a percentage equal to the duty cycle of the Enable signal used to drive the circuit into the high impedance state in PFSCl sleep-based tristate circuit. The same behavior is not seen in CMOS and the switch-based PFSCl tristate circuits. Also, at hundreds of MHz frequencies, the dynamic power dissipation of CMOS circuits which increases proportionally with frequency is much greater than power dissipation of a comparable PFSCl circuit.

It may also be noted that in a case where multiple gates of switch-based PFSCl tristate circuits are connected to the same output node, the power dissipation increases by a factor equal to the number of gates attached to the node. This situation does not occur in sleep-based PFSCl and CMOS tristate circuits where only one of the gates is on. Therefore, in such a case, sleep-based PFSCl tristate circuits are the most appropriate choice

5. Conclusion

In this paper, two new design techniques to implement tristate PFSCl circuits have been proposed. The techniques are based on MOS switch and sleep transistor concepts. Different tristate circuits based on both techniques have been

developed and simulated using 0.18 μm CMOS technology parameters. A performance comparison of the proposed circuits with the conventional CMOS circuit indicates that the tristate PFSCl circuits based on sleep transistor technique are more power efficient and have minimum power delay product values than the conventional CMOS and the switch based PFSCl ones.

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