Editorial

Networks-on-Chip: Architectures, Design Methodologies, and Case Studies

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As the density of VLSI design increases, more processors or cores can be placed on a single chip. Therefore, the design of a Multi-Processor System-on-Chip (MP-SoC) architecture, which demands high throughput, low latency, and reliable global communication services, cannot be done by just using current bus-based on-chip communication infrastructures. Networks-on-Chip (NoC) has been proposed in recent years as a promising solution of on-chip interconnection network to provide better scalability, performance, and modularity for current and future MP-SoC architectures.

The paper entitled “Networks on chips: structure and design methodologies” introduces several NoC architectures and discusses the design issues of communication performance, power consumption, signal integrity, and system scalability in an NoC. Then, a novel Bidirectional NoC (BiNoC) architecture with a dynamically self-reconfigurable bidirectional channel is presented, which can break the performance bottleneck caused by bandwidth restriction in conventional NoCs.

Since buffers in on-chip networks constitute a significant proportion of the power consumption and the area of interconnects, reducing the buffer size is an important problem. The paper entitled “A buffer sizing algorithm for network on chips with multiple voltage-frequency islands” describes a two-phase algorithm to size the switch buffers in NoC in considering the support of multiple-frequency islands.

The paper entitled “Self-calibrated energy-efficient and reliable channels for on-chip interconnection networks” depicts the design of an energy-efficient and reliable channel for on-chip interconnection networks (OCINs) using a

self-calibrated voltage scaling technique with self-corrected green (SCG) coding scheme.

Among the NoC components, links that connect the NoC routers are the most power-hungry components. The paper entitled “Intelligent on/off dynamic link management for on-chip networks” presents an intelligent dynamic power management policy for NoCs with improved predictive abilities based on supervised online learning of the system status, where links are turned off and on via the use of a small and scalable neural network.

Monitoring and diagnostic systems are required in modern NoC implementations to assure high performance and reliability. In the paper entitled “Status data and communication aspects in dynamically clustered network-on-chip monitoring,” the design of a dynamically clustered NoC monitoring structure for traffic and fault monitoring is illustrated.

Since biological organisms have better adaptability than computer systems in dealing with environmental changes or noise. A case study on the design of an evolvable neuromolecular hardware motivated from some biological evidence, which integrates inter- and intra-neuronal information processing, is depicted in the paper entitled “A hardware design of neuromolecular network with enhanced resolvability: a bio-inspired approach.”

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