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Research Article

Message Broadcasting via a New Fault Tolerant Irregular Advance Omega Network in Faulty and Nonfaulty Network Environments

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Interconnection Network (IN) is a key element for all parallel processing applications. Multistage Interconnection Network (MIN) is an efficient IN for these applications, as it has the quality of excellent performance at low cost with high reliability. MINs are effective medium for message broadcasting. Doing the same task in faulty situations is a critical challenge. In this paper, we have presented a new Fault Tolerant Interconnection Network named as Irregular Advance Omega Network (IAON); also we have presented its routing algorithm. IAON is the modified form of Advance Omega Network. The proposed MIN can endure multiple faults and provides a suitable path between every source to every destination. We have examined the fault tolerance capacity of IAON and compared its performance with other existing MINs. In order to check the performance of proposed MIN, message broadcasting was performed in three conditions as follows: (1) when network was fault free; (2) when network was Single Switch Faulty in every stage; (3) when network was Double Switch Faulty in every stage. Results showed that IAON performed better than the earlier proposed MINs.

1. Introduction and Motivation

Interconnection Networks have a broad range of application specific domains, for example, On Chip Networks, Storage Area Networks, Local Area Networks, and Wide Area Networks. In all these networks, the basic component is IN which connects various modules with each other [1–5] and therefore, these modules have the proficiency of communication [6–12]. These modules can be of any type like memory, I/O component, processor, functional units, register files, and so forth. MINs are essential INs for various parallel computing and telecommunication applications such as Omega Network, Advance Omega Network, and Clos Network. It is better than the crossbar INs in terms of cost and performance. Generally, a MIN consists of N input and N output devices which are connected via a number of switching stages [13–21]. Based on the availability of paths, MIN may be blocking or nonblocking. Blocking MINs have a unique path between each input and output device, for example, Omega Network. In nonblocking MIN, any input device can be connected to any output device without affecting the existing connection pattern, for example, Clos Network. Nonblocking characteristic shows multipath nature of MINs. Due to the multipath nature of MINs, the concept of fault tolerance came into the limelight [22–34]. Currently, fault tolerance is one of the most widely researched topics [26–34] in the field of MINs. It is defined as

> *"The basic idea for fault-tolerance is to provide multiple paths between source and destination so that alternate paths can be used in case of faults [16]."*

Moreover, data packets can be transmitted using message unicasting method, message multicasting method, and message broadcasting method. In unicasting, a data packet is sent from a source to a single destination. In case of multicasting, a data packet is sent from a source to an arbitrary number of destinations, while in the broadcasting, a data packet

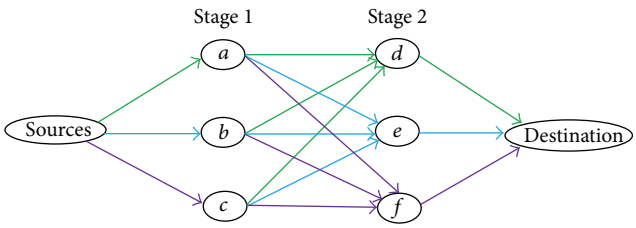

Figure 1: Single and double switch faulty situations in MIN.

is transmitted from a source to all given destinations. In this research work, we have applied message broadcasting technique to analyze the performance of proposed MIN. Adaptive dynamic rerouting strategy [30] was applied on MALN [15], IASEN-2 [18], and IAON for data transmission. In case of faulty switching elements (SEs), data packets were dynamically rerouted [30] from faulty SE to nonfaulty SE to get the desired destination.

1.1. Issue of Fault Tolerance in Multistage Interconnection Networks. The concept of fault tolerance in MINs has been demonstrated in Figure 1. In this figure, we have considered a sample IN which has 2 stages. SEs of this network are a, b, c, d, e, and f. In Figure 1, the primary, first alternate, and second alternate paths are shown by green, light blue, and purple arrows, respectively. Initially, it is assumed that the network is nonfaulty and data will go through a primary path from a source to a destination or to multiple destinations. After this, it is assumed that one SE is faulty in each stage; therefore, data will be routed through first alternate path. These types of networks are known as Single Switch Fault Tolerant Network. Finally, it is assumed that two SEs are faulty in each stage therefore, data will choose second alternate path. These types of networks are known as Double Switch Fault Tolerant Network. If more than two SEs are faulty in each stage then data packets will not reach to their given destinations.

Various researchers have concentrated on fault tolerance [26–34] issue in order to increase the reliability of MINs. Literature survey revealed that in [13–34] ample work has been carried out on Single Switch Fault Tolerant Networks. However, providing an efficient communication through Double Switch Fault Tolerant Network still remained a major research challenge. Towards this problem, we have developed a Double Switch Fault Tolerant MIN named as Irregular Advance Omega Network. It is a reliable IN which provides an excellent communication between every pair of source and destination in presence of multiple faults and also produces better results than the earlier proposed MINs. Furthermore, it is compared with Modified Alpha Network (MALN) [15] and IASEN-2 [18]. Both MALN [15] and IASEN-2 [18] are 4-stage INs for network size $N = 16$ and can tolerate single switch fault in each stage simultaneously.

The rest of the paper is organized as follows. In Section 2, previous fault tolerant networks have been discussed. Section 3 explains the structure of IAON. In Section 4 routing algorithm has been explained. In Section 5, performances of MALN, IASEN-2, and IAON were analyzed with simulation results. Finally, conclusion is presented in Section 6 followed by references.

Before moving to next section, let us have a look on the symbols which are used throughout the paper. Table 1 shows these symbols and their meanings.

2. Preliminaries and Background

Before reaching on next section, we have given a succinct description of MALN [15] and IASEN-2 [18] which were compared with IAON.

2.1. Modified Alpha Network. MALN has N sources and N destinations with $n = \log_2 N$ stages. It is divided into two subgroups with $N/2$ sources and $N/2$ destinations in each. The sources and destinations are connected with the entire network through multiplexer and demultiplexers, respectively. The SEs of n-3, n-2, and n-1 stages are connected through auxiliary links [15]. In the routing process, MALN takes the source and destination addresses in binary format. In the first step, it checks the MSB of the destination address and selects one subnetwork [15], that is, G0 or G1. If the address of SE is known then data will be sent through the shortest path and further routing is not required. If the SE is busy then it routes the data through the auxiliary link otherwise, it drops the request and follows the next step [15]. In the next step, the secondary path is selected and we have to set the MSB of routing tag as 1. In this case, data will be moved through the intermediate stages and if the SE is busy in any of the stages except the last one then the whole procedure is repeated again [15]. In the further step, it routes the data to auxiliary switch of the same stage and then send data to its destination address [15].

2.2. Irregular Augmented Shuffle Exchange Network-2. IASEN-2 has $n = \log_2 N$ stages with N source and N destinations. In this network, first and last stages contain $N/2$ SEs. In the same way, second and third stages have $N/8$ SEs. The SEs of all the stages are allied through the connecting links [18]. In second and third stage it has some extra interconnecting links which are known as auxiliary links [18]. The sources and destinations have a strong connectivity with the entire network through multiplexer and demultiplexers. As far as the routing process of IASEN-2 is concerned, if a SE receives a request from a source or from the SE of previous stage it immediately forwards it towards the SE of next stage [18]. In case if this particular SE is faulty or busy then request will arrive on the alternate SE of the same stage. If the alternate SE is also busy or faulty then network will be failed to send the request to its appropriate destination. If it does not happen so, then it sends the request towards the destination side [18]. If request arrives at the SE of last stage then it will be sent to its appropriate destination through demultiplexer.

Table 1: Various symbols and their meanings.

Symbols	Meaning of Symbol
SE_{P1}	Primary SE of first stage
FB	SE is either faulty or busy
First_Alternate_SE_1	First alternate SE of first stage
Second_Alternate_SE_1	Second alternate SE of first stage
SE-e	SE e of second stage
SE-f	SE f of second stage
SE-g	SE g of second stage
SE_{P3}	Primary SE of third stage
First_Alternate_SE_3	First alternate SE of third stage
Second_Alternate_SE_3	Second alternate SE of third stage
SE_1	SE of first stage
SE_3	SE of third stage
$IAON_{MIN}$	Minimum number of alternate paths in IAON
Allied_SE_1	Allied SEs of first stage
BW_{MALN}	Bandwidth of MALN
$BW_{IASEN-2}$	Bandwidth of IASEN-2
BW_{IAON}	Bandwidth of IAON
PA_{MALN}	Probability of Acceptance of MALN
$PA_{IASEN-2}$	Probability of Acceptance of IASEN-2
PA_{IAON}	Probability of Acceptance of IAON
TP_{MALN}	Throughput of MALN
TP_{MALN_S}	Throughput of MALN in single switch faulty case
$TP_{IASEN-2}$	Throughput of IASEN-2
$TP_{IASEN-2\_S}$	Throughput of IASEN-2 in single switch faulty case
TP_{IAON}	Throughput of IAON
TP_{IAON_S}	Throughput of IAON in single switch faulty case
TP_{IAON_D}	Throughput of IAON in double switch faulty case
PU_{MALN}	Processor Utilization of MALN
PU_{MALN_S}	Processor Utilization of MALN in single switch faulty case
$PU_{IASEN-2}$	Processor Utilization of IASEN-2
$PU_{IASEN-2\_S}$	Processor Utilization of IASEN-2 in single switch faulty case
PU_{IAON}	Processor Utilization of IAON
PU_{IAON_S}	Processor Utilization of IAON in single switch faulty case
PU_{IAON_D}	Processor Utilization of IAON in double switch faulty case
PP_{MALN}	Processing Power of MALN
PP_{MALN_S}	Processing Power of MALN in single switch faulty case
$PP_{IASEN-2}$	Processing Power of IASEN-2
$PP_{IASEN-2\_S}$	Processing Power of IASEN-2 in single switch faulty case
PP_{IAON}	Processing Power of IAON
PP_{IAON_S}	Processing Power of IAON in single switch faulty case
PP_{IAON_D}	Processing Power of IAON in double switch faulty case
rt_{MALN}	Routing Time of MALN
$rt_{IASEN-2}$	Routing Time of IASEN-2
rt_{IAON}	Routing Time of IAON
β_{MALN}	Arrival Time of MALN
$\beta_{IASEN-2}$	Arrival Time of IASEN-2
β_{IAON}	Arrival Time of IAON
γ_{MALN}	Total Arrival Time of MALN
$\gamma_{IASEN-2}$	Total Arrival Time of IASEN-2
γ_{IAON}	Total Arrival Time of IAON
δ_{MALN}	Single Switch Fault Arrival Time of MALN
$\delta_{IASEN-2}$	Single Switch Fault Arrival Time of IASEN-2
δ_{IAON}	Single Switch Fault Arrival Time of IAON
ρ_{IAON}	Double Switch Fault Arrival Time of IAON
NoN	Number of nodes including source and destination node
T	Routing Time between two nodes
NoD	Total number of generated data packets on a source node
NoS	Total number of stages in a MIN

3. Proposed Interconnection Network

The structure of $N \times N$ Irregular Advance Omega Network is based on Advance Omega Network [14]. IAON has 3 stages for every network size. In this network, sources, multiplexers, demultiplexers, and destinations are represented by S, Mux, Demux, and D, respectively. The sizes of Mux and Demux are 2×1 and 1×2, respectively. Presently, there are 16 Mux and 16 Demux in this network. Each Mux connects the N sources to SEs of first stage and each Demux connects SEs of third stage to N destinations. In first and third stage, the network has 4 SEs in each, while second stage has 3 SEs.

The size of SEs in first and third stage is $(N/4 \times 4)$ and $(4 \times N/4)$, respectively. In the second stage, SE e and g have the size 5×5. The size of SE f is 6×6. Each source is connected with two other SEs of first stage through auxiliary links. In the same way, each destination is connected with two other SEs of third stage through auxiliary links. In Figure 2, auxiliary links of second stage are shown by green colour. In IAON, each source and each destination have one primary and two alternate SEs. If the SE is directly connected with any source or any destination then it will be primary SE of that particular source or destination. If it is indirectly (through auxiliary links) connected with any source or destination, then it will be first or second alternate SE of that particular source or destination. Hence, SEs a, b, and c are the primary, first, and second alternate SEs for source 0, respectively. Equally, we can see the primary, first alternate, and second alternate SEs of other sources and destinations in Figure 2.

Redundancy graph [15] of IAON is shown in Figure 3. In this figure, source and destination are shown by green nodes.

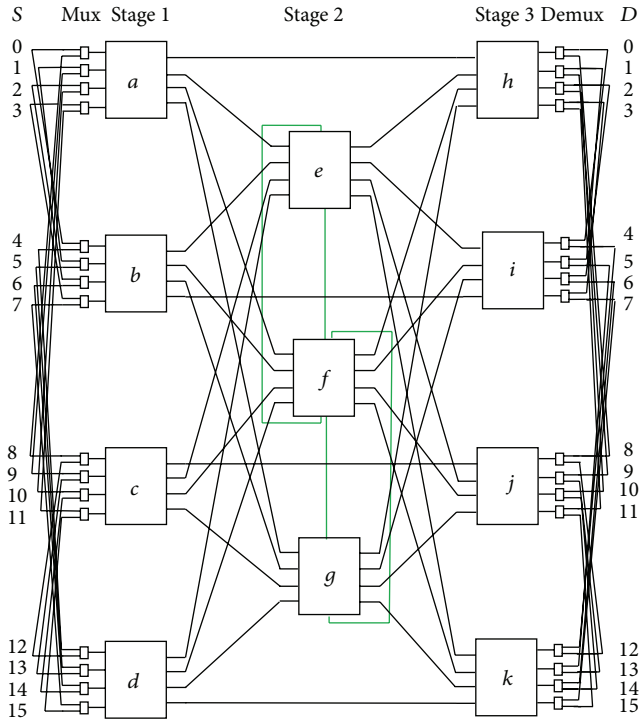

Figure 2: 16 × 16 IAON.

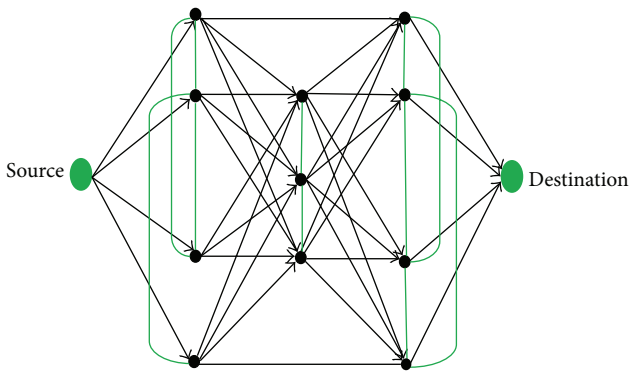

Figure 3: Redundancy graph of IAON.

All the SEs are shown by black nodes, while auxiliary links are shown by green lines. This graph represents that the proposed MIN has the potency of good communication in faulty cases.

4. Routing Algorithm of IAON

Algorithm_IAON_Broadcast is designed for message broadcasting purpose (Algorithm 1). Initially, we have to take the total number of destinations as input from user side then as mentioned in the algorithm function FIRST-STAGE *(Source)* will be called. This function will check the nonfaulty SE in the first stage and transmit the data packets towards that particular SE. If all the SEs that is, primary, first alternate, and second alternate SE are busy or faulty then network will be failed and data transmission process will be stopped. In

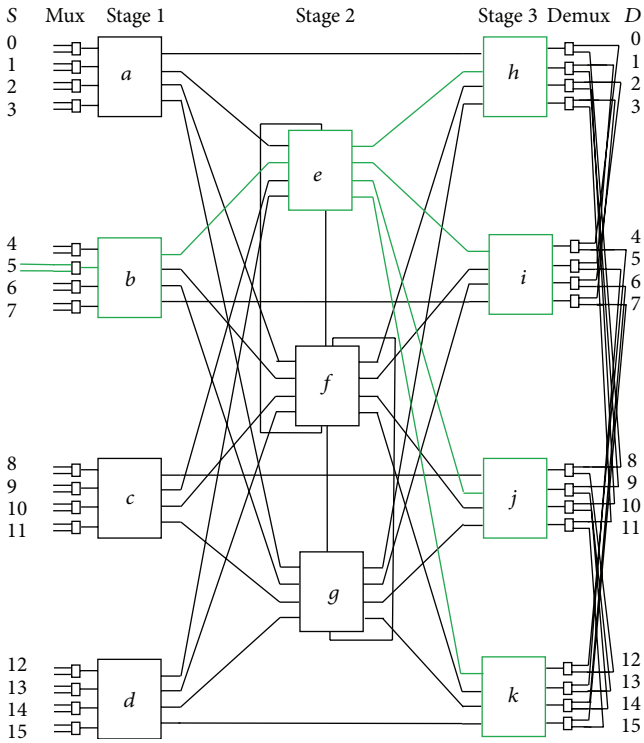

Figure 4: Primary path for source 5.

function SECOND-STAGE *(Source)*, initially primary SE e will collect the data packets from the nonfaulty SE of first stage. If SE e is faulty or busy then these data packets will be dynamically rerouted through first alternate SE f. In case, if SE f is also faulty then second alternate SE g will receive all the data packets.

If all the SEs of second stage are busy or faulty then path will be blocked and data transmission will not be possible in this case. In function THIRD-STAGE *(Source)*, the primary SE obtains the data packets from nonfaulty SE of second stage. This function will also search the nonfaulty SE in third stage and send the data packets to nonfaulty SE. Further, data packets will be transmitted to all destinations. If it does not happen so, IAON will be failed and data transmission process will be stopped.

4.1. Explanation of Routing Algorithm. In this section, we have demonstrated the routes of data packets in Nonfaulty, Single Switch Faulty and Double Switch Faulty cases for source 5.

Case 1 (route of data packets when network is nonfaulty). In this case, we have assumed that IAON does not have any fault and data packets are easily transmitted through the primary SEs. Figure 4 shows the route of data packets through primary SEs. In this case the primary paths for source 5 are as follows:

Path 1: *b-e-h*

Path 2: *b-e-i*

Path 3: *b-e-j*

Path 4: *b-e-k*.

Input: N
Output: Data Packets Successfully Reached on N Destinations or Network Fails
BEGIN
(1) **for** $i = 0$ ***to*** N
(2) Source = i
(3) FIRST-STAGE (Source)

FIRST-STAGE (Source)
(1) **if** SE_{P1} == FB
(2) First_Alternate_SE_1
(3) **else** SECOND-STAGE (Source)
(4) **if** First_Alternate_SE_1 == FB
(5) Second_Alternate_SE_1
(6) **else** SECOND-STAGE (Source)
(7) **if** Second_Alternate_SE_1 == FB
(8) Network Fails
(9) **else** SECOND-STAGE (Source)

SECOND-STAGE (Source)
(1) **if** SE-e == FB
(2) SE-f
(3) **else** THIRD-STAGE (Source)
(4) **if** SE-f == FB
(5) SE-g
(6) **else** THIRD-STAGE (Source)
(7) **if** SE-g == FB
(8) Network Fails
(9) **else** THIRD-STAGE (Source)

THIRD-STAGE (Source)
(1) **if** SE_{P3} == FB
(2) First_Alternate_SE_3
(3) **else** Collect data packets on SE_{P3} and Send to N destinations
(4) **if** First_Alternate_SE_3 == FB
(5) Second_Alternate_SE_3
(6) **else** Collect data packets on First_Alternate_SE_3 and Send to N destinations
(7) **if** Second_Alternate_SE_3 == FB
(8) Network Fails
(9) **else** Collect data packets on Second_Alternate_SE_3 and Send to N destinations
END

Algorithm 1: Algorithm_IAON_Broadcast.

It shows that SEs b, e, h, i, j, and k will be the primary SEs for source 5, and these are shown by green colour in Figure 4.

Case 2 (route of data packets when network is Single Switch Faulty in every stage). In this case, we have assumed that SEs b, e, and h are faulty then first alternate paths for source 5 are as follows:

Path 1: a-f-i
Path 2: a-f-j
Path 3: a-f-k.

Figure 5 shows that SE b is connected with SE a through Mux; hence, SE a is the first alternate SE of first stage for source 5. Similarly, SE f of second stage will be the first alternate SE of second stage. At last in the third stage, Figure 5 shows that SE h is allied with SEs i and j. Therefore, the SEs i and j will be the first alternate SEs of second stage and these SEs are shown by light blue colour in Figure 5. However, SE k is not connected with SE h; hence, it will be treated as primary SE and it is shown by green colour in Figure 5.

Case 3 (route of data packets when network is Double Switch Faulty in every stage). In this case, we have assumed that SEs b, a, e, f, h, and i are faulty then second alternate paths for source 5 are as follows:

Path 1: d-g-j

Path 2: d-g-k.

Figure 6 shows that SE b is connected with SE d through Mux. Hence, SE d is the second alternate SE of first stage for source 5. Similarly, SE g of second stage will be the second alternate SE of second stage. At last in the third stage, Figure 6 shows that SE h and i are allied with SEs j and k. Therefore, the

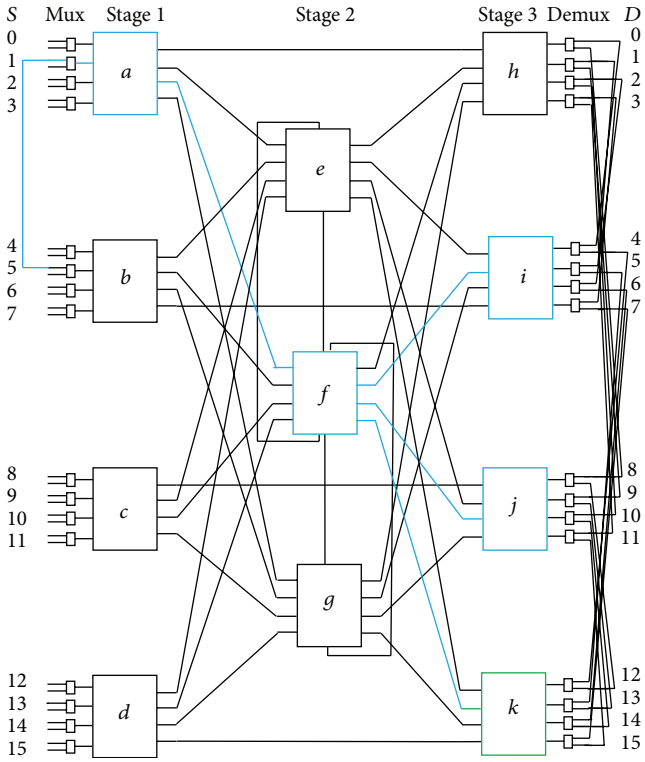

Figure 5: First alternate path for source 5.

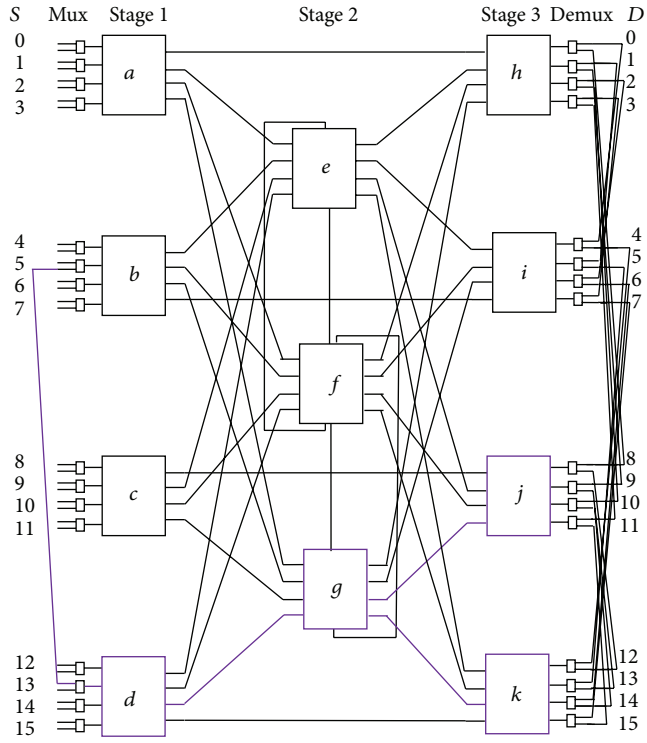

Figure 6: Second alternate path for source 5.

SEs j and k will be the second alternate SEs of second stage, and all these SEs are shown by purple colour in Figure 6.

All the discussed cases clearly explained the proposed routing algorithm. This description also proved that IAON is a Double Switch Fault Tolerant MIN.

4.2. Theorem. Minimum number of alternate paths between every source to every destination is 21.

Proof. In Section 3, it is given that the second stage of IAON connects the SEs of first stage to the SEs of third stage. It shows that the second stage is an important stage of IAON and all the alternate paths are generated by this stage. It is given in Figure 2. This figure shows that if a SE of first stage sends the data packets to the SE of second stage then it will be received by any one SE of second stage. In this way, SEs e, f, and g will generate the 3 different paths. Remaining 4 paths will be generated by auxiliary links of second stage. In this way, we will have the total 7 paths, which are generated by the second stage of IAON. These paths are as follows:

Path 1: SE_1-e-SE_3

Path 2: SE_1-f-SE_3

Path 3: SE_1-g-SE_3

Path 4: SE_1-e-f-SE_3

Path 5: SE_1-f-e-SE_3

Path 6: SE_1-f-g-SE_3

Path 7: SE_1-g-f-SE_3.

Further, it is known that each source is allied with 3 SEs of first stage. Therefore, total number of alternate paths will be

$$\text{IAON}_{\text{MIN}} = (7 \times \text{Allied\_SE}_1)$$
$$\text{IAON}_{\text{MIN}} = (7 \times 3)$$
$$\text{IAON}_{\text{MIN}} = 21.$$

The above discussed hypothesis clearly proves our theorem and tells us that the given theorem is applicable on each network size of IAON. Furthermore, we have taken an example to understand the same fact. □

Example 1. Let the source be 9 and let destination are 2. Figure 2 shows that source 9 is connected with SEs c, a, and d. Equally, destination 2 is connected with SEs h, i, and j. To obtain the alternate paths again we have considered three different cases.

Case 1 (when data packets will be transmitted through primary SE c of first stage). In this case the alternate paths are as follows:

Path 1: c-e-h

Path 2: c-f-h

Path 3: c-g-h

Path 4: c-e-f-h

Path 5: c-f-e-h

Path 6: c-f-g-h

Path 7: c-g-f-h.

Case 2 (when data packets will be transmitted through first alternate SE *a* of first stage). In this case the alternate paths are as follows:

Path 1: *a-e-h*
Path 2: *a-f-h*
Path 3: *a-g-h*
Path 4: *a-e-f-h*
Path 5: *a-f-e-h*
Path 6: *a-f-g-h*
Path 7: *a-g-f-h.*

Case 3 (when data packets will be transmitted through second alternate SE *d* of first stage). In this case the alternate paths are as follows:

Path 1: *d-e-h*
Path 2: *d-f-h*
Path 3: *d-g-h*
Path 4: *d-e-f-h*
Path 5: *d-f-e-h*
Path 6: *d-f-g-h*
Path 7: *d-g-f-h.*

In all these cases the total numbers of paths are 21. It proved that IAON has minimum 21 alternate paths from any source to any destination.

5. Performance Analysis and Simulation Results

To evaluate the performance of IAON, we have simulated the proposed routing algorithm in java technology using JDK 1.6 platform. We have compared the probability of acceptance, throughput, processor utilization and processing power of IAON with MALN [15] and IASEN-2 [18]. Basically, message broadcasting was performed in our simulation. In nonfaulty case, data packets will take the shortest path from source node to destination node and we assumed that the data transmission time between two nodes is 0.1 ms. In faulty situation, we have dynamically rerouted the data packets from faulty to appropriate nonfaulty node. Therefore, these data packets can be transmitted to the given destinations. In faulty cases, we have assumed that a data packet takes 0.2 ms in its rerouting process. Routing time of a data packet is explained in Sections 5.3 to 5.7. Before coming on the simulation results let us have a look on the various performance parameters.

5.1. Request Generation Probability (p). The term "Request Generation Probability" represents the number of data packets generated on a source node and these generated data packets can be transmitted to N destinations through IAON, MALN [15], and IASEN-2 [18]. In this simulation, p is assumed to be 0.1, 0.2, . . . , 0.9, 1. Data packets were generated and transmitted to MALN, IASEN-2, and IAON in faulty and nonfaulty cases.

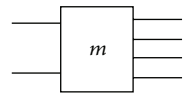

Figure 7: SE m of size 2×4.

5.2. Bandwidth (BW). To calculate the BW of IAON, MALN, and IASEN-2, we have applied the probabilistic method on these networks. Before calculating the BW of IAON, MALN, and IAEN-2, let us have a look on the probabilistic method [13–17].

Assume that a switching element m has $a = 2$ input lines and $b = 4$ output lines as shown in Figure 7 and therefore, the size of SE m is 2×4.

As we know that p is the Request Generation Probability and when it is applied on the input lines of SE m then it collects the data packets and transmits them towards the SE of next stage. Hence,

"Probability [13, 14] of not getting the request is: $(1 - (p/b))$*",*

"Probability [13, 14] of not getting the request from "a" inputs is: $(1 - (p/b))^a$*",*

"Probability [13, 14] of one output getting the request from "a" inputs is: $1 - (1 - (p/b))^a$*",*

"Probability [13, 14] of one output getting the request from "a" inputs is: $1 - (1 - (p/b))^a$*",*

"Total number of requests [13, 14] that are passed per unit time is: $b - b(1 - (p/b))^a$*".*

For SE m, *"Total number of requests that are passed per unit time is:* $4 - 4(1 - (p/4))^2$*".*

The output of a stage will be the input of next stage and finally the output rate of last stage will be the BW of a MIN [13–17]. In this way, BW of a MIN can be obtained easily. The definition of BW is as follows.

Definition 2. "BW is defined as the mean number of active memory modules in a transfer cycle of INs and therefore, BW is the total number of request matured [14–17]."

According to Definition 2, BW of a MIN will be BW $= b^n \times p_n$ bytes/ms or BW $= N_{\mathrm{DST}} \times p_n$ bytes/ms and $p_0 = p$.

Here, b^n is the total number of destinations (N_{DST}) and p_0 is also the request generation probability.

5.2.1. BW Calculations of MALN, IASEN-2, and IAON. To calculate the BW we have assumed that total number of stages

for each network size will be constant that is, for MALN, IASEN-2, and IAON it will be 4, 4, and 3, respectively.

Probability equations for MALN [15] are as follows:

$$\begin{aligned} p(1)_{\mathrm{MALN}} &= \left\{1-\left(1-\frac{p}{3}\right)\right\}^{3}, \\ p(2)_{\mathrm{MALN}} &= \left\{1-\left(1-\frac{p(1)}{6}\right)\right\}^{((N/8)+1)}, \\ p(3)_{\mathrm{MALN}} &= \left\{1-\left(1-\frac{p(2)}{((N/8)+1)}\right)\right\}^{3}, \\ p(4)_{\mathrm{MALN}} &= \left\{1-\left(1-p(3)\times 1-\frac{p(1)}{2}\right)\right\}^{2}, \\ \mathrm{BW}_{\mathrm{MALN}} &= \left\{p(4)_{\mathrm{MALN}}\times N_{\mathrm{DST}}\right\}. \end{aligned} \tag{1}$$

As we know, N_{DST} is the total number of destinations.

Probability equations for IASEN-2 [18] are as follows:

$$\begin{aligned} p(1)_{\mathrm{IASEN\text{-}2}} &= \left\{1-\left(1-\frac{p}{2}\right)\right\}^{2}, \\ p(2)_{\mathrm{IASEN\text{-}2}} &= \left\{1-\left(1-\frac{p(1)}{6}\right)\right\}^{((N/2)+1)}, \\ p(3)_{\mathrm{IASEN\text{-}2}} &= \left\{1-\left(1-\frac{p(2)}{((N/2)+1)}\right)\right\}^{3}, \\ p(4)_{\mathrm{IASEN\text{-}2}} &= \left\{1-\left(1-p(3)\times 1-\frac{p(1)}{2}\right)\right\}^{2}, \\ \mathrm{BW}_{\mathrm{IASEN\text{-}2}} &= \left\{p(4)_{\mathrm{IASEN\text{-}2}}\times N_{\mathrm{DST}}\right\}. \end{aligned} \tag{2}$$

Probability equations for IAON are as follows:

$$\begin{aligned} p(1)_{\mathrm{IAON}} &= \left\{1-\left(1-\frac{p}{4}\right)\right\}^{(N/4)}, \\ p(2)_{\mathrm{IAON}} &= \left\{1-\left(1-\frac{p(1)}{16}\right)\right\}^{5}, \\ p(3)_{\mathrm{IAON}} &= \left\{1-\left(1-p(2)\times\left(1-\frac{p(1)}{N/4}\right)\right)\right\}^{4}, \\ \mathrm{BW}_{\mathrm{IAON}} &= \left\{p(3)_{\mathrm{IAON}}\times N_{\mathrm{DST}}\right\}. \end{aligned} \tag{3}$$

Figure 8 shows the bandwidth comparison of MALN, IASEN-2, and IAON for network size $N = 16, 32, 64$, and 128. Bandwidth of IAON is better than the other two MINs [15, 18].

5.3. Routing Time (rt). It is the time that a data packet takes from a source node to the given destination node. It is calculated by the following formula:

$$\mathrm{rt} = (\mathrm{NoN}-1)\times T, \tag{4}$$

where routing times of MALN [15], IASEN-2 [18], and IAON are as follows:

$$\begin{aligned} \mathrm{rt}_{\mathrm{MALN}} &= (4\times T) \quad \text{NoN is 5 in MALN,} \\ \mathrm{rt}_{\mathrm{IASEN\text{-}2}} &= (5\times T) \quad \text{NoN is 6 in IASEN-2,} \\ \mathrm{rt}_{\mathrm{IAON}} &= (4\times T) \quad \text{NoN is 5 in IAON.} \end{aligned} \tag{5}$$

5.4. Arrival Time (β). Arrival time is the time that a source node takes in order to send a data packet to all given destinations. It is given by the following formula:

$$\beta = \left(\mathrm{rt}\times N_{\mathrm{DST}}\right). \tag{6}$$

Therefore, arrival time of MALN, IASEN-2, and IAON is as follows:

$$\begin{aligned} \beta_{\mathrm{MALN}} &= \left(4\times T\times N_{\mathrm{DST}}\right), \\ \beta_{\mathrm{IASEN\text{-}2}} &= \left(5\times T\times N_{\mathrm{DST}}\right), \\ \beta_{\mathrm{IAON}} &= \left(4\times T\times N_{\mathrm{DST}}\right). \end{aligned} \tag{7}$$

Arrival time is also explained in Example 3.

Example 3. Suppose we have to calculate the arrival time of a data packet for the network shown in Figure 9.

In Figure 9, we have taken a single stage IN. In this figure, red node is source, green nodes are destinations, and rests of the nodes are SEs of the network. At present, data packet is going through a light blue SE of network and data path is shown by green dotted arrows. It is assumed that a data packet is taking 0.1 ms from a SE to another SE. Hence,

$T = 0.1$ ms,

NoN = 3,

rt $= (3-1)\times 0.1$,

rt $= 0.2$ ms,

$\beta = (\mathrm{rt}\times N_{\mathrm{DST}})$,

$N_{\mathrm{DST}} = 2$,

$\beta = 0.4$ ms is the arrival time of a data packet.

5.5. Total Arrival Time (γ). Total arrival time is the time that all generated data packets take from a source to all given destinations. It is given by the following formula:

$$\begin{aligned} \gamma &= \beta\times \mathrm{NoD}, \\ \gamma_{\mathrm{MALN}} &= \left(\beta_{\mathrm{MALN}}\times \mathrm{NoD}\right), \\ \gamma_{\mathrm{IASEN\text{-}2}} &= \left(\beta_{\mathrm{IASEN\text{-}2}}\times \mathrm{NoD}\right), \\ \gamma_{\mathrm{IAON}} &= \left(\beta_{\mathrm{IAON}}\times \mathrm{NoD}\right). \end{aligned} \tag{8}$$

If NoD are 100 then total arrival time of Example 3 will be $\gamma = 40$ ms.

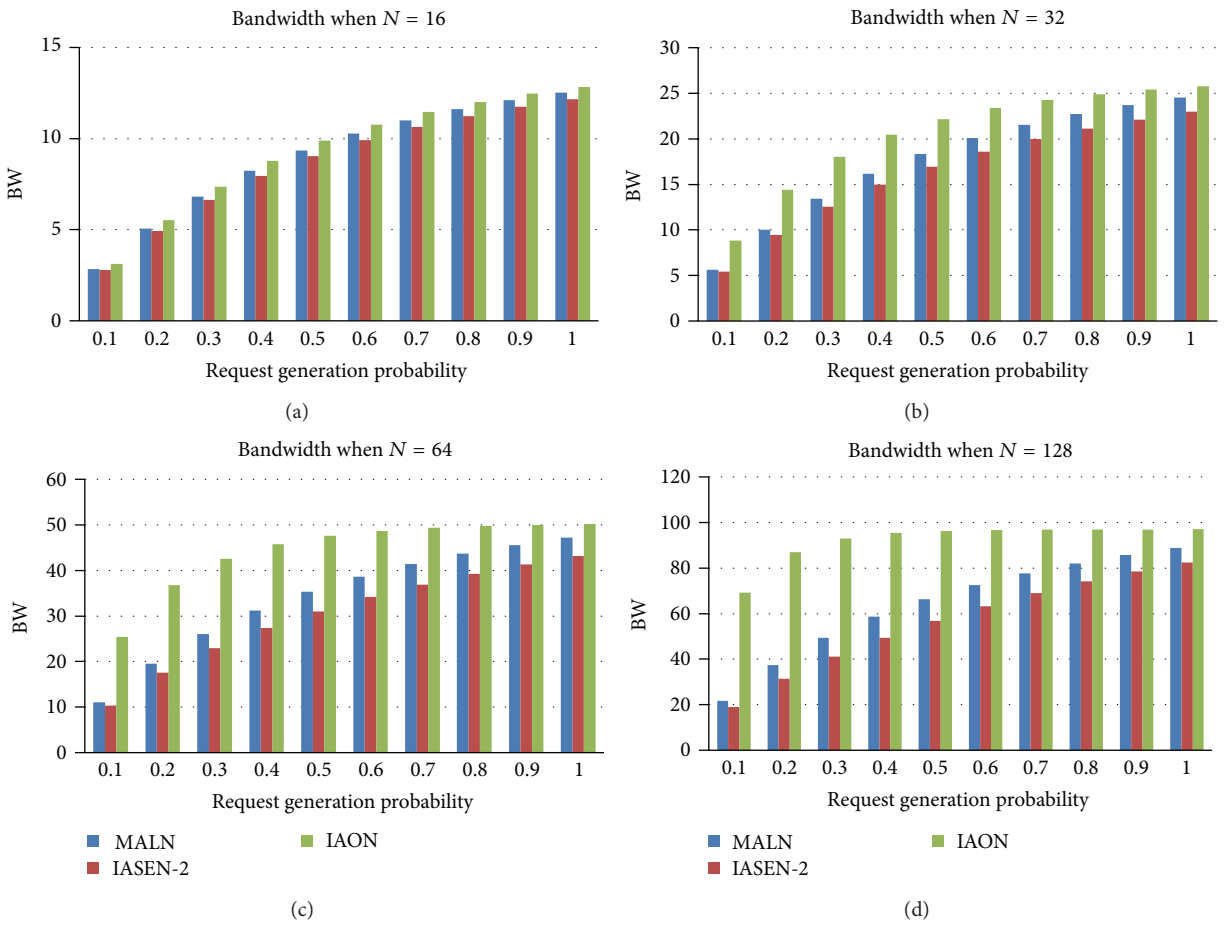

Figure 8: The bandwidth of MALN, IASEN-2, and IAON when network sizes are 16, 32, 64, and 128 separately.

5.6. Single Switch Fault Arrival Time (δ). When single switch is faulty in every stage of the network then the arrival time of all the data packets from a source to all the destinations is given by the following formula:

$$\begin{aligned} \delta &= \gamma + (\text{NoS} \times T), \\ \delta_{\text{MALN}} &= \gamma_{\text{MALN}} + (4 \times T) \quad \text{NoS for MALN is 4}, \\ \delta_{\text{IASEN-2}} &= \gamma_{\text{IASEN-2}} + (4 \times T) \quad \text{NoS for IASEN-2 is 4}, \\ \delta_{\text{IAON}} &= \gamma_{\text{IAON}} + (4 \times T) \quad \text{NoS for IAON is 3}. \end{aligned} \tag{9}$$

In Example 3, the network has only one stage therefore, NoS = 1 and we assumed that the light blue SE in Figure 9 is faulty then

$$\delta = [40 + \{1 \times .1\}],$$

$$\delta = 40.1 \text{ ms}.$$

5.7. Double Switch Fault Arrival Time (ρ). When double switch is faulty in every stage of the network then in this case the arrival time of a data packet from a source to all the destinations is given by the following formula:

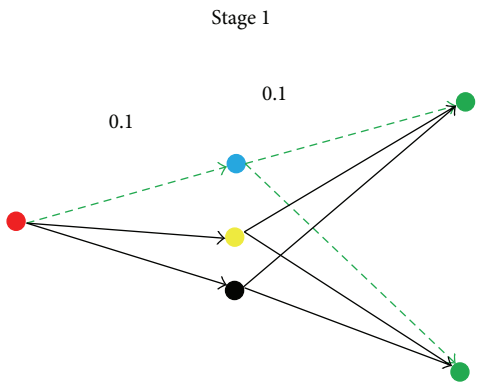

Figure 9: Calculation of arrival time.

$$\begin{aligned} \rho &= \gamma + (\text{NoS} \times 2 \times T), \\ \rho_{\text{IAON}} &= \gamma_{\text{IAON}} + (6 \times T). \end{aligned} \tag{10}$$

We know that MALN [15] and IASEN-2 [18] are not Double Switch Fault Tolerant Network. Therefore, we cannot calculate the double switch fault arrival time of these networks.

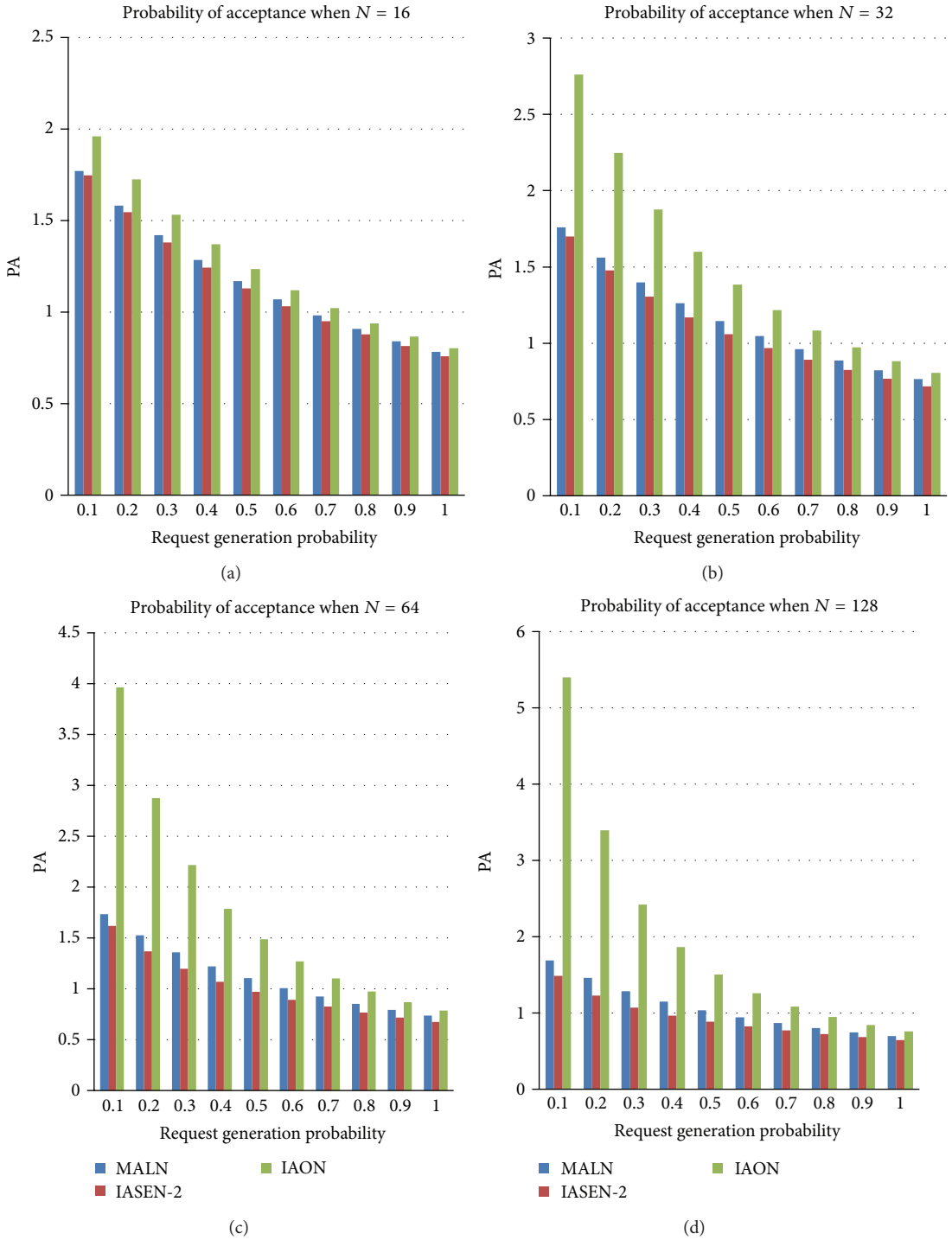

Figure 10: The probability of acceptance of MALN, IASEN-2, and IAON when network sizes are 16, 32, 64, and 128 separately.

In Example 3, now we assumed that the light blue and yellow SEs in Figure 9 are faulty then

$$\rho = 40 + (1 \times 2 \times 0.1) \quad \rho = 40.2\ \text{ms}. \tag{11}$$

5.8. Probability of Acceptance (PA). How many requests are going to be accepted by the destination side which is sent by the source side in a transfer cycle? PA is the answer of this question. Actually, during the data transmission process some data packets get blocked due to switch failure, link failure, or any other reason. Therefore, the total number of generated data packets on a source node and total number of accepted data packets by a destination node in a transfer cycle will not be the same [13]. It can be given by the following definition.

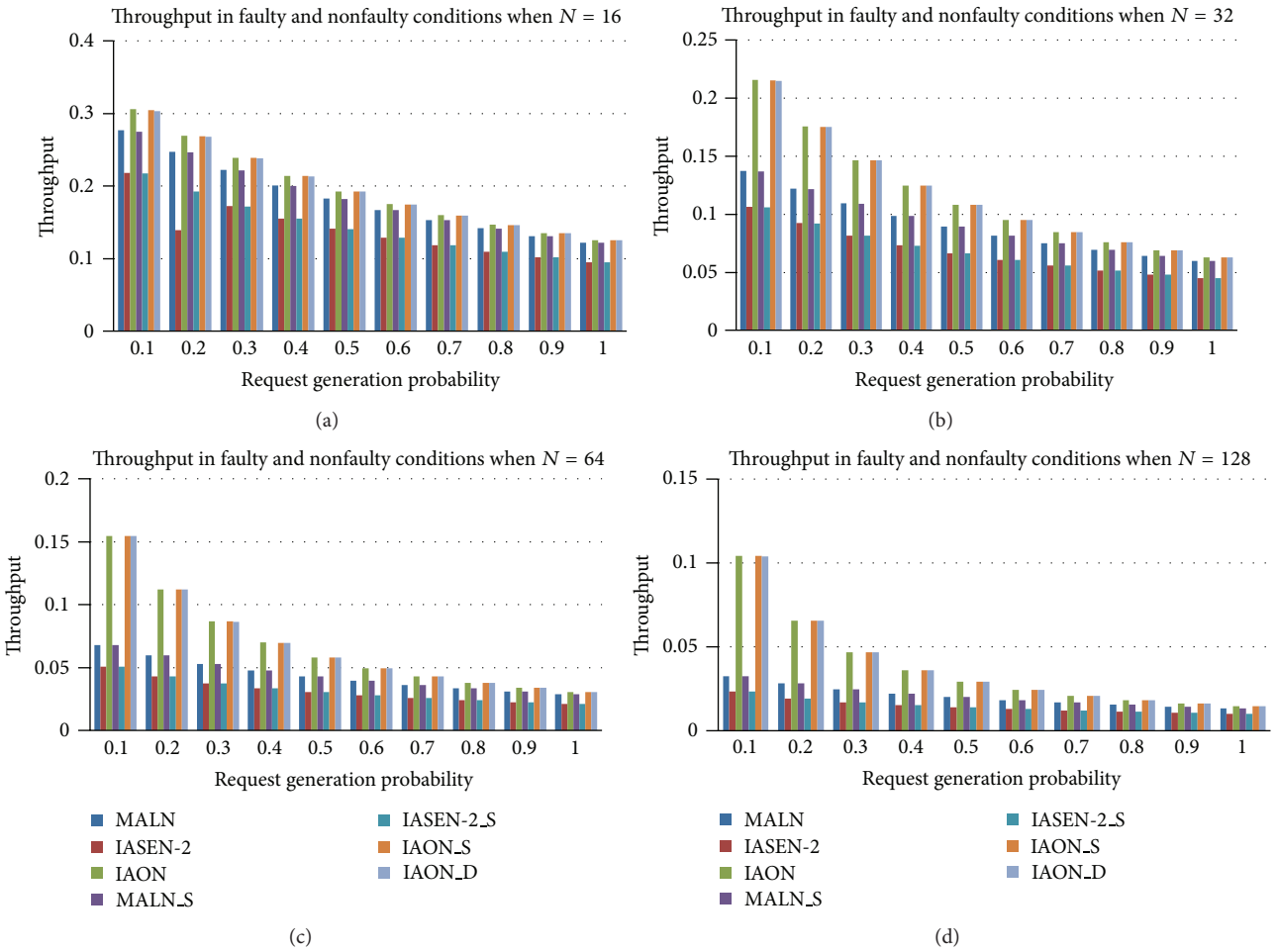

Figure 11: The throughput of MALN, IASEN-2, and IAON in faulty and nonfaulty cases, when the network sizes are 16, 32, 64, and 128 separately.

Definition 4. *"It is defined as ratio of bandwidth to the expected number of requests generated per transfer cycle [15–18]".*

Formula for PA [15–17] is

$$\mathrm{PA} = \left(\frac{\mathrm{BW}}{N_{\mathrm{DST}} \times p}\right). \tag{12}$$

Now, PA of MALN, IASEN-2, and IAON is given by the following formulas:

$$\begin{aligned} \mathrm{PA}_{\mathrm{MALN}} &= \left(\frac{\mathrm{BW}_{\mathrm{MALN}}}{N_{\mathrm{DST}} \times p}\right), \\ \mathrm{PA}_{\mathrm{IASEN\text{-}2}} &= \left(\frac{\mathrm{BW}_{\mathrm{IASEN\text{-}2}}}{N_{\mathrm{DST}} \times p}\right), \\ \mathrm{PA}_{\mathrm{IAON}} &= \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{N_{\mathrm{DST}} \times p}\right). \end{aligned} \tag{13}$$

5.9. Throughput (TP). Basically, it is the average number of data packets which are going to be accepted by all destinations in a transfer cycle [13]. We can define it as follows.

Definition 5. *"Throughput means average number of cells delivered by a network per unit time [15–17]."*

Formula for TP is [13]

$$\mathrm{TP} = \left(\frac{\mathrm{BW}}{N_{\mathrm{DST}} \times t}\right). \tag{14}$$

Here, t is the transmission time of a MIN in ms.

TP of MALN [15], IASEN-2 [18], and IAON is given by the following formulas:

$$\begin{aligned} \mathrm{TP}_{\mathrm{MALN}} &= \left(\frac{\mathrm{BW}_{\mathrm{MALN}}}{N_{\mathrm{DST}} \times \gamma_{\mathrm{MALN}}}\right), \\ \mathrm{TP}_{\mathrm{IASEN\text{-}2}} &= \left(\frac{\mathrm{BW}_{\mathrm{IASEN\text{-}2}}}{N_{\mathrm{DST}} \times \gamma_{\mathrm{IASEN\text{-}2}}}\right), \\ \mathrm{TP}_{\mathrm{IAON}} &= \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{N_{\mathrm{DST}} \times \gamma_{\mathrm{IAON}}}\right), \\ \mathrm{TP}_{\mathrm{MALN\_S}} &= \left(\frac{\mathrm{BW}_{\mathrm{MALN}}}{N_{\mathrm{DST}} \times \delta_{\mathrm{MALN}}}\right), \end{aligned}$$

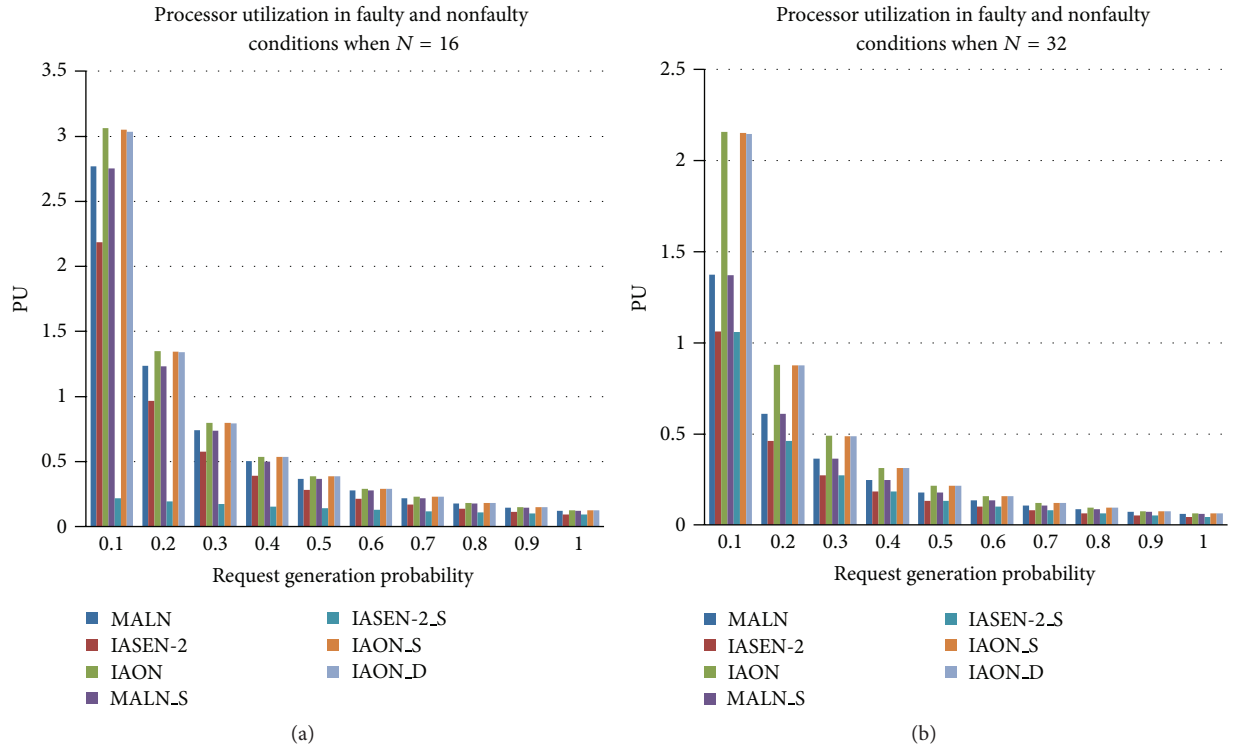

Figure 12: The processor utilization of MALN, IASEN-2, and IAON in faulty and nonfaulty cases, when the network sizes are 16 and 32 separately.

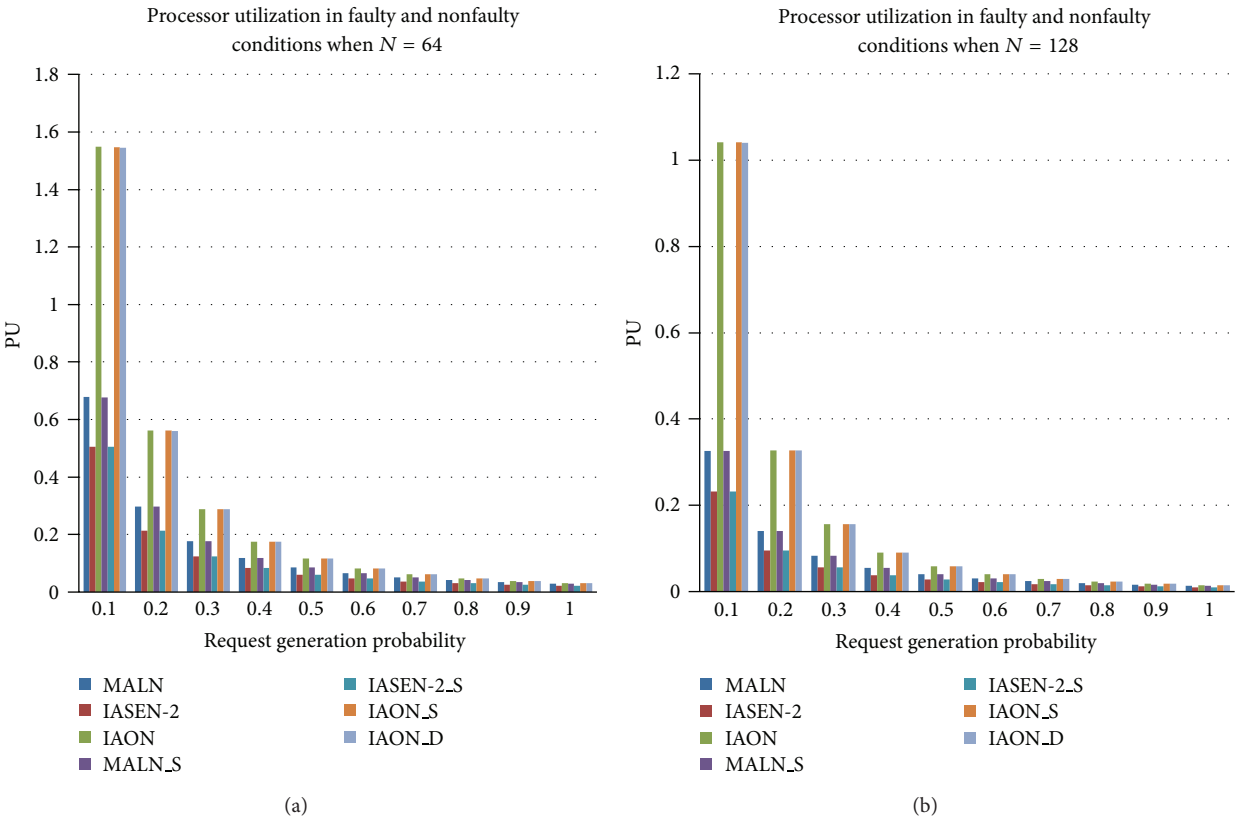

Figure 13: The processor utilization of MALN, IASEN-2, and IAON in faulty and nonfaulty cases, when the network sizes are 64 and 128 separately.

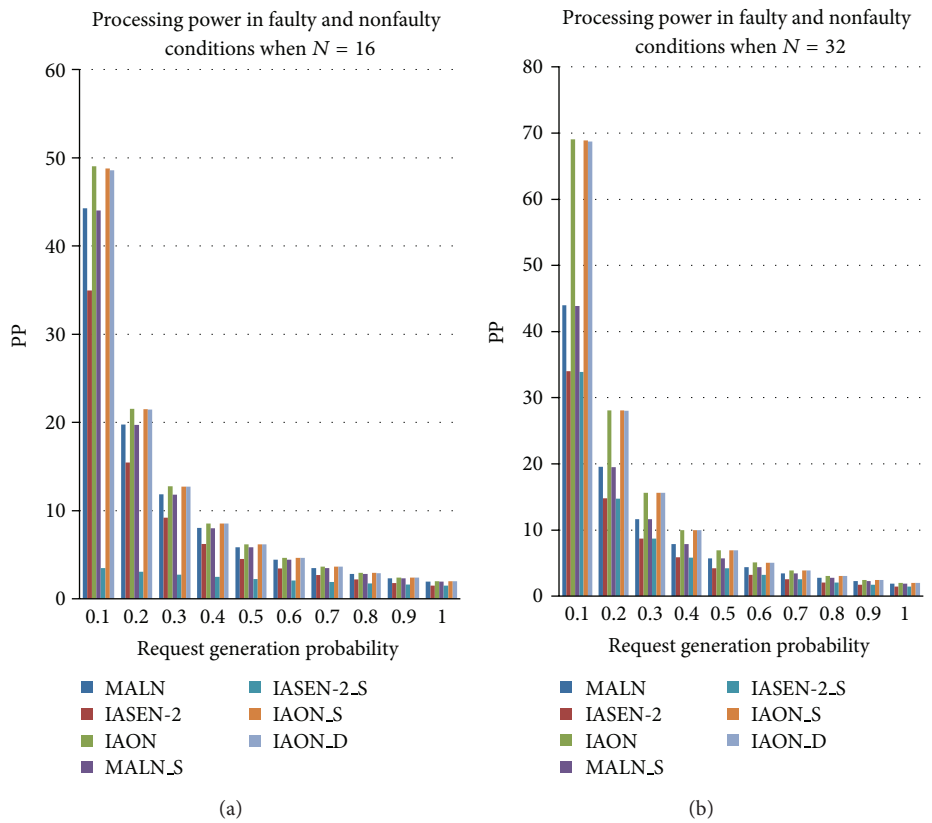

FIGURE 14: The processing power of MALN, IASEN-2, and IAON in faulty and nonfaulty cases, when the network sizes are 16 and 32 separately.

$$\mathrm{TP}_{\mathrm{IASEN\text{-}2\_S}} = \left(\frac{\mathrm{BW}_{\mathrm{IASEN\text{-}2}}}{N_{\mathrm{DST}} \times \delta_{\mathrm{IASEN\text{-}2}}}\right),$$
$$\mathrm{TP}_{\mathrm{IAON\_S}} = \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{N_{\mathrm{DST}} \times \delta_{\mathrm{IAON}}}\right),$$
$$\mathrm{TP}_{\mathrm{IAON\_D}} = \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{N_{\mathrm{DST}} \times \rho_{\mathrm{IAON}}}\right). \quad (15)$$

5.10. Processor Utilization (PU). In each transfer cycle, data packets are transmitted from source side to destination side [13–16]. For this transmission, processor plays a vital role in order to make this computation fast and efficient. Therefore, a specific amount of time is taken by the processor for each transfer cycle [15]. This time is considered as the utilization time of the processor and can be defined as follows.

Definition 6. "PU is defined as percentage of time the processor is active doing computation without accessing the global memory [15–17]."

Formula for PU [13] is

$$\mathrm{PU} = \left(\frac{\mathrm{BW}}{p \times N_{\mathrm{DST}} \times t}\right) \quad (16)$$

PU of MALN [15], IASEN-2 [18], and IAON is given by the following formulas

$$\mathrm{PU}_{\mathrm{MALN}} = \left(\frac{\mathrm{BW}_{\mathrm{MALN}}}{p \times N_{\mathrm{DST}} \times \gamma_{\mathrm{MALN}}}\right),$$
$$\mathrm{PU}_{\mathrm{IASEN\text{-}2}} = \left(\frac{\mathrm{BW}_{\mathrm{IASEN\text{-}2}}}{p \times N_{\mathrm{DST}} \times \gamma_{\mathrm{IASEN\text{-}2}}}\right),$$
$$\mathrm{PU}_{\mathrm{IAON}} = \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{p \times N_{\mathrm{DST}} \times \gamma_{\mathrm{IAON}}}\right),$$
$$\mathrm{PU}_{\mathrm{MALN\_S}} = \left(\frac{\mathrm{BW}_{\mathrm{MALN}}}{p \times N_{\mathrm{DST}} \times \delta_{\mathrm{MALN}}}\right),$$
$$\mathrm{PU}_{\mathrm{IASEN\text{-}2\_S}} = \left(\frac{\mathrm{BW}_{\mathrm{IASEN\text{-}2}}}{p \times N_{\mathrm{DST}} \times \delta_{\mathrm{IASEN\text{-}2}}}\right),$$
$$\mathrm{PU}_{\mathrm{IAON\_S}} = \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{p \times N_{\mathrm{DST}} \times \delta_{\mathrm{IAON}}}\right),$$
$$\mathrm{PU}_{\mathrm{IAON\_D}} = \left(\frac{\mathrm{BW}_{\mathrm{IAON}}}{p \times N_{\mathrm{DST}} \times \rho_{\mathrm{IAON}}}\right). \quad (17)$$

5.11. Processor Power (PP). PP is calculated on the behalf of processors which are used during the transmission of data packets [13]. It can be defined as follows.

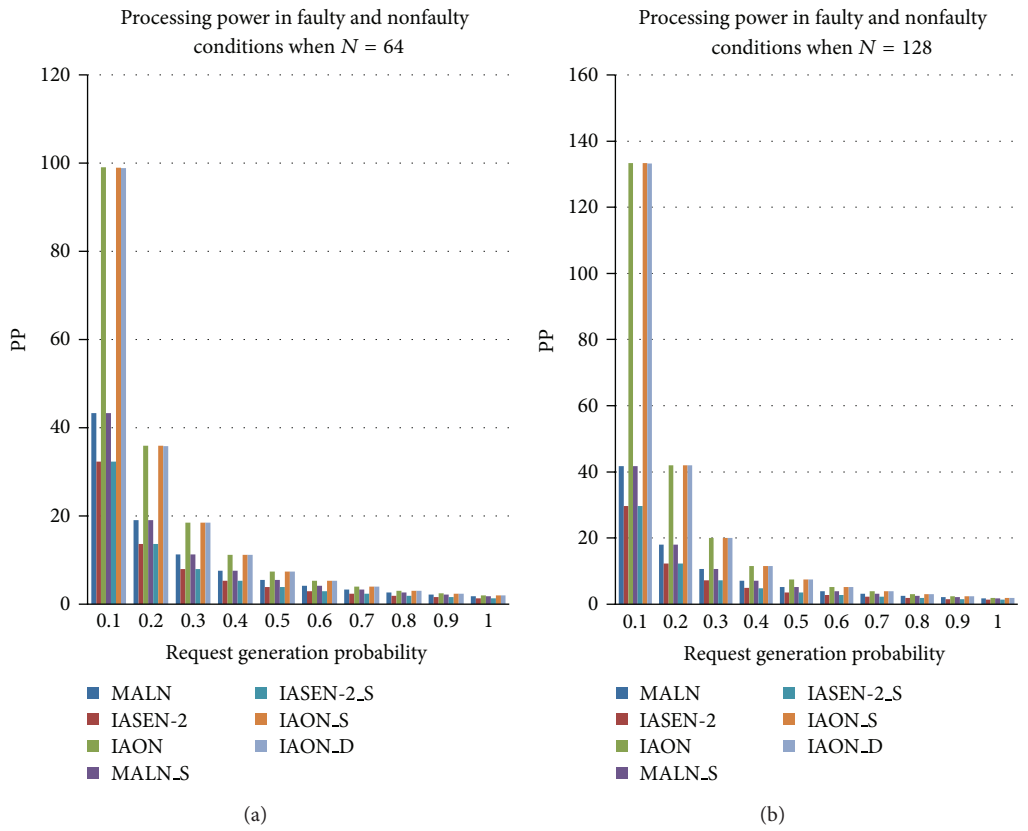

Figure 15: The processing power of MALN, IASEN-2, and IAON in faulty and nonfaulty cases, when the network sizes are 64 and 128 separately.

Definition 7. *"PP is defined as sum of processor utilization over the number of processors [13, 17]."*

Formula for PP is

$$\mathrm{PP} = \left(N_{\mathrm{DST}} \times \mathrm{PU}\right) \tag{18}$$

PP of MALN [15], IASEN-2 [18], and IAON is given by the following formulas:

$$\begin{aligned}
\mathrm{PP}_{\mathrm{MALN}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{MALN}}\right), \\
\mathrm{PP}_{\mathrm{IASEN\text{-}2}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{IASEN\text{-}2}}\right), \\
\mathrm{PP}_{\mathrm{IAON}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{IAON}}\right), \\
\mathrm{PP}_{\mathrm{MALN_S}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{MALN_S}}\right), \\
\mathrm{PP}_{\mathrm{IASEN\text{-}2_S}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{IASEN\text{-}2_S}}\right), \\
\mathrm{PP}_{\mathrm{IAON_S}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{IAON_S}}\right), \\
\mathrm{PP}_{\mathrm{IAON_D}} &= \left(N_{\mathrm{DST}} \times \mathrm{PU}_{\mathrm{IAON_D}}\right).
\end{aligned} \tag{19}$$

Now, we have shown the results which were obtained using the above-mentioned formulas.

Figure 10 shows the probability of acceptance of MALN [15], IASEN-2 [18], and IAON in faulty and nonfaulty cases for network size $N = 16, 32, 64$, and 128. Both figures show that IAON is better than MALN and IASEN-2 in terms of PA.

Figure 11 shows the throughput of MALN [15], IASEN-2 [18], and IAON in faulty and nonfaulty cases for network size $N = 16, 32, 64$, and 128. This figure shows that IAON is better than MALN and IASEN-2 in terms of TP. In Figures 11, 12, 13, 14, and 15 we have shown the performance of MALN_S, IASEN-2_S, IAON_S, and IAON_D. The significance of these networks is as follows:

MALN_S: MALN [15] is Single Switch Fault Tolerant in every stage,

IASEN-2_S: IASEN-2 [18] is Single Switch Fault Tolerant in every stage,

IAON_S: IAON is Single Switch Fault Tolerant in every stage,

IAON_D: IAON is Double Switch Fault Tolerant in every stage.

Figures 12 and 13 show the processor utilization of MALN [15], IASEN-2 [18], and IAON in faulty and nonfaulty cases for network size $N = 16, 32, 64$, and 128. Both figures show that IAON is better than MALN and IASEN-2 in terms of PU.

Figures 14 and 15 show the processing power of MALN [15], IASEN-2 [18], and IAON in faulty and nonfaulty cases for network size $N = 16, 32, 64$, and 128. Both figures show that IAON is better than MALN and IASEN-2 in terms of PP.

In Figures 11, 12, 13, 14, and 15, the time is converted from ms to seconds to explain the results evidently.

6. Conclusion

Faults are not a new issue in the MINs. However, developing a MIN with high performance and great fault tolerability is an important factor in recent networks. In this paper, we have proved that IAON can tolerate concurrently 2-faulty SEs in each stage. Also we have demonstrated that it has more alternate paths for data transmission as compared to MALN and IASEN-2. The routing algorithm of IAON is a generalized algorithm for message broadcasting and it provides the suitable way to all data packets to reach the given destinations in faulty and nonfaulty situations. Furthermore, all the performance factors such as probability of acceptance, throughput, processor utilization, and processing power of IAON are better than MALN and IASEN-2 in faulty and nonfaulty cases. In future, the interconnection pattern of IAON can be changed in such a way that it can produce better results in crucial faulty situations.

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