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Research Article

Near-Threshold Computing and Minimum Supply Voltage of Single-Rail MCML Circuits

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In high-speed applications, MOS current mode logic (MCML) is a good alternative. Scaling down supply voltage of the MCML circuits can achieve low power-delay product (PDP). However, the current almost all MCML circuits are realized with dual-rail scheme, where the NMOS configuration in series limits the minimum supply voltage. In this paper, single-rail MCML (SRMCML) circuits are described, which can avoid the devices configuration in series, since their logic evaluation block can be realized by only using MOS devices in parallel. The relationship between the minimum supply voltage of the SRMCML circuits and the model parameters of MOS transistors is derived, so that the minimum supply voltage can be estimated before circuit designs. An MCML dynamic flop-flop based on SRMCML is also proposed. The optimization algorithm for near-threshold sequential circuits is presented. A near-threshold SRMCML mode-10 counter based on the optimization algorithm is verified. Scaling down the supply voltage of the SRMCML circuits is also investigated. The power dissipation, delay, and power-delay products of these circuits are carried out. The results show that the near-threshold SRMCML circuits can obtain low delay and small power-delay product.

1. Introduction

High-speed circuits are now required in a wide range of applications such as high-speed processors and Gbps multiplexers for optical transceivers [1, 2]. In MOS current mode logic (MCML) techniques, the output swing of the circuits is much little than conventional CMOS ones, and thus the circuits realized with the MCML techniques can operate at a high speed [3, 4].

As CMOS process technology scales, the demand for more processing results in large power dissipations. It can be shown that the power dissipations of integrated circuits will increase over time if significant changes for the circuit architectures are not made. Scaling supply voltage is an efficient technique to achieve low power-delay product (PDP) [5]. The power dissipation of MCML cells is proportional to the product of their supply voltage and the biasing current, and thus it is independent of the operation frequency because of their constant biasing current. Therefore, the supply voltage of MCML circuits should be reduced as much as possible [6]. However, the current almost all MCML circuits are realized with dual-rail scheme [7–10]. The NMOS series configuration in the dual-rail logic circuits limits their minimum supply voltage. Moreover, the dual-rail logic circuits increase transistor counts, resulting in extra area overhead [11]. A single-rail structure of MCML circuits has been reported [11]. The single-rail logic circuits reduce the area overhead, and thus low delay can be expected. Moreover, the logic evaluation tree of the SRMCML cells such as AND and OR gates can be realized by only using MOS transistors in parallel. This can further reduce power dissipations because of their low source voltage [12].

In this paper, the analysis model for calculating minimum supply voltage of single-rail MCML (SRMCML) circuits is addressed, so that the minimum supply voltage of SRMCML circuits can be estimated according to the model parameters of MOS transistors. A dynamic flop-flop based on SRMCML is also proposed. The performance optimization algorithm for near-threshold sequential circuits is presented to optimize and improve the speed of the SRMCML circuits. An SRMCML mode-10 counter is verified.

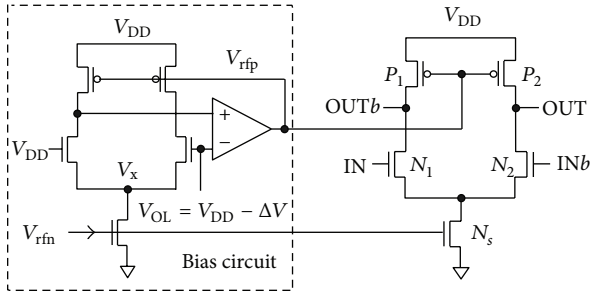


Figure 1: DRMCML inverter/buffer and its bias circuit.

This paper is organized as follows. In Section 2, the MCML circuits with dual-rail and single-rail structures are described, and the design methods of the basic single-rail MCML combinational logic cells are also presented. In Section 3, the analysis model for calculating minimum supply voltage of MCML circuits is addressed, and the relationship between the minimum supply voltage and the model parameters of MOS transistors is derived. In Section 4, a dynamic flop-flop based on the SRMCML is proposed, and the power dissipation, delay, and power-delay products of the proposed dynamic flop-flop are given. The performance metrics of the SRMCML circuits and the performance optimization algorithm are addressed in Sections 5 and 6, respectively. In Section 7, near-threshold SRMCML mode-10 counter is introduced, and the power dissipation, delay, and power-delay product of the mode-10 counter using the performance optimization algorithm are compared with basic SRMCML one. Finally, the work of this paper is summarized in the last section.

2. SRMCML Circuits

The basic dual-rail MOS current mode logic (DRMCML) buffer/inverter with its biasing circuit is shown in Figure 1, which is composed of three main parts: the PMOS transistors P_1 and P_2 that are used as load resistors, the evaluation tree with full differential pull-down switch network consisting of N_1 and N_2, and the biasing current source transistor N_s. The load transistors are controlled by the voltage V_{rfp} [3]. The NMOS transistor N_s provides the biasing current source, which is mirrored from the current source in the bias circuit. In the DRMCML, the bias circuit generates two signals V_{rfp} and V_{rfn} to ensure the proper output voltage swings and biasing current.

In DRMCML circuits, the pull-down network switches the biasing current between two branches, and then the loads (PMOS transistors) convert the constant current to output voltage swings. The high and low digital logic levels are $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - I_B R_D$, respectively, where R_D is the PMOS load resistance. The logic swing is $\Delta V = V_{OH} - V_{OL} = I_B R_D$.

DRMCML is a differential logic with dual-terminal inputs and dual-terminal outputs. The two-input and three-input AND/NAND and OR/NOR gates based on DRMCML are shown in Figure 3.

In almost all designs, the logic swing of DRMCML circuits is taken as $\Delta V < V_{th}$, this is because the NMOS transistor N_1 can operate at saturation region. For two-level DRMCML circuits, as shown in Figures 3(a) and 3(b), the logic transistor N_1 operates at saturation region, while the logic transistor N_2 operates at linear region. Therefore, the minimum supply voltage of two-level DRMCML circuits can been written as

$$V_{DD,min,two\text{-}level} = V_{1,gs} + V_{2,ds} + V_{s,sat}, \quad (1)$$

where $V_{1,gs}$ is gate-source voltage of the transistor N_1 at saturation region, $V_{2,ds}$ is drain-source voltage of the transistor N_2 at linear situation, and $V_{s,sat}$ is the drain-source voltage of the transistor N_s at velocity saturation point, respectively.

For three-level DRMCML circuits, as shown in Figures 3(c) and 3(d), the transistor N_1 operates at saturation region, while the transistors N_2 and N_3 operate at linear situation. Therefore, the minimum operating supply voltage of the three-level DRMCML circuits can be written as

$$V_{DD,min,three\text{-}level} = V_{1,gs} + V_{2,ds} + V_{3ds} + V_{s,sat}, \quad (2)$$

where $V_{1,gs}$ is gate-source voltage of the transistor N_1 at saturation region, $V_{2,ds}$ and $V_{3,ds}$ are drain-source voltages of the transistor N_2 at linear state, and $V_{s,sat}$ is the drain-source voltage of the transistor N_s at velocity saturation point, respectively.

Obviously, the NMOS series configuration of the logic tree in dual-rail MCML circuits limits the reduction of the minimum supply voltage. The dual-rail structure increases extra area overhead, because the complex valuation tree must be used. Moreover, the dual-rail structure increases complexity of the layout place and route.

A solution for the above problems is that MCML circuits are realized with single-rail structure, as shown in Figure 2 [12]. The SRMCML circuits are realized only using an NMOS pull-down network to perform the demanded logic operation. The output OUTb of the SRMCML is fed back the gate of the NMOS transistor N_2, which is different from DRMCML circuits. The basic SRMCML gates, such as buffer/inverter, two-input XOR/XNOR, and two-input and three-input OR/NOR and AND/NAND are shown in Figure 4.

Similar to DRMCML, the valuation of SRMCML circuits is performed in the current domain. The pull-down network switches the biasing current between two branches, and then the loads (PMOS transistors) convert the constant current to output voltage swings.

As shown in Figure 2, the structure of the single-rail MCML circuits is simpler than the dual-rail ones, because only a pull-down network is demanded. Therefore, the single-rail logic circuits reduce area overhead. Moreover, from Figure 4, the multi-input OR/NOR and AND/NAND cells based on SRMCML can be realized by only using MOS transistors in parallel and thus avoid the series configuration of the logic evaluation block in the multi-input DRMCML OR/NOR and AND/NAND cells. This structure can reduce power consumption of MCML circuits because of the low source voltage.

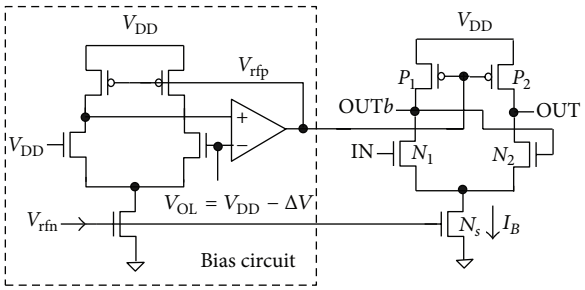


Figure 2: SRMCML inverter/buffer and its bias circuit.

3. Minimum Supply Voltage of SRMCML Circuits

Scaling down the supply voltage of SRMCML circuits can effectively reduce their power consumption, because their power dissipation is in direct proportion to the supply voltage. However, the supply voltage of the SRMCML circuits has a minimum limit, at which the biasing source transistor should operate at velocity saturation region, and the pull-down network NMOS transistors should be turn on. If the relationship between the minimum supply voltage and the model parameters of MOS transistors is derived, the minimum supply voltage of SRMCML circuits can be estimated before circuit designs.

As shown in Figure 4, the almost all basic SRMCML gates use single-level configuration except for the two-input XOR/NXOR. For two-level SRMCML circuits shown in Figure 5, the minimum supply voltage can beexpressed as (1), which is the same as two-level DRMCML circuits.

When the NMOS transistor operates at velocity saturation point, we can get its drain current $I_{d,\mathrm{sat}}$ and the drain-source voltage $V_{\mathrm{ds,sat}}$ expressed by the gate-source voltage V_{gs} according to the BSIM3 MOSFET model

$$I_{d,\mathrm{sat}} = W_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}} \left(V_{\mathrm{gs}} - V_{\mathrm{th}} - A_{\mathrm{bulk}} V_{\mathrm{ds,sat}}\right),$$
$$V_{ds,\mathrm{sat}} = \frac{E_{\mathrm{sat}} L_{\mathrm{eff}} \left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)}{A_{\mathrm{bulk}} E_{\mathrm{sat}} L_{\mathrm{eff}} + \left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)}, \tag{3}$$

where W_{eff} is the effective channel width of MOS device. C_{ox} is the gate capacitance per unit area, ν_{sat} is the carrier saturation velocity of the MOS device, E_{sat} is the critical electric field, and L_{eff} is the effective channel length of MOS device, respectively. A_{bulk} is the bulk charge effect that can be estimated from the simulation model card. If the channel length is small, A_{bulk} is about unity, and it rises as channel length is increased.

From (3), we can get $V_{\mathrm{ds,sat}}$ expressed by $I_{d,\mathrm{sat}}$ by eliminating parameter V_{gs},

$$V_{\mathrm{ds,sat}} = \frac{I_{d,\mathrm{sat}}}{2A_{\mathrm{bulk}} W_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}}} \times \left(\sqrt{1 + \frac{4A_{\mathrm{bulk}} W_{\mathrm{eff}} L_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}} E_{\mathrm{sat}}}{I_{d,\mathrm{sat}}}} - 1\right), \tag{4}$$

since a part of (4) satisfies

$$\frac{4A_{\mathrm{bulk}} W_{\mathrm{eff}} L_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}} E_{\mathrm{sat}}}{I_{\mathrm{ds,sat}}} \gg 1. \tag{5}$$

Equation (4) can be simplified as

$$V_{\mathrm{ds,sat}} = \sqrt{\frac{L_{\mathrm{eff}} E_{\mathrm{sat}} I_{d,\mathrm{sat}}}{A_{\mathrm{bulk}} W_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}}}}. \tag{6}$$

Again, from (3), we get V_{gs} expressed by $I_{d,\mathrm{sat}}$ by eliminating $V_{\mathrm{ds,sat}}$

$$V_{\mathrm{gs}} = V_{\mathrm{th}} + \frac{I_{\mathrm{ds,sat}}}{2W_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}}} \times \left(1 + \sqrt{1 + \frac{4A_{\mathrm{bulk}} W_{\mathrm{eff}} L_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}} E_{\mathrm{sat}}}{I_{\mathrm{ds,sat}}}}\right). \tag{7}$$

Equation (7) can be simplified as

$$V_{\mathrm{gs}} = V_{\mathrm{th}} + \sqrt{\frac{A_{\mathrm{bulk}} L_{\mathrm{eff}} E_{\mathrm{sat}} I_{d,\mathrm{sat}}}{W_{\mathrm{eff}} C_{\mathrm{ox}} \nu_{\mathrm{sat}}}}. \tag{8}$$

For the hand calculation, (6) and (8) are simpler and more convenient than (4) and (7).

According to the BSIM3 MOSFET model, when the NMOS transistor operates at linear state, its drain current $I_{d,\mathrm{lin}}$ is expressed as

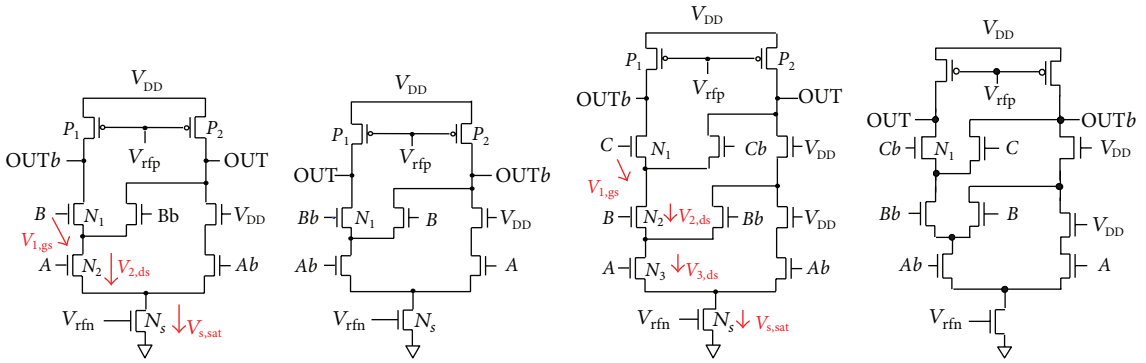
$$I_{d,\mathrm{lin}} = \mu_{\mathrm{eff}} C_{\mathrm{ox}} \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}} \left(V_{\mathrm{gs}} - V_{\mathrm{th}} - \frac{A_{\mathrm{bulk}} V_{\mathrm{ds,lin}}}{2}\right) V_{\mathrm{ds,lin}}, \tag{9}$$

where μ_{eff} is the effective mobility and $V_{\mathrm{ds,lin}}$ is the drain-source voltage. For the convenience of hand calculation, a part of the original equation has been omitted at the acceptable error range. From (9), we can get $V_{\mathrm{ds,lin}}$ expressed by $I_{d,\mathrm{lin}}$

$$V_{\mathrm{ds,lin}} = \frac{V_{\mathrm{gs}} - V_{\mathrm{th}}}{A_{\mathrm{bulk}}} - \frac{1}{A_{\mathrm{bulk}}} \sqrt{\left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)^2 - \frac{2A_{\mathrm{bulk}} L_{\mathrm{eff}} I_{\mathrm{ds,lin}}}{\mu_{\mathrm{eff}} C_{\mathrm{ox}} W_{\mathrm{eff}}}}. \tag{10}$$

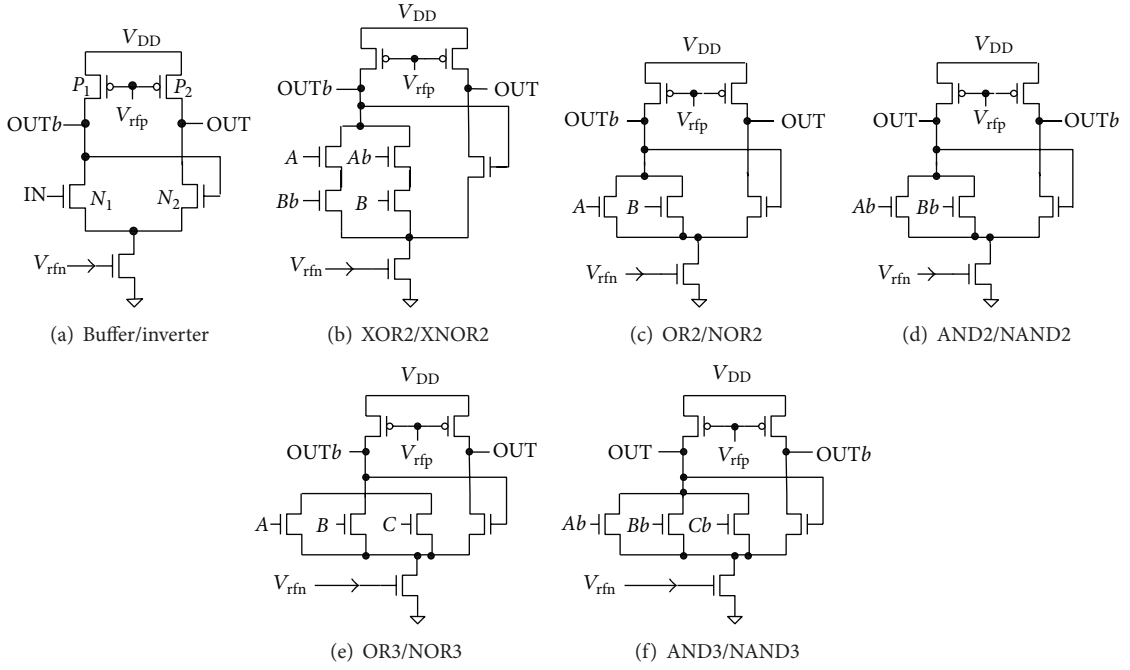
Substituting (10) into (1), applying parameters to the corresponding transistors in Figure 5, substituting $V_{2,\mathrm{gs}}$ with $V_{\mathrm{DD,min}} - V_{s,\mathrm{sat}}$, and then rearranging, we can arrive at the final equation of the minimum supply voltage of the 2-level SRMCML logic circuits which is

$$V_{\mathrm{DD,min,two\text{-}level}} = \frac{1}{2 - A_{2,\mathrm{bulk}}} V_{2,\mathrm{th}} - \frac{A_{2,\mathrm{bulk}} - 1}{2 - A_{2,\mathrm{bulk}}} V_{1,\mathrm{gs}} + \frac{1}{2 - A_{2,\mathrm{bulk}}} \times \sqrt{\left(V_{1,\mathrm{gs}} - V_{2,\mathrm{th}}\right)^2 + \left(2 - A_{2,\mathrm{bulk}}\right) \frac{2L_{2,\mathrm{eff}} I_B}{\mu_{\mathrm{eff}} C_{\mathrm{ox}} W_{2,\mathrm{eff}}}} + V_{s,\mathrm{sat}}. \tag{11}$$



(a) AND2/NAND2 (b) OR2/NOR2 (c) AND3/NAND3 (d) OR3/NOR3

Figure 3: Basic gates based on DRMCML.



(a) Buffer/inverter (b) XOR2/XNOR2 (c) OR2/NOR2 (d) AND2/NAND2

(e) OR3/NOR3 (f) AND3/NAND3

Figure 4: SRMCML gates.

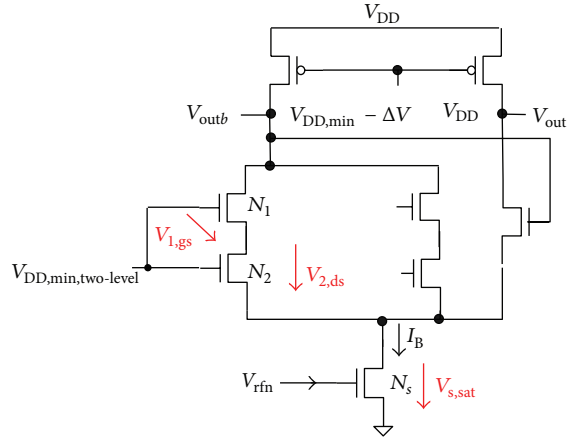


Figure 5: Operating supply voltage of two-level SRMCML circuits.

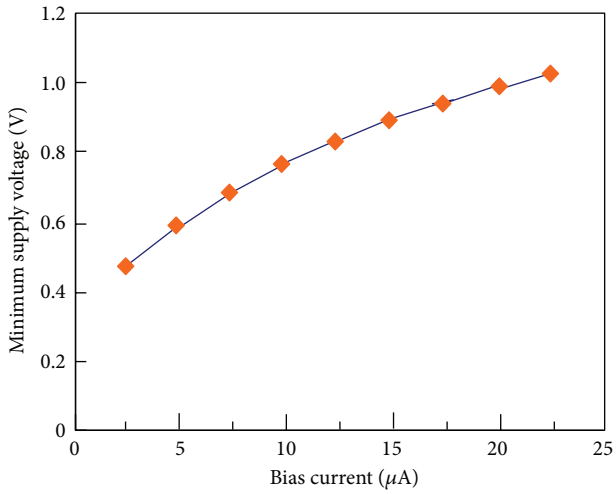


FIGURE 6: Minimum supply voltage of the two-level SRMCML logic circuits.

When $V_{s,\text{sat}}$ and $V_{1,\text{gs}}$ shown in (11) are estimated using (6) and (8), $I_{d,\text{sat}}$ should be replaced by the bias constant current I_B, and other model parameters should be substituted with the BSIM3 MOSFET model parameters of the corresponding transistors.

According to (11), the minimum supply voltage can be estimated. When the corresponding model parameters in (11) are substituted with actual values from the model card, the relationship of the minimum supply voltage $V_{\text{DD,min,two-level}}$ and the bias current I_B can be got, as shown in Figure 6.

If SRMCML circuits operate at a low speed, only a small I_B is required. Therefore, for low speed applications, a small I_B can be used. From Figure 6, the supply voltage can be reduced for low speed applications, so that more power saving can be obtained.

4. Dynamic Flop-Flop Based on SRMCML

A common approach for realizing D flip-flop (DFF) is to use a master-slave configuration. The DFF can be realized by cascading a negative latch (master stage) with a positive one (slave stage). The structure of the DFF based on SRMCML is shown in Figure 7, which is a dynamic positive edge-triggered one based on the master-slave configuration.

As is shown in Figure 7, when Clk = 0, the input data is sampled on the node A for storage. During this period, the slave stage of the SRMCML flip-flop is in a hold mode, while the node B of the slave stage is in a high-impedance state. On the rising edge of the clock, the transmission gate (T_2) of the slave stage is turned on, so that the value of node A, which is sampled right before the rising edge, propagates to the output Q. The node B stores the value of the node A.

This implementation of an edge-triggered flip-flop is very efficient because it requires only very small transistors. The reduced count of transistors is very attractive for low-power and high-speed digital applications.

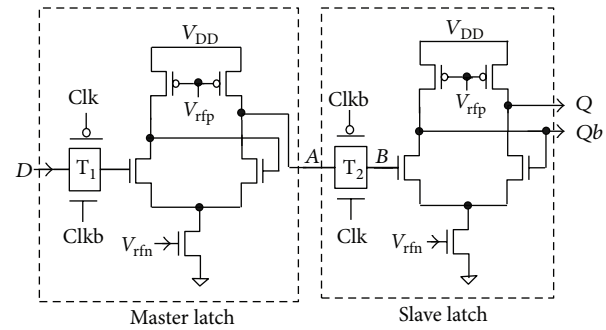


FIGURE 7: Dynamic D flip-flop based on SRMCML.

In order to investigate the performance of the SRMCML dynamic DFF, it has been simulated using HSPICE at the 130 nm CMOS process. The power dissipation and delay of the SRMCML dynamic DFF are shown in Figure 8.

Taken as references, the power dissipation and delay of the basic SRMCML gate cells are also shown in Figure 8. In these simulations, the device size of PMOS load transistors and biasing current source NMOS transistor in the SRMCML circuits is taken with $W/L = 8\lambda/10\lambda$ and $16\lambda/4\lambda$, and $\lambda = 65$ nm, respectively. The device size of NMOS transistors of the differential pair is taken with $4\lambda/2\ \lambda$. The threshold voltage V_{th} of the NMOS transistors is 0.282 V. The bias current of all the circuits is 8 μA. Since the power dissipation of the MCML circuits is almost independent of their frequency, the operation frequency is taken as 1 GHz.

From Figure 8, the power dissipations and delays of all the basic SRMCML gate cells are almost the same. It can be seen that the power dissipation and delay of the proposed SRMCML dynamic DFF are only slightly larger than the basic SRMCML gate cells.

In order to investigate the performance of the SRMCML dynamic DFF in near-threshold regions, the SRMCML dynamic DFF has been simulated using HSPICE by varying the source voltage ranging from 0.7 V to 1.3 V with 0.1 V step at the 130 nm CMOS process. The power-delay products of the SRMCML dynamic DFF are shown in Figure 9. From Figure 9, the power-delay products of the SRMCML dynamic DFF can be effectively reduced by lowering its source voltage.

5. Performance Parameters of SRMCML Circuits

This section focuses on the performance of the SRMCML gates as a function of numerous design parameters. In order to optimize the performance of the SRMCML gates, some metrics of performances should be determined. These performance metrics for the SRMCML gates consist of hard constraints and optimization goals. The hard constraints including gain, voltage swing ratio (VSR), and signal slope ratio (SSR) must not be violated. Optimization goals including power dissipation and power-delay product should be minimized or maximized.

The performance parameters for a typical SRMCML circuit are voltage gain A_V, voltage swing ratio (VSR), signal

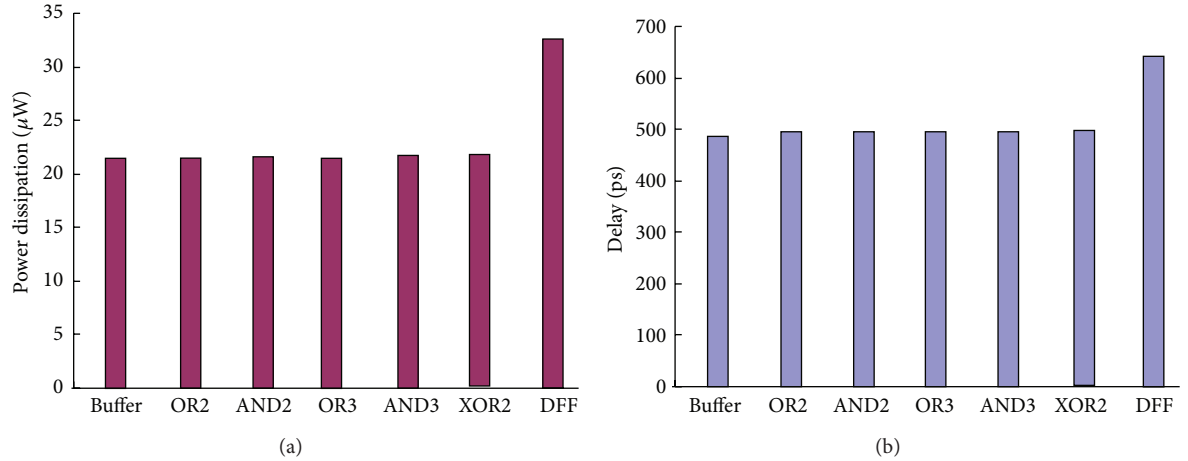


Figure 8: Power dissipation and delay of SRMCML cells. (a) Power dissipation and (b) delay.

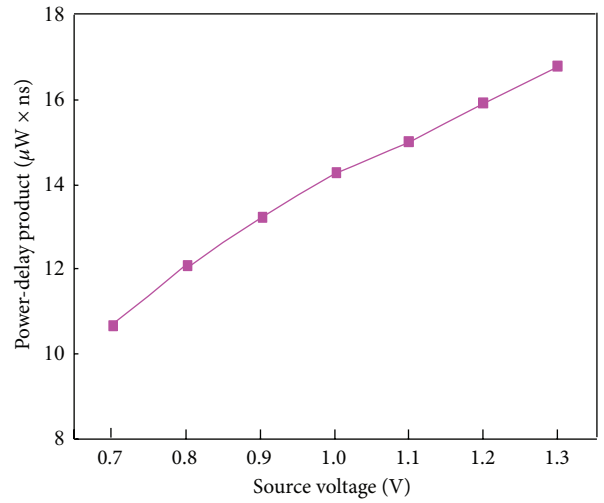


Figure 9: Power-delay products of the dynamic DFF based on SRMCML.

slope ratio (SSR), current matching ratio (CMR), noise margin (NM), voltage swing (ΔV), power dissipation P, delay time t_d, and power-delay product (PDP) [9, 10, 13].

5.1. Voltage Gain (A_V). The voltage gain A_V is defined as the max voltage gain of the MCML circuits. It is a key parameter for regenerating and stability of the MCML circuit. For SRMCML, A_V is expressed as

$$A_V = g_m R_D = \Delta V \sqrt{u_n C_{\mathrm{OX}} \frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}} I_B}}, \tag{12}$$

where g_m is transconductance, C_{OX} is oxide capacitance of the transistors, u_n is electron mobility, and W_{eff} and L_{eff} are effective width and length of the transistors, respectively.

It is obvious that the voltage gain A_V must be greater than 1 for all process and voltage deviations. A 40% margin would be sufficient for those variations in process, voltage, and matching conditions. Therefore, the lower limit of the voltage gain A_V in our work is set as 1.4.

5.2. Voltage Swing Ratio (VSR). The ideal operation of MCML circuits is a perfect current switch, where all the current flows down into one branch or the other. In reality, a little amount of the biasing current flows in the "off" path, resulting in a reduction in the output voltage swing. We set this constraint that the output voltage swing must be at least 95% of the applied input voltage.

5.3. Signal Slope Ratio (SSR). Since the speed of the MCML gate depends not only on the propagation delay but also on the output waveform shape of the previous gate, the reasonable rise and fall time must be ensured. The signal slope ratio SSR used in the work is defined as the ratio of rise and fall time (T_{rf}) and propagation delay (t_d)

$$\mathrm{SSR} = \frac{T_{\mathrm{rf}}}{t_d}. \tag{13}$$

This metric should be kept as low as possible. We set this constraint as an absolute limit of 5.

5.4. Current Matching Ratio (CMR). This constraint is the current amount flowing through the actual current source in comparison to the reference biasing current source. In order to achieve design predictability, the actual current should be close to the reference biasing current. The most main parameter that affects this ratio is the output impedance of the biasing current source (the transistor N_S) and its drain-source voltage.

5.5. Noise Margin (NM). A sufficiently large noise margin (NM) in SRMCML circuits should been achieved because of reduced voltage swings. NM is given by

$$\mathrm{NM} = \Delta V \frac{\sqrt{4A_V^2 - 1 - \sqrt{8A_V^2 + 1}}}{A_V^2\sqrt{2}} \times \frac{\sqrt{4A_V^2 + 1 + \sqrt{8A_V^2 + 1}}}{2\sqrt{2}}. \tag{14}$$

The high noise immunity of SRMCML circuits can accept small NM values. Practically, an NM of 40% swing voltage (ΔV) is sufficient to ensure proper operation of SRMCML circuits without the performance degrading.

5.6. Voltage Swing (ΔV). For the SRMCML circuits, the logic swing ΔV should be correctly selected. For Figure 4(a), the logic low voltage must be enough high, so that the NMOS transistors N_1 and N_2 work in the saturation state, and thus it can be written as

$$V_{\mathrm{DD}} - (V_{\mathrm{DD}} - \Delta V) < V_{\mathrm{TH,N_1}} \Longrightarrow \Delta V < V_{\mathrm{TH,N_1}}, \tag{15}$$

where $V_{\mathrm{TH,N_1}}$ is the threshold voltage of the NMOS transistors N_1 and N_2. At the same time, the logic low voltage ($V_{\mathrm{DD}}-\Delta V$) must be low enough, so that the input NMOS transistor of the next SRMCML circuits can be shut down reliably

$$(V_{\mathrm{DD}} - \Delta V) - (V_{\mathrm{DD}} - V_{\mathrm{gs,sat}}) < V_{\mathrm{TH,N_1}} \Longrightarrow \Delta V > V_{\mathrm{gs,sat}} - V_{\mathrm{TH,N_1}}, \tag{16}$$

where $V_{\mathrm{gs,sat}}$ is the gate-source voltage of the on-turn transistor N_1. The similar analysis can be carried out for the other SRMCML gates shown in Figure 4, and the same conclusions as (15) and (16) can be obtained.

5.7. Power Dissipation (P) and Delay Time (T_d). Similar to the DRMCML circuits, the important performance metrics of the SRMCML gates include power consumption, propagation delay, and power-delay product. Due to the constant biasing current, for given V_{DD} and I_B, the power consumption of an SRMCML gate is almost independent of the switching frequency, logic function, and fanouts. It can be written as

$$P = V_{\mathrm{DD}} I_B. \tag{17}$$

```
for 0.5 uA ≤ I_B ≤ 100 uA
    {for 200 mV ≤ ΔV ≤ 1.3 V
        {initialize V_DD = 1.3 V
          for 0.13 um ≤ LRFP ≤ 1.3 um
        {Find smallest W_1, W_2 which satisfy:
                0.26 um ≤ W_1, W_2 ≤ 2.6 um,
                Gain > 1.4,
                Voltage Swing Ratio > 0.95,
                Signal Slope Ratio < 5,
                if above is possible,
                then store parameters
              }
          Find LRFP which gives I_B and ΔV
        }
    Find ΔV which gives I_B
     Store value of I_B, ΔV, W_1, W_2, LRFP
    }
```

Algorithm 1: Optimization procedure of SRMCML circuits.

Assuming that the whole I_B ideally flows through one branch of the differential pair and charges the load capacitance C of the SRMCML gate, its delay time is given by

$$t_d = 0.69 \cdot R_D C = \frac{0.69 \cdot C \cdot \Delta V}{I_B}, \tag{18}$$

where C is load capacitance on the output node. From (18), the delay of the SRMCML gate is linearly reduced as the signal swing decreases.

The power-delay product can be calculated as

$$\mathrm{PDP} = P \cdot t_d = 0.69 V_{\mathrm{DD}} \cdot \Delta V \cdot C. \tag{19}$$

6. Performance Optimization Algorithm for SRMCML Circuits

The relationships between performance metric and design parameters include several aspects.

(a) We should construct the mathematical model among delay time, power dissipation, and device dimension.

(b) For a given A_V, we need to get the operating current of the SRMCML gate, so that the value of power dissipation is the optimal one.

(c) We need to determine the device dimension by the biasing current.

The first step in the optimization algorithm is to initialize the $V_{\mathrm{DD}} = 1.3$ V. For a number of discrete values of I_B ranging from 0.5 uA to 100 uA, we try to find the channel widths of the PMOS load transistors, full differential pull-down network consisting of N_1 and N_2, and the biasing current source N_s. In the next loop in the optimization algorithm, we try to find the ΔV. For each I_B, we choose and fix a ΔV. In the third loop in the optimization, we choose and fix the length of the PMOS loads. Finally, within each iteration, we choose and fix the best width of the differential pull-down switch network.

This optimization procedure is illustrated in Algorithm 1. In Algorithm 1, *LRFP* is the length of the PMOS transistors P_1

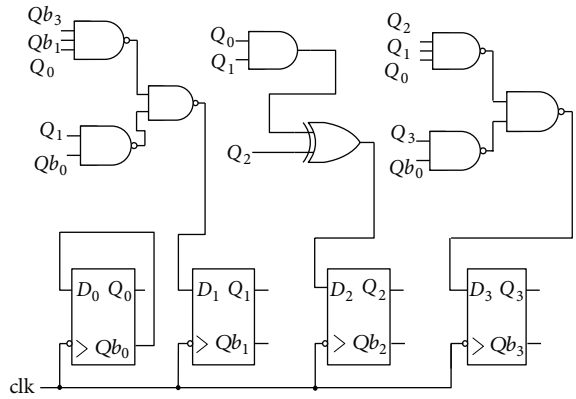


Figure 10: The SRMCML mode-10 counter.

and P_2 and W_1 and W_2 are the widths of the NMOS transistors N_1 and N_2.

By carrying out the performance optimization algorithm, we can obtain the optimal values of I_B, ΔV, the length of *LREF* of the PMOS transistors, and the width of the NMOS transistors N_1 and N_2.

7. Simulations and Analyses

In this section, the near-threshold mode-10 counters are realized using basic SRMCML and the optimization algorithm. The influences of process and temperature variations for the SRMCML circuits are analyzed. The conventional static CMOS mode-10 counter is used for comparing the performances with SRMCML ones in terms of power, delay, and power-delay product.

The structure of the decimal counter based on SRMCML is shown in Figure 10. The decimal counter consists of NAND2, NAND3, and dynamic DFF. The device size of PMOS load transistors and biasing current source NMOS transistor is taken with $W/L = 8\lambda/10\lambda$ and $16\lambda/4\lambda$, respectively. The device size of NMOS transistors of the SRMCML is taken with $4\lambda/2\lambda$ and $\lambda = 65$ nm.

The SRMCML dynamic DFF and decimal counter based on the performance optimization are stimulated by using HSPICE at the 130 nm CMOS process. The simulation frequency of all the MCML circuits is 1 GHz.

The performances of the circuits would be sensitive to process and temperature variations, especially in low supply voltages. As mentioned in Section 5, in the designs of SRMCML circuits, the sufficient margin of the hard constraints including gain, voltage swing ratio (VSR), and signal slope ratio (SSR) must be set for those variations in process, voltage, and matching conditions.

The worst case corner simulations for the SRMCML mode-10 counters have been carried out to take process variations into account. Considering temperature variations, the circuits have also been simulated in operating temperature ranging from 4°C to 60°C. The results show that the SRMCML mode-10 counters have correct logic function for worst case corner simulation and temperature variations in the source voltages ranging from 0.7 V to 1.3 V.

According to (11), the minimum supply voltage of the SRMCML circuits depends on the model parameters of the corresponding MOS transistors. Therefore, the process and temperature variations would affect the minimum supply voltage because of the variation of these MOS transistors. The worst case corner simulations show that the process variations result in about 5.7% reduction of the minimum supply voltage of the SRMCML mode-10 counters. In the operating temperature ranging from 4°C to 60°C, the minimum supply voltage of the SRMCML mode-10 counters has about 7.6% error compared with the value estimated according to (11).

The comparison results of the power dissipation and delay of the SRMCML decimal counters are shown in Figure 11. From Figure 11(a), the power dissipations of the SRMCML mode-10 counters based on the basic SRMCML and using the optimization algorithm are almost the same. Just as shown in (17), the power dissipation of the SRMCML decimal counters decreases linearly with supply voltage scaling down.

Figure 11(b) shows that the SRMCML mode-10 counter using the performance optimization algorithm attains lower delay than basic SRMCML. According to (18), the delay of SRMCML circuits is independent of the source voltage. Since the delay of the two transmission gates (T_1 and T_2) in the dynamic flip-flops of the SRMCML counters increases with supply voltage scaling down, therefore, the total delay of the SRMCML mode-10 counters slightly rises with supply voltage scaling down.

For comparison, the mode-10 counter based on the conventional static CMOS using the transmission gate flip-flop with master-slave construction has been also simulated at the same CMOS technology. Their power dissipations and delay have been compared with SRMCML ones, as shown in Figure 11. Just as expected, the delay of SRMCML counters is mush smaller than the conventional static CMOS one, and thus SRMCML can operate in higher speed than CMOS.

From Figure 11(a), the power consumption of SRMCML mode-10 counters is higher than the static CMOS one. Although the static CMOS mode-10 counter consumes much lower power than SRMCML ones in low source voltage, its delay rises dramatically with supply voltage scaling down.

The power-delay product metric provides a good tradeoff between power and delay features. The power-delay products

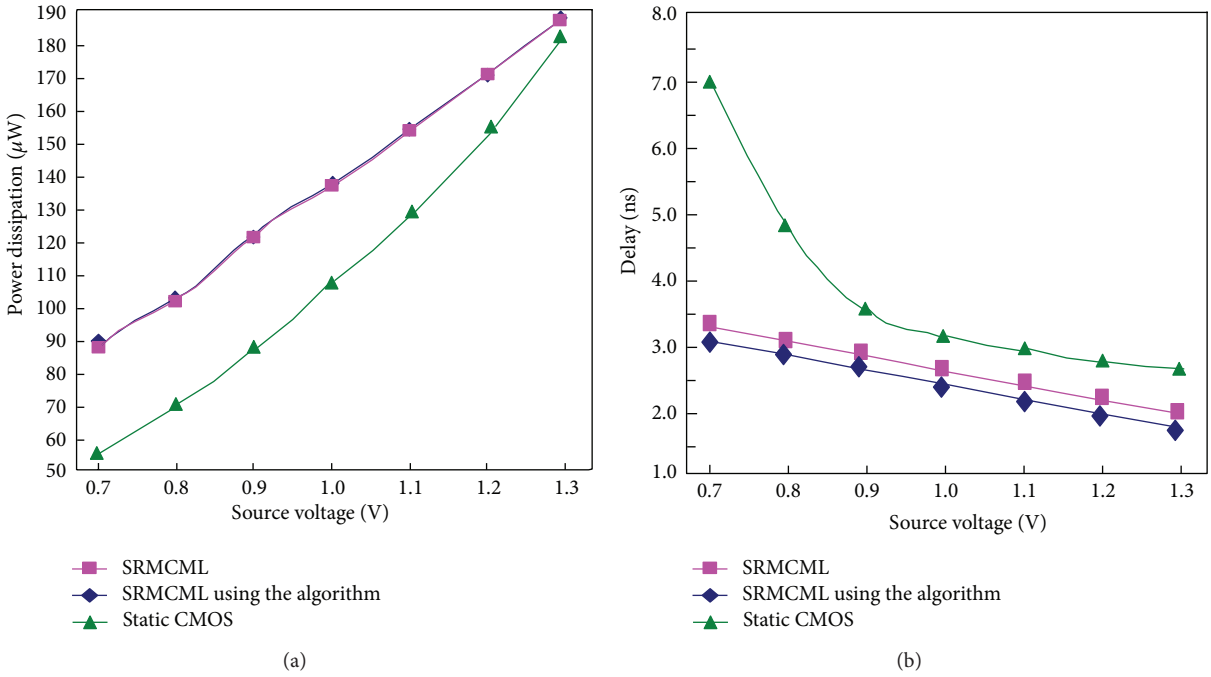


Figure 11: Power dissipation and delay of the mode-10 counter based on SRMCML. (a) Power dissipation and (b) delay.

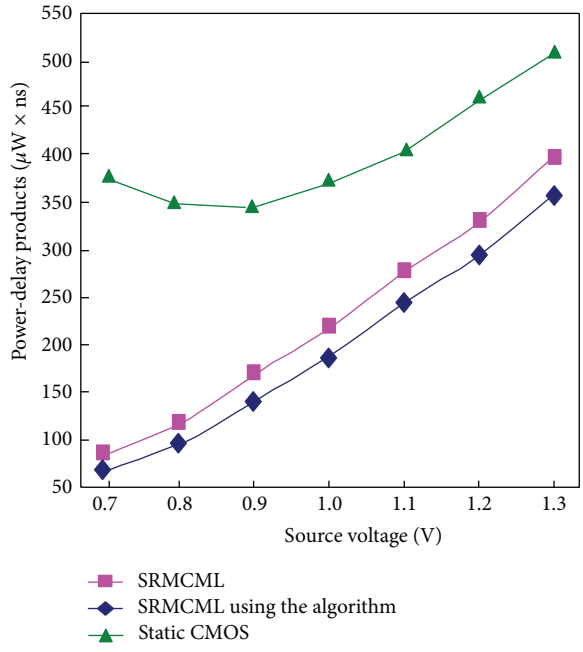


Figure 12: Power-delay products of the mode-10 counter.

of the SRMCML and static CMOS decimal counters are compared in Figure 12. From Figure 12, it can be seen that the power-delay products of the SRMCML using the performance optimization algorithm are smaller than the basic SRMCML because of the reduced circuit delay. The SRMCML mode-10 counters attain lower PDP than conventional static CMOS, especially in low source voltages.

8. Conclusions

Scaling down the supply voltage of single-rail MOS current mode logic (SRMCML) circuits can effectively reduce their power consumption, because their power dissipation is in direct proportion to the supply voltage. However, the supply voltage of the SRMCML circuits has a minimum limit for

ensuring the proper operation. In this work, the analysis model for calculating minimum supply voltage of SRMCML circuits is addressed. The relationship between the minimum supply voltage and the model parameters of MOS transistors has been derived, so that the minimum supply voltage of SRMCML circuits can be estimated before circuit designs.

An MCML dynamic flop-flop based on SRMCML structure is also addressed in this work. The optimization algorithm for the near-threshold computing of the SRMCML circuits is proposed. Scaling down the supply voltage of the SRMCML circuits is investigated. The comparisons of power dissipation, delay, and power-delay products of these circuits are carried out. The results show that the near-threshold SRMCML circuits can obtain low delay and small power-delay product compared with the conventional static CMOS one.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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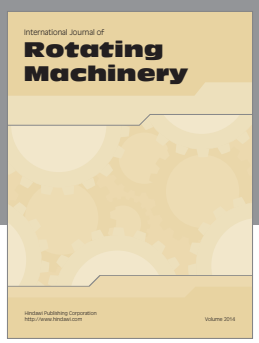

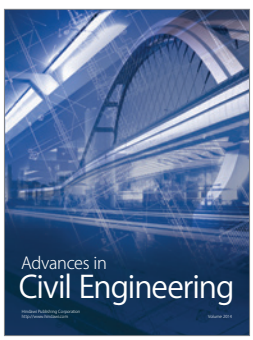

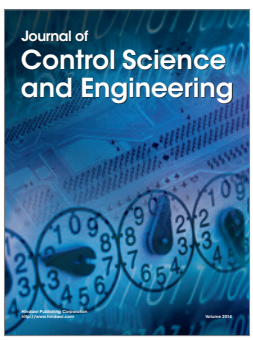

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