Research Article

Design and Analysis of a Low Cost Wave Generator Based on Direct Digital Synthesis

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Signal generators are widely used in experimental courses of universities. However, most of the commercial tests signal generators are expensive and bulky. In addition, a majority of them are in a fixed working mode with many little-used signals. In order to improve this situation, a small sized and highly accurate economic signal generator based on DDS technology has been developed, which is capable of providing wave signals commonly used in experiments. Firstly, it is introduced the basic principles of DDS and is determined the overall scheme of the signal generator. Then, it proposes a design of the hardware, which include power supply module, display module, keyboard module, waveform generating module based on DDS chip, and the minimum system module based on C8051F010. The signal generator was designed to output sine and square waveforms, and the other achieved performances included the frequency range 0.1 Hz–12.5 MHz, the frequency resolution 0.05 Hz–0.1 Hz, the output amplitude 1.0–4.5 V, the frequency accuracy $K_{f_{\min}} = 94.12\%$ and $K_{f_{\max}} = 99.99\%$, and the signal distortion $R_{\text{THDmin}} = 0.638\%$ and $R_{\text{THDmax}} = 11.67\%$.

1. Introduction

Signal generators are widely utilized in experimental courses [1–8]. Furthermore, square wave and sine wave signals generated by signal generators are extensively used in a wide range of applications, usually as a standard signal in electronic circuit testing, parameter measurement, or demonstration in experimental courses. However, due to the high cost, fixed working mode and poor extensibility combine the programmable functions for generating arbitrary waveforms and other functions cannot be fully played out in the teaching experiments of common signal generator; a cheap and small signal generator which can meet common signal output functions and be suitable for experimental courses was needed [9–12]. Based on DDS technology, an economic signal generator with small size and high precision was developed. Square wave signal with tunable frequency, pulse width, and duration and high precision sine signal with adjustable amplitude and frequency can be produced to satisfy the requirements in teaching experiments. Some reports focus on developing signal generator by DDS technology in theory. There are still

few reports about manufacturing of the signal generator by DDS technology.

2. The Overall Design Scheme of the Signal Generator

2.1. Basic Principle of DDS Technology. The basic principle of DDS is using the phase concept to carry out frequency synthesis [2], which allows signals changing with phase to be obtained according to the variation of given signals under different amplitude. Phase accumulator is formed by cascaded N -bit adder with N -bit accumulator register. For each arriving clock pulse f_{MCLK} , the adder sums up the control word (M) with the accumulated phase data produced by the phase accumulator register, and the result is sent back to the input port of the accumulator register, so that the adder continuously sums up the frequency control word under the effect of the subsequent clock pulse. The phase adder continuously performs linear adding of the frequency control word in an accumulative fashion under the effect of

FIGURE 1: Diagrammatic sketch of the operating principle of phase accumulator.

the clock input. As shown in Figure 1, a sine wave is regarded as oscillation of a phase cycle in a rotating vector manner, and each given point on the phase wheel corresponds to an angular division point on a sine wave in a $0 \sim 2\pi$ cycle. Every time a vector turns around a phase circle at a constant speed, a complete cycle of sine wave is produced. It can be seen that the phase accumulator adds the control word once following each clock input, the output data of the phase accumulator is the phase of the synthesized signal, and the output frequency of the phase accumulator is the signal frequency of the DDS output. The frequency control word determines the number of division points that can jump on the phase cycle in each time clock cycle. More division points lead to faster overflow of the phase accumulator and shorter time to complete equal sine wave cycles; thus changing the value of the control word (M) can alter the output frequency [4]. The output data of the phase accumulator serves as the phase sampling address of a waveform memory (ROM). A phase/amplitude conversion is completed after retrieving the binary waveform sample values stored in the waveform memory using a lookup table.

2.2. The Overall Program Design of Signal Generator. The functional structure of the signal generator block diagram, as shown in Figure 2, mainly consists of a power supply system,

FIGURE 2: Block diagram of the signal generator based on DDS.

SCM system, DDS waveform generator module, amplitude adjustment module, square wave generator module, relay output module, and so on. The power supply system provides 2.5 V, 3.3 V, ± 5 V, and ± 15 V power supply voltage. The +5 V input of the power supply system goes through an integrated three-terminal voltage regulator to obtain 2.5 V and 3.3 V voltage and then uses a DC-DC power supply module for conversion to +5 V and +15 V. The SCM system is employed to control the operation of the human-machine interface, read keyboard, display on LCD, and adjust the output sine wave amplitude. It also undertakes programming of the DDS device to produce the corresponding frequency signal, to control the relays and switch sine and square wave outputs.

3. Hardware Design of the Signal Generator

3.1. Design of the Power Supply Circuit. As shown in Figure 3, the inputs and outputs of AS1117-2.5, AS1117-3.3, and the DC-DC module use 330 μ F and 0.1 μ F capacitors for frequency compensation, to prevent the regulator from generating high-frequency self-excited oscillation and to suppress high-frequency interference in the circuit. The output terminals of the A05S05-2W and A05S15-1W power modules have resistors and capacitors to form a low-pass filter, which can smooth power output spikes and reduce interference to the subsequent circuit chip. The reverse protection design is also used in the power supply circuit, where a diode D3 is in cut-off state under normal power supply. If the input voltage is reversed, the diode conducts and the current from the external power supply flows through the FUSE and diode D3 into the negative terminal of the power supply. Since the diode forward resistance is very small, the current increases sharply and burns out the FUSE, disconnects the circuit, and thus protects the internal circuit from being damaged.

3.2. Design of LCD Module. The liquid crystal display module was built on LCM1602 that has 2×16 characters and internal font. The interface is shown in Figure 4, where R_{12}

FIGURE 3: Circuit of the power supply.

potentiometer can be used to adjust the potential of feet 3 to change the contrast of the LCD display.

3.3. Design of Keyboard Circuit. The front panel of the signal generator is shown in Figure 5. By means of pressing the left or right buttons to select each bit of data to be transferred and then using add or subtract settings, the number of buttons can be reduced and remained the same when the data for transmission needs to be extended. This allows the circuit to be very flexible since appropriate changes can be made in the software. The circuit output functions can be selected by “sine/square wave” buttons. The output signal frequency can be configured under a square wave output state, whilst for a sine wave output state, the signal frequency or amplitude can be set or modified through the “Mode” button.

As shown in Figure 6, the “sine/square wave” is designed with a locking switch, whilst the “Add,” “Reduce,” “Shift left,” “Shift right,” and “Mode” buttons are designed without locking switch. The output is high level 3.3 V when SW1~SW5 are released and low level when pressing them. When Switch6 is released, PIN2 connects to PIN3 and PIN5 connects to PIN6, while PIN1 is hanging, SIN/REC is high level, and LED_SIN lights up, indicating the output is sine wave. When it is pressed, SIN/REC is low level, and PIN4 connects to PIN6, and LED_REC lights up, showing the output is squared wave signals.

3.4. The Circuit Design of Wave Generator

3.4.1. The Circuit Design of Sine Wave Generator. As is shown in Figure 7, the signal generator is based on a DDS chip

FIGURE 4: The interface circuit of LCD.

FIGURE 5: The shifting keyboard panel design.

AD9833 made by Analog Devices, Inc. (ADI), which is 25 MHz with active crystal as a reference clock.

3.4.2. Design of the Sine Wave Amplitude Modulation Circuit. According to the required sinusoidal amplitude which is input by the keyboard, the D/A port of the microcontroller produces a corresponding DC signal, then feeds it to the multiplier, and multiplies it with a fixed amplitude sinusoidal signal, to achieve the function of regulating the amplitude, as shown in Figure 8.

The multiplier is selected to be MPY634, which is powered by ± 15 V voltage, and can adopt a single-ended input (± 10 V) or a differential input (± 11 V), while the output voltage can reach ± 11 V. The relation of output voltage and input voltage is given by

$$V_{\text{out}} = A \left(\frac{(x_1 - x_2)(y_1 - y_2)}{\text{SF}} - (Z_1 - Z_2) \right). \quad (1)$$

Since the multiplier has internal negative feedback and V_{out} is limited, the amplification factor (A) is infinite in theory and is at least 85 dB in practice; therefore,

$$\frac{(x_1 - x_2)(y_1 - y_2)}{\text{SF}} - (Z_1 - Z_2) = 0. \quad (2)$$

The sinusoidal wave amplitude ranges from 0.038 V to 0.650 V; thus the DC component (V_o) is 0.344 V. The output from the multiplier must be the sine wave without DC component, so the DC component should be subtracted using circuit shown in Figure 8. The resistor R_{27} is linked

between port Z_1 and port OUT, and resistor R_{26} is linked between ports Z_1 and Z_2 .

Assuming the resistances of R_{26} and R_{27} are x and y , then

$$Z_1 - Z_2 = V'_{\text{out}} * \frac{y}{x + y}. \quad (3)$$

V'_{out} is the output voltage of multiplier, and the following can be concluded:

$$\frac{(x_1 - x_2)(y_1 - y_2)}{\text{SF}} = V'_{\text{out}} * \frac{y}{x + y}. \quad (4)$$

Therefore,

$$V'_{\text{out}} = \frac{x + y}{y} * \frac{(x_1 - x_2)(y_1 - y_2)}{\text{SF}}. \quad (5)$$

Assuming that

$$K_0 = \frac{x + y}{y} * \frac{1}{\text{SF}}. \quad (6)$$

K_0 is the gain of the multiplier of the two differential inputs,

$$V'_{\text{out}} = K_0 * (x_1 - x_2)(y_1 - y_2). \quad (7)$$

The current of the multiplier output cannot output directly because of its weakness of driving power, so a high speed operational amplifier must be set before the input of the multiplier to increase the output current.

FIGURE 9: The circuit of offset voltage of the amplifier.

Taking $R_{30} = 2 \text{ K}\Omega$, $R_{31} = 1 \text{ K}\Omega$, $R_{32} = 1 \text{ K}\Omega$, the amplifier multiple is $A = 1 + R_{31}/R_{30} = 3$; then

$$V_{\text{out}} = 3 * V'_{\text{out}} = 3K_0 * (x_1 - x_2)(y_1 - y_2). \quad (8)$$

The output voltage of DAC of the MCU is ranging from 0 to 2.4 V and the sinusoidal waveform of DDS is ranging from 0 to 0.65 V, so the DC component of sinusoidal waveform (V_o) is 0.344 V.

Reducing the DC component at Y input of MPY634, the amplitude of sinusoidal waveform is

$$V_{\text{in}} = V_{\text{dds}} - V_o = \pm 0.306 \text{ V}. \quad (9)$$

Multiplying the two differential inputs X and Y gives $2.4 * 0.306 = 0.7344$, so it is required to get the amplitude of sinusoidal waveform more than 4 V; the gain must be chosen above $4/0.7344 = 5.4$.

The way of the circuit connection decides the value of 1/SF.

When Port SF is hanging, the amplification factor is SF = 10 V which is accurately modified by laser in the integrated circuit and the error is 0.1% or less.

Through resistor R_{SF} linking between PIN SF and PIN $-V_S$, the value of SF can be changed:

$$R_{\text{SF}} = 5.4 * \left(\frac{\text{SF}}{10 - \text{SF}} \right). \quad (10)$$

Defining $x = 136 \text{ K}\Omega$, $y = 4 \text{ K}\Omega$, then

$$K = 3 * K_0 = 3 * \frac{x + y}{y} * \frac{1}{\text{SF}} = 10.5 \quad (11)$$

$$V_{\text{out}} = 10.3 * (x_1 - x_2)(y_1 - y_2)$$

$$V_{\text{outMax}} = 10 * 2.4 * (\pm 0.306) = \pm 7.3 \text{ V}.$$

Because of the amplifier providing $\pm 5 \text{ V}$ in practice, the output voltage can only reach about $\pm 4.5 \text{ V}$.

The amplitude of sinusoidal waveform ranges from 0.038 V to 0.650 V and its DC component is 0.344 V, which is obtained by resistor divider. As shown in Figure 9, the AS1117-2.5 three-port voltage stabilizer provides the voltage of 2.5 V, providing the offset voltage of 0.344 V through resistor dividing.

Taking $R_1 = 60 \text{ K}\Omega$, $R_2 = 10 \text{ K}\Omega$, $R_3 = 10 \text{ K}\Omega$, the output scope of reference voltage is

$$V_{\text{ref0min}} = 2.5 * \frac{R_3}{R_1 + R_2 + R_3} = 0.3125 \text{ V} \quad (12)$$

$$V_{\text{ref0max}} = 2.5 * \frac{R_2 + R_3}{R_1 + R_2 + R_3} = 0.6250 \text{ V}.$$

Therefore, the output scope of reference voltage ranges from 0.3125 V to 0.6250 V, and it is possible through adjusting potentiometer to get the offset voltage of 0.344 V. Therefore it is possible to eliminate the DC component of sinusoidal waveform from DDS output. Introducing a positive feedback to the circuit constitutes a hysteresis comparator, through adding a branch of voltage divider from comparator output to in-phase input. This can be seen from the schematic in Figure 10(a).

When input voltage V_I is gradually increased from zero but is less than or equal to V_T , which is called ceiling trigger level, $V_o = V_{\text{om}}^+$,

$$V_T = \frac{R_1 V_{\text{REF}}}{R_1 + R_2} + \frac{R_2}{R_1 + R_2} V_{\text{om}}^+. \quad (13)$$

When the input voltage V_I is greater than V_T , $V_o = V_{\text{om}}^-$, and the triggering level is changed into V_T' which is called the lower trigger level:

$$V_T' = \frac{R_1 V_{\text{REF}}}{R_1 + R_2} + \frac{R_2}{R_1 + R_2} V_{\text{om}}^-. \quad (14)$$

FIGURE 10: Principle of the hysteresis comparator.

FIGURE 11: The circuit of generating square waveform.

The threshold voltage is

$$\begin{aligned}\Delta V &= V_T - V'_T = \frac{R_2}{R_1 + R_2} V_{om}^+ - \frac{R_2}{R_1 + R_2} V_{om}^- \\ &= \frac{R_2}{R_1 + R_2} (V_{om}^+ - V_{om}^-).\end{aligned}\quad (15)$$

From Figure 10(b) of voltage transmission characteristics of the hysteresis comparator, it can be seen that the comparison voltage is different between the direction of increment and the direction in input voltage, and the interference within the hysteresis range will not affect the output voltage.

The circuit of generating square waveform is shown in Figure 11. Port V_{REF} provides 2.5 V voltage for the voltage regulator module, the voltage can be regulated by adjusting a potentiometer, and the comparator outputs about 4 V of high level. So the backlash voltage of the circuit is

$$\Delta V = \frac{R_9}{R_{33} + R_9} (V_{om}^+ - V_{om}^-) \approx 40 \text{ mV}.\quad (16)$$

3.5. The Design of Controlling Circuit of Relay Output. As shown in Figure 12, the relay module UA2 is equivalent to a double-pole double-throw switch. The control sides PIN1

and PIN8 are, respectively, connected to the +5 V supply and sine/square waveform changeover switch, PIN2, PIN3, PIN4 are the switch for final wave output switching, and PIN6, PIN7, PIN8 are the switch for shifting sine wave to hysteresis comparator to produce a square wave. Diode D1 is for current limiting to prevent excessive current impact on the circuit.

When the sine/square waveform switch is released, SIN/REC becomes high level, and there is no current through the relay coil or the current is very small, which means that it does not produce magnetic force. The connection of PIN6 and PIN7 will put the sinusoidal signal into the comparator to create square waveform. Then, the square signal will input into PIN2 of the decay, which would sent to external interface because of the connection of PIN2 and PIN3. When the sine/square waveform switch is pressed, SIN/REC changes to low level; thus the relay coil generates a magnetic force. The connection of PIN5 and PIN6 separates the sine wave signal from the comparator to prevent generating interference. The connected PIN4 and PIN3 deliver the sine signal generated from the amplitude to the external output interface.

3.6. The Design of MCU Controlling Circuit. As shown in Figure 13, a CYGNAL C8051F series MCU was chosen to

FIGURE 12: The circuit of relay controller.

FIGURE 13: The controlling circuit of MCU.

implement the functions of reading keyboard, displaying LCD, programming DDS chip, and adjusting the amplitude of the sinusoidal signal. Considering the rules of microcontroller pin configuration, the internal digital resources start from P0 port; therefore when assigning peripheral device port, the MCU starts assigning from P3 port to reserve P0 port for the internal resources.

3.7. The Deployment of PCB and Anti-Interference Design.

Because of the hybrid-system of digital circuit and analog circuit, and its high operating frequency, much attention should be put to the deployment of PCB and its anti-interference design. Considering the cost and the size, the PCB board is designed with double-layer plate and double wiring. Separate the digital circuit and analog circuit in PCB

FIGURE 14: The PCB design diagram of AD9833.

FIGURE 15: The whole PCB design diagram.

layout and wiring. In general, we should adopt the way of separating digital signal ground with analog signal ground and connecting them at a point. For the part of analog circuit, which includes DDS chip, multiplier, and relay, it should use the way of linking grounds, respectively, and linking the ground at a point, thicken the ground line at the same time.

The clock circuit of DDS wave generator is a critical part in the design, which can be easily interfered and have great influence on the quality of the output wave, so we should pay special attention to this part. In order to reach the purpose of isolation, the crystal oscillator should be close to the pin of DDS chip, thicken the line of crystal oscillator and the power, add cuprum to the shell of the crystal oscillator. The PCB design diagram of AD9833 is shown in Figure 14.

We should make the power line bold as large as possible because of its high current and take the impedance into consideration. The STAR structure is used in the power wiring. In fact, in this design, it is designed into the shortest structure by manual wiring at first, which must control the width of the conducting wire. Then, for each current channel of their device, the conducting wire must guarantee more than 20 mils. Finally, the circuit will be fulfilled into STAR structure. Finally fulfill the circuit into STAR structure. The whole PCB design diagram is shown in Figure 15.

4. The Software Design of Signal Generator

4.1. The Overall Design of Software. The main program diagram of SCM software is shown in Figure 16, which is based on the idea of structured and modular design. The initialization section mainly deals with writing operation on a few special function registers, to set the mode and initial value of each module and initialize variables used. Then, output the default waveform, and restore the last working state if reset source is the watchdog or the missing clock detector. Scanning of the keyboard is controlled by timer T0, implemented into different subfunctions according to different waveforms and waveform generating mode.

4.2. The Software Design of Signal Generator. AD9833 is programmable DDS signal generator with two 28-bit frequency registers inside and two 12-bit phase registers. The software block diagram is shown in Figure 17.

Firstly, write 16-bit operating mode command word to determine working conditions and select the frequency register and phase register, and, secondly, write one or two frequency control words to control the output frequency. Finally, write phase control word, so that the DDS signal generator can output waveforms corresponding to a frequency determined by the value of the frequency register, and the phase determined by the value in the mode register. The sequence chart of data writing is shown in Figure 18.

4.3. The Software Design of Keyboard Inputting. The block diagram of keyboard scanning is as shown in Figure 19. Use the 10 ms interrupt of timer T0 to implement keyboard scanning, and eliminate keyboard dither according to the number of interruption. In the timer several operations are governed such as mode switching, data adding, data reduction, and left or right shift of data to be configured. In different modes, the range of the input data can be limited to prevent the input out of range. If no keyboard action can be detected beyond seven seconds, it will automatically exit the FM or AM mode and return to normal waveform generation status.

4.4. The Software Design of LCD Displaying

4.4.1. The State of Sine Condition. In different modes, the LCD must display different interface for the user. If it is the normal sinusoidal waveform generation mode, as demonstrated in Figures 20(a) and 21(a), then turn off the LCD blinking of cursor and character, display the current amplitude in the first line, and show current frequency in the second line. The high bit 0 is not displayed. If it is sinusoidal FM mode, as shown in Figures 20(b) and 21(b), set the character and cursor to blink, and adjust the lowest bit by default and adjust the cursor by the left and right keys. The lowest bit to the right will move the cursor to the highest level, and the highest bit to the left will move the cursor to the lowest position. The data size is changed by the Add and Subtract keys; if the most significant bit to adjust the data size is limited to be only 0 or 1, the amplitude can not be higher

FIGURE 16: The main program diagram.

FIGURE 17: The block diagram of DDS writing data.

FIGURE 18: The sequence chart of DDS writing data.

than the magnitude of 10 V, and the frequency can not be set higher than the value of 20 MHz. Sinusoidal amplitude modulation is shown in Figures 20(c) and 21(c), the same case as the FM mode.

4.4.2. The State of Square Wave. Using the keys is the only way to adjust the frequency under the condition of the square wave, so there are only two modes in this state: normal mode and FM mode. If it is the normal mode as shown in Figure 22(a), then turn off the LCD cursor and character blinking, display “REC WAVE” in the first line, and show the current frequency in the second line, while the high bit 0 is not displayed. If it is the FM mode, as shown in Figure 22(b), the process is the same as the process occurring in the state of sinusoidal FM mode.

5. Experimental Data and Analysis

5.1. Frequency Characteristics. The control word ΔM generated from the microcontroller is an integer, so it is calculated using floating point operation and then transferred into an integer and written into the DDS chip. Ignoring the decimal

part during integer conversion, therefore the error ΔM is ± 1 and the frequency resolution is

$$\Delta F_{\text{out}} = \frac{\Delta M * f_{\text{MCLK}}}{2^{28}} = 0.093 \text{ Hz.} \quad (17)$$

(1) *Frequency Resolution.* Inclusion of rounding algorithm can reduce the error caused by removing the decimal portion, and ΔM is 536.87; thus if the decimal portion is directly removed then the obtained result is 536 and the error is 0.87. After the improvement of the rounding algorithm, the result is 537 and the error is 0.13, which is significantly reduced. After rounding algorithm, the frequency control word M is

$$M \approx \left\lceil \frac{F_{\text{out}} * 2^{28}}{f_{\text{MCLK}}} + 0.5 \right\rceil. \quad (18)$$

Among the above, $f_{\text{MCLK}} = 25 \text{ MHz}$.

The most significant deviation of the frequency control word is 0.5, so the frequency resolution is

$$\Delta F_{\text{out}} = \frac{\Delta M * f_{\text{MCLK}}}{2^{28}} = 0.046566 \text{ Hz.} \quad (19)$$

FIGURE 19: The block diagram of keyboard scanning.

The worst relative frequency accuracy is

$$\delta F_{\text{out}} = \frac{\Delta F_{\text{out}}}{F_{\text{out(min)}}} \times 100\% = 4.6566\%. \quad (20)$$

(2) *Frequency Accuracy.* The DDS working principle is based on digital sampling and the process of module recovery; therefore the number of sampling points will affect the frequency distortion and the accuracy of the composite signal. Through theoretical analysis, the sampling points and the frequency accuracy of output signal have the following mathematical relationship:

$$K_f = \frac{N}{N+1} \times 100\%. \quad (21)$$

In the formula, K_f is the frequency accuracy and N is the number of sampling points.

The more the sampling points, the higher the frequency accuracy; on the contrary, the fewer the number of samples, the lower the frequency accuracy. In this paper, the number of points varies with different output frequencies, which means the accuracy of frequency can be different:

$$\begin{aligned} K_{f_{\min}} &= 94.12\% \\ K_{f_{\max}} &> 99.99\%. \end{aligned} \quad (22)$$

(3) *Signal Distortion.* The relationship between the signal distortion and sampling point is

$$R_{\text{THD}} = \sqrt{\left[\frac{\pi/N}{\sin(\pi/N)} \right]^2 - 1} \times 100\%. \quad (23)$$

FIGURE 20: The block diagram of LCD displaying under the state of sinusoidal wave.

FIGURE 21: The LCD working sketches under the state of sinusoidal wave.

FIGURE 22: The LCD working sketches under the state of square wave.

When considering the impact of D/A converter on the accuracy of waveform distortion, the equation can be rewritten as

$$R_{\text{THD}} = \sqrt{\left[1 + \frac{1}{6 \times 2^D}\right] \left[\frac{\pi/N}{\sin(\pi/N)}\right]^2} - 1 \times 100\%. \quad (24)$$

In the formula, R_{THD} is waveform distortion, D is effective digit of the DAC converter, and N is the number of sampling points.

The frequency synthesizer in this paper is based on ROM look-up table. The principle suggests that the frequency control word not only determines the output frequency, but also determines the number of sampling points of the synthesized signal. The larger the frequency control word, the larger the output frequency and the smaller the number of sampling points; on the contrary, the smaller the frequency control word, the smaller the output frequency and the larger the number of sampling points. Along with the output

FIGURE 23: The waveform distortion contrast chart.

FIGURE 24: Experimental data of frequency testing.

frequency variation, the output signal waveform distortion also changes.

The waveform distortion contrast chart is shown in Figure 23, and the normal sine wave output is shown in Figure 22(a). When the frequency control word and the output frequency are increased, the sampling points will be reduced and the output waveform can be distorted, as shown in Figure 22(b).

This paper presents the maximum and minimum output signal waveform distortion:

$$\begin{aligned} R_{\text{THDmin}} &= 0.638\% \\ R_{\text{THDmax}} &= 11.67\%. \end{aligned} \quad (25)$$

The frequency testing data curves are as shown in Figure 24.

5.1.1. Analysis of Frequency Error

(1) *The Error of Phase Truncation.* In order to obtain high-frequency resolution, the digit of phase accumulator N is generally rather large. However since ROM capacity is limited, the N -bit phase accumulator output only employs the high A bit for addressing ROM ($N > A$), and the low bit ($B - A$) is rounded, resulting in a phase truncation error. Spectrum emission caused by phase truncation is mainly about the

spectrum of spurious signal staying at the spectrum on both sides of the output signal, and the spurious spectrum is the combination of the reference clock and output frequency; the spurious spectral amplitude varies with the function of $S_a(x)$. According to the theoretical analysis, the main spectrum S and the magnitude of the strongest stray spectrum S_{spur} satisfy the following relationship:

$$\frac{S}{S_{\text{spur}}} \geq 6(N - B) \text{ dB}, \quad (26)$$

whereby N is the digit of phase accumulator and B is the discarded digit. The value of $(N - B)$ decides the level of the strongest truncated spectrum relative to the main spectrum which is caused by phase deduction. The design of the DDS module in this study uses a 28-bit phase accumulator and 12-line ROM address, and the rounded digit in the accumulator is $B = 16$. From (16) it can be calculated that the level of the strongest truncated spectrum relative to the main spectrum is more than -72 dB.

(2) *Amplitude Quantization Error.* Because the ROM stores the coding samples of waveform amplitude, these code words are represented by finite-bit binary data, which introduces amplitude quantization error. In general, the amplitude of the quantization noise signal is much smaller than the amplitude of the spurious signal caused by the phase truncation and

FIGURE 25: Amplitude characteristic.

DAC errors; within a certain range it is regarded as homogeneous distributed white noise. The total noise ratio can be obtained with statistical methods,

$$\text{SNR} = 6.02A + 1.76 \text{ dB.} \quad (27)$$

In the above A is effective addressing digit of phase accumulator output, and the total amplitude quantization SNR is 74 dB caused by spurious signals.

5.2. Amplitude Characteristics. As shown in Figure 25, when the input voltage is fixed at 1 V, 2 V, 3 V, and 4 V, within the low frequency range (0–10 kHz) the signal attenuation is 0 dB, which means the actual output amplitude is consistent with the given amplitude. When the frequency is over 10 kHz, the amplitude starts to decay; the higher the frequency, the greater the attenuation, and the system 3 dB cutoff frequency is at 80 kHz. The magnification of the multiplier will decrease with the increase of input signal frequency. While maintaining a constant amplitude sinusoidal signal input, we must change D/A output voltage. When the sine waveform amplitude is set to 1 V, the attenuation is less than –4 dB at the frequency of 100 kHz, when the amplitude is set to 2 V, the amplitude attenuation is close to –5 dB, and when the amplitude is set to 3 V, attenuation is greater than –5 dB.

5.3. Real Output Waveform. The amplitude and frequency are improved by the above method, and the output of the

sine wave is measured as an example. Figure 26 shows the different frequency of sinusoidal signal output waveform when fixing the certain amplitude. Figure 27 shows the different amplitude of sinusoidal signal output waveform when fixing the certain frequency. The figures also show that the designed signal generator output is stability and has high accuracy.

6. Conclusions

A signal generator with integrated programmable DDS device is present. By DDS device and microcontroller, and it can change frequency and phase under the control of MCU. The amplitude of the output sinusoidal signal can be adjusted using the microcontroller; 12-bit D/A port was used to generate a variable voltage and then do the multiplication with the fixed amplitude of a sinusoidal signal in the multiplier. A sinusoidal signal with certain amplitude can be changed into a square wave signal through hysteresis comparator, changing comparison voltage to adjust the variable duty cycle of the square wave. Experimental results showed that the signal generator is of high resolution, high precision, small size, and light weight and is convenient and stable in use. According to the sampling theorem, the system DDS chip operates at 25 MHz reference clock, and the output frequency of the sinusoidal signal can theoretically reach 12.5 MHz. However, when the output frequency increases to 10 kHz the

(a) The sinusoidal signal waveform output peak-peak voltage of 4 V and frequency of 6 Hz

(a) The sinusoidal signal waveform output peak-peak voltage of 5 V and frequency of 3 Hz

(b) The sinusoidal signal waveform output peak-peak voltage of 4 V and frequency of 3 Hz

(b) The sinusoidal signal waveform output peak-peak voltage of 3 V and frequency of 3 Hz

(c) The sinusoidal signal waveform output peak-peak voltage of 4 V and frequency of 1 Hz

(c) The sinusoidal signal waveform output peak-peak voltage of 2 V and frequency of 3 Hz

FIGURE 26: Sinusoidal signal output waveform with different frequency and fixed amplitude.

FIGURE 27: Sinusoidal signal output waveform with different amplitude and fixed frequency.

amplitude begins to decay due to bandwidth limitations of the multiplier. Although nonlinear compensation algorithm has been used in the system software to enlarge bandwidth to some extent, further improvements are still needed.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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