Research Article

Drive Current Enhancement in TFET by Dual Source Region

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Received 9 January 2015; Revised 15 April 2015; Accepted 3 May 2015

Academic Editor: Muhammad Taher Abuelma'atti

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This paper presents tunneling field-effect transistor (TFET) with dual source regions. It explores the physics of drive current enhancement. The novel approach of dual source provides an effective technique for enhancing the drive current. It is found that this structure can offer four tunneling junctions by increasing a source region. Meanwhile, the dual source structure does not influence the excellent features of threshold slope (SS) of TFET. The number of the electrons and holes would be doubled by going through the tunneling junctions on the original basis. The overlap length of gate-source is also studied. The dependence of gate-drain capacitance C_{gd} and gate-source capacitance C_{gs} on gate-to-source voltage V_{gs} and drain-to-source voltage V_{ds} was further investigated. There are simulation setups and methodology used for the dual source TFET (DS-TFET) assessment, including delay time, total energy per operation, and energy-delay product. It is confirmed that the proposed TFET has strong potentials for VLSI.

1. Introduction

Consumer electronics meet minimizes active and leakage power by scaling down the supply voltage below 0.5 V [1]. The proposed TFET has been the subject of intense investigation in the last decade. It has gained an immense popularity because of its lower threshold slope and off-state current I_{off} [2–4]. Always operated in highly reversed conditions of p-n junctions, TFETs also present significant low power dissipation. The conduction current in TFETs is essentially generated by the band-to-band tunneling (BTBT) of carriers through the forbidden-band gap, and the tunnel probability is mainly governed by the applied voltage, and TFETs devices produce an ideal on-off switching with a steep threshold slope [5–8]. However, experimental results show that the on-state currents are typically much smaller than those provided by metal-oxide-semiconductor field-effect transistor (MOSFET).

The main challenge for those boosters is to improve its on-state current I_{on} without degrading the device performance. In order to address these issues, a low on-state current has been reported to dramatically improve with the use of high- k gate dielectric, silicon on insulator technology [4–6], and double-gate (DG) architecture [7]. Further developments are necessary in issues such as the formation of the

high- k gate stack with low interface state density and low gate leakage current [8]. The double gate (DG) can have a better gate control over the channel. In addition, many methods have been proposed, such as heterojunctions [9, 10] and III–V materials [11–16], in which the tunneling probability is enhanced by the reduction of tunneling width with the conduction or valence band discontinuities. However, the ambipolar leakage current I_{amb} was also increased; poor SS have been seen in them.

Although numerous advanced techniques have been proposed to more effectively control the tunnel width for improving on-state current I_{on} and lowering the threshold slope (SS) in TFET, most of these methods are negative effect; what is more, the drawback of the TFET is obviously reflected; I_{off} and the ambipolar leakage current I_{amb} were also increased simultaneously. Fortunately, TFETs have been experimentally demonstrated in a new structure that causes the gate field to be easy to penetrate the channel region.

The structures of the above TFETs are generally design by adopting only one source, drain, and one channel region. These structures enhance the tunneling ability; however, the tunneling areas were not made larger. TFET is a gated p-i-n diode; it exploits a BTBT mechanism of electrons from the valance band of the source to the conduction band of the channel region to generate current [2]. In terms of a DG

TFET, if there were two source regions, the two source regions share the drain region; there will be a 50% increase in the total number of electrons and holes.

The key idea of present work is that common drain and two source regions were used. If the double gate and dual source TFET (DS-TFET) were recruited, four tunneling junctions will exist in the new geometry, which results in the increasing in the total number of electrons and holes in those tunnel junctions without influencing the threshold slope. This paper will show the dual source structure, realized in Ge/Si heterojunction TFET. This gate-source all-overlap structure geometry can also lead to the increase of the on-state current I_{on} . In addition, longer length of drain region could suppress the ambipolar leakage current I_{amb} .

2. Device Structure and Simulation

This DS-TFET device can be fabricated using the process flow shown in Figure 1(a): first, drain region is in the middle of the device by wet chemical etching process; drain doping region is then formed by ion implantation. Two source regions end in the device, which is formed by chemical etching and formed by ion implantation. Then the wet chemical etching method etches the SiO_2 layer, which is replaced by the H_fO_2 through the chemical vapor deposition (CVD). Then the drain and source electrode is formed by CVD. At last, spacers are formed and gate contact is defined. The device structure for dual source tunnel field-effect transistor (n-type TFET) used in this paper is shown in Figure 1(b). The parameters for the dual source structure in this simulation are the highly boron-doped p-region (10^{20} cm^{-3}), the lightly phosphorous-doped n-region (10^{16} cm^{-3}), and the highly phosphorous-doped n-region (10^{19} cm^{-3}) to reduce ambipolar effects act as the source, the channel, and the drain, respectively. For simplicity of explanation, Ge/Si heterojunction TFET in this work with body thickness (T_{body}) of 10 nm, electrical oxide thickness of 2 nm, and channel length is 45 nm. The gate work function (ϕ_m) was designed to be 4.6 eV.

For the device operation of an n-TFET, a positive V_{DS} is applied. The mechanism of current flow in this device is based on the BTBT of electrons from the valance band of source region that is below the bottom of the conduction band of the channel region. The tunneling of electron takes place on the edges of the gate near the source. Silicon is an indirect band gap material, so indirect lateral tunneling dominates the main part of the total current in those conventional TFETs. Due to the corresponding smaller BTBT generation rate, the on-state current I_{on} is very small. When the gate overlaps the source completely, the indirect current will be enlarged with the increasing overlap areas, the final tunneling current is also obviously increased in the uniform field limit. Another reason is that two source regions, the total tunneling electrons, are twice as large as a single p-i-n structure TFET.

In order to reduce the ambipolar current, longer length drain region is used in this structure. Now, here exists an intrinsic drift region, and the gate could not influence the channel-drain tunneling junction; hence, the ambipolar and leakage current could be suppressed.

Drain current was studied through TCAD simulator, employing dynamic nonlocal tunneling models, and the standard drift-diffusion carrier transport and Shockley-Read-Hall (SRH) recombination models and Lombardi's mobility model. Although the use of a classical drift-diffusion model or an abrupt doping profile, this does not have much impact on the focus of this paper and relative results due to variation in different device parameters.

3. Results and Discussion

3.1. Current-Voltage Characteristics. Figure 2(a) shows the transfer characteristics of the new structure DS n-TFET and conventional n-TFET with the drain-to-source voltage at $V_{DS} = 1.0 \text{ V}$. Threshold voltage V_T is the value of V_{GS} when I_{DS} is a constant current of $10^{-15} (\mu\text{A}/\mu\text{m})$ and the value of V_T is about 0.52 V, which is shown in Figure 2(a). All other device parameters for the two devices remained the same, and the high- k gate dielectrics H_fO_2 oxide thickness is 2 nm. In the first case, the new device is a structure without considering gate-channel underlap and overlap situations. An on-state current of $0.93 \mu\text{A}/\mu\text{m}$ and an on/off ratio of 10^{11} are obtained with a V_{DS} of 1.0 V in the DS-TFET; the on-state current of DS-TFET is nearly twice than that of conventional TFET. This result indicates that the dual source regions contribute to the tunneling current.

Output characteristics for different values of the gate overdrive voltage for the DS-TFETs are shown in Figure 2(b). For different gate overdrive voltages $V_{GT} = V_{GS} - V_T$. It is observed that I_{DS} initially very rapidly increases with increasing V_{DS} . As shown, the drain current saturates for drain voltages above approximately 1.2 V. Finally, an increase in V_{DS} results in sustained growth in channel potential; some of the electrons are pulled back to common drain, so the electron concentration will reduce in the channel, a good saturation of I_{DS} , at higher V_{DS} . There is a perfect saturation of the drain current I_{DS} in Figure 2(b). The pinch off voltage is found to be $\sim 1.1 \text{ V}$ in Figure 2(b) for overdrive voltage $V_{GT} = 0.5 \text{ V}$. It is evident in Figure 2(a) that I_{DS} does not increase for further increase in V_{DS} beyond the pinch off value of $\sim 1.1 \text{ V}$.

The excellent characteristics of the DS-TFET can be obtained by using heterojunction. A Si-based heterojunction can be used to reduce the effective tunneling barrier height by replacing the Si in source region with Ge (all the dimension for simulated devices are same, gate length is 45 nm and oxide thickness is 2 nm). The on-state current of the Ge/Si heterojunction for HDS-TFET can reach $10 \mu\text{A}/\mu\text{m}$ at $V_{DS} = V_{GS} = 1.0 \text{ V}$, as shown in Figure 3(a).

The I_{on}/I_{off} ratio for the conventional TFET, DS-TFET, and Ge/Si DS-TFET is shown in Figure 3(b). The DS-TFET has better I_{on}/I_{off} ratio than that of conventional TFET. All other dimensions and parameters for all the devices in this case are kept the same. At smaller gate lengths, the SRH current is dominant of total current. However, the short channel effect affects the SRH current which leads to the increasing of the off-current and the smallest I_{on}/I_{off} ratio at 10 nm gate length. When L_g exceeds 35 nm, the BTBT current cannot be increased and off-current will be unaffected. Hence the ratio remains the same.

FIGURE 1: (a) Process flow of DS-TFET. (i) Wet chemical etching of oxide layer. (ii) Drain implantation. (iii) Wet chemical etching of oxide layer. (iv) Source implantation. (v) Wet chemical etching and CVD for metal electrode. (v) Spacer formation and gate electrode. (b) Two-dimensional cross section of the simulated device structure for DS-TFET and conventional TFET: $L_{\text{gate}} = 45 \text{ nm}$, $X_d = 25 \text{ nm}$, $L_d = 10 \text{ nm}$, $T_{\text{OX}} = 2 \text{ nm}$, $T_{\text{body}} = 10 \text{ nm}$, and $L_{\text{underlap}} = 2 \text{ nm}$.

Extract the threshold voltage swing, for a given gate voltage V_{GS} . The threshold voltage slope (SS) is defined as

$$\text{SS} = \frac{1000}{(d/V_{\text{GS}}) \log I_{\text{DS}}}. \quad (1)$$

It is worth noting that the threshold slope of the HDS-TFET is only half of the DS-TFET. As can be also seen in Figure 3, the simulated on-state current is about three orders of magnitude compared to the DS-TFET and conventional TFET, and the on/off ratio is also about 10^{11} .

3.2. Analysis of Gate-To-Source Capacitance and Gate-To-Drain Capacitance. Figure 4 shows the small signal total gate (C_{gg}), gate-to-source (C_{gs}), and gate-to-drain (C_{gd}) of the conventional n-type TFET and n-type DS-TFET. C_{gs} and C_{gd} are extracted from the small-signal AC simulations at a frequency of 1 MHz. In terms of the MOSFET, the total gate capacitance is known to be equally distributed between the source and drain terminals. However, when the DS-TFET is forward biased, the terminal bias makes the entire gate capacitance to fall upon the drain terminal, causing much higher C_{gd} ($\approx C_{\text{gg}}$). As shown in the Figure 4, the value of C_{gd} is 10 times more than that of C_{gs} . On the contrary, when

FIGURE 2: Device characteristics for the new structure n-TFET with 10-nm-thick silicon body and conventional n-TFET: (a) logarithmic and linear transfer characteristics for different values of V_{DS} ; (b) simulated output characteristics at different values of the gate overdrive V_{GT} .

the DS-TFET is a negative gate bias, C_{gs} is the biggest part of the total capacitance. The gate capacitance of DS-TFET was just slightly increased. This can explain that the dual source regions can increase total capacitance.

As shown in Figure 4, C_{gs} rapidly decreases for the further increase in V_{GS} ($V_{\text{GS}} > 0 \text{ V}$). When the DS-TFET is forward biased and V_{GS} is greater than threshold voltage V_T , the electron inversion layer becomes thicker for the further increase in V_{GS} , and potential barrier is reduced in channel-to-drain side, so C_{gd} rapidly increases. C_{gd} is the Miller capacitance, when electron concentration is equal to the body doping concentration in the inversion layer, the total number of electrons reaches saturation, and C_{gd} becomes constant. It can be seen clearly in Figure 4 that

C_{gs} decreases slightly from the value of the V_{GS} of -0.5 V to 0.5 V , due to the electron inversion blocks the coupling of the gate-to-source capacitance and the source depletion width increases with gate voltage. In particular, V_{GT} is greater than 0 V ($V_{\text{GS}} > 0.5 \text{ V}$), C_{gs} once again decreases, due to the V_{DS} can easily affect the channel-to-source tunnel junction, so the tunnel barrier of channel-to-source side will be more narrow. However, V_{GS} is less than -0.5 V , source depletion layer is formed and so does the source charge, and now C_{gd} is much less than C_{gs} . In particular, V_{GS} is smaller than -0.55 V , C_{gd} drops quickly with decreasing V_{GS} ($V_{\text{GS}} < -0.5 \text{ V}$). C_{gd} is very small, due to the presence of the channel-to-drain tunnel barrier. C_{gs} is dominated by the gate and the source depletion width, as shown in Figure 4. These features of capacitance fully demonstrate the symmetry of TFET. We now investigate the influence of V_{DS} on the gate-to-source capacitance and gate-to-drain capacitance. A plot of gate-to-drain capacitance C_{gd} and gate-to-source capacitance C_{gs} as a function of V_{DS} for V_{GT} is shown in Figure 5. For n-type DS-TFET and conventional n-TFET, it is observed that gate-to-source capacitance increases for increasing V_{DS} ; however, the gate-to-drain capacitance drops rapidly at $V_{\text{DS}} = 0.6 \text{ V}$. It also indicates in Figure 4 that the capacitance values of DS-TFET are bigger than conventional one; however, they are still the same order of magnitude. It is the same as previous result that two capacitors are connected in parallel. At a fixed V_{DS} , the trends of the C_{gs} and C_{gd} coincide with the foregoing discussion [17, 18]. It is also shown from the capacitance-voltage characteristics at $V_{\text{GT}} = 0.4 \text{ V}$ and 0.6 V in Figure 5(b) that C_{gd} rapidly decreases for further increase at $V_{\text{DS}} = 0.6 \text{ V}$. Meanwhile, the C_{gs} reaches saturation, due to the reduction in the tunnel barrier width for further V_{DS} ; the source depletion width also weakly depends on the drain voltage. C_{gd} will be very small due to higher potential barrier between channel and drain and reduction of the inversion electron concentration in the channel, respectively. On the other hand, C_{gs} increases rapidly before $V_{\text{DS}} = 1.2 \text{ V}$, due to the reduction in tunneling barrier for higher V_{DS} . After saturation, C_{gs} continues to increase no longer, because the additional V_{DS} cannot affect the channel-to-drain junction.

3.3. Impact of Scaling. We now research the impact of a varying drain region length X_d on the ambipolar current dependence of the device performance. All other device parameters are kept the same as that in the previous case. For the DS-TFET, the transfer characteristics are shown for four different lengths of the drain region. In order to see the impact of the total length of command drain region on the ambipolar current, the transfer characteristics were shown in Figure 6(a). As shown in Figure 6(a), the leakage current I_{off} drops, due to an increasing in length of the common drain region. It is evident that a shorter common drain region causes more and larger electrostatic field drop on the channel-to-drain side junction. The V_{DS} now appears across the channel-drain junction, and the geometry enables stronger coupling of gate-to-drain, which results in a higher leakage current. The longer the length of X_d , the less the leakage current.

FIGURE 3: (a) Transfer characteristics of the Ge/Si DS-TFET, DS-TFET, and conventional TFET; (b) I_{on}/I_{off} ratio versus gate length.

FIGURE 4: Gate-to-drain capacitance and gate-to-source capacitance (a) total gate capacitance (b) with respect to the gate voltage at $V_{DS} = 0.5$ V for conventional and DS-TFET.

FIGURE 5: (a) Capacitance-voltage characteristics showing the C_{gd} and C_{gs} capacitances as function of V_{DS} at $V_{GT} = 0.4$ V for DS n-TFET and conventional n-TFET. (b) Capacitance-voltage characteristics showing the C_{gd} and C_{gs} capacitances as function of V_{DS} for two different values of V_{GT} for DS n-TFET.

FIGURE 6: Transfer characteristics of the DS-TFET: (a) drain-extension dependence; (inset) ambipolar current versus drain region length, where the X_d is the distance from middle to the gate edge; (b) gate-source overlap dependence; (inset) on-state current versus overlap length.

To improve the on-state current for the DS-TFET, the gate-source overlap was adopted. All other device parameters are kept the same as that in the previous case; the gate-source overlap length L_d is only changed. It can be seen in Figure 6(b) that the gate-source overlap length L_d was increased, which resulted in increasing on-state current I_{on} . It can be explained that vertical tunneling happened in the vertical orientation except for gate-source overlap region, in which L_d is 0 nm.

This implies that the gate electrode would affect not only the channel-source tunneling junction, but also the middle of channel. Not only in lateral direction electrons is tunneling across the tunneling junction, but in vertical direction. Due to these electrons would be far away from the middle of the source region to close to oxide-semiconductor

interface. It can be seen clearly in Figure 7 that an increasing in gate-source overlap length resulting in corresponding enlargement of tunneling junction area. The on-state current increases linearly with the tunnel junction area for L_d . When the overlap length reaches 25 nm, the current is dominated totally by vertical band-to-band tunneling (BTBT) current.

All the above simulation results also indicate that it is reasonable to experimentally research the DS-TFET geometry since the device performance is easily affected by the gate-source and gate-channel periphery.

3.4. Delay-Power versus Supply Voltage. In Figure 8(a), the simulated gate capacitance is shown as a function of gate voltage at a drain voltage of 0 V. In on-state, the capacitance C_{gg} is dominated by the enhancement Miller capacitance C_{gd} ,

FIGURE 7: Plots showing the eBTBT rates for the DS n-TFET biased at $V_{DS} = 1.0$ V and $V_{GS} = 2.0$ V for different values of the gate-source overlap. (a) 5-nm overlap length, (b) 10-nm overlap length, (c) 15-nm overlap length, (d) 20 nm overlap length, and (e) 25 nm overlap length.

which mainly comes from inversion charge [18]. The simulated curve is the same as Figure 4. Although the threshold voltages are different, the device capacitance is still less than 17 fF in Figure 8(a). For different work function, there are different threshold voltages, respectively. It can be seen in Figure 8(b) that the threshold voltages V_T increase since work function ϕ_m is increased, which is consistent with the work function characteristics [19]. From 4.3 eV to 4.6 eV, the values of V_T are 0.23 V, 0.26 V, 0.45 V, and 0.52 V, respectively.

Figure 9(a) shows the effects of V_T on the on-state current I_{ON} . The on-state current will be limited by V_T . For a higher V_T DS-TFET, if it operates in threshold region leading to a lower I_{ON} , hence, it is required to apply a larger V_{DD} to achieve a lower delay. The relatively higher threshold voltage leads to a lower leakage current; the lower V_T consumes lesser energy for the operating frequencies < 100 MHz. The lower V_T requires a lower V_{DD} for obtaining the same targeted performance leading to quite lower energy dissipation. The extracted delay is shown as a function of supply voltage in Figure 9(b) for the DS-TFET. Roughly delay is given by $C_L V_{DD} / I_{ON}$ [20]. Better I_{ON} gives a better performance for a fixed V_{DD} . Figure 8(a) shows that the capacitance magnitude is about 17 fF. DS-TFET delay decreases with decreasing the threshold voltage, due to the on-state current improved at a fixed supply voltage. As shown in Figure 9(c), the dynamic power is roughly calculated by $C_L V_{DD}^2 / \tau$ [21, 22]. It can be proved in Figure 9(c) that the lower delay at a fixed V_{DD} results in larger dynamic power dissipation. The static power dissipation can be obtained by $V_{DD} \times I_{OFF}$, and it can be seen in Figure 9(d) that the higher V_T results in higher static power dissipation. All the device performance has been improved remarkably; the static power dissipation is $\ll 1$ fW. It is necessary to reduce power consumption for a longer battery life. For this purpose, it is shown in Figure 9(e) static energy as a function of maximum operation frequency.

(a)

(b)

FIGURE 8: (a) Gate capacitance C_{gg} as a function of gate-to-source voltage V_{DS} for different threshold voltage V_T . (b) Simulated transfer characteristics, for DS-TFET device with varying V_T , where V_T is defined at a gate voltage where the device exhibits a sharp rise in drain current.

Figure 9(e) indicates that static energy will decrease with increasing in the operating frequency. Meanwhile, the curve shows that the smaller the threshold voltage, the less the static energy. For a lower operating and a given V_{DD} , it is import to reduce threshold voltage for a leakage current. For mobile devices, most of the time they are in standby mode where very low signal active and longer battery life are need, so it is necessary to optimize the high V_T devices. Due to very low leakage current, the DS-TFET is fit for the low power circuit at a lower operating frequency and for a fixed V_{DD} .

Figure 10(a) shows the total energy per operation as a function of operating frequencies. The total energy consists of static and dynamic energy. For the lower V_T DS-TFET, on-state current is higher at the lower supply voltage and

FIGURE 9: (a) On-state current I_{ON} at $V_{DS} = V_{GS} = V_{DD}$, (b) delay versus supply voltage for DS-TFET devices for different threshold voltage, (c) dynamic power versus supply voltage, (d) static power versus supply voltage, and (e) static energy versus supply voltage maximum frequency.

FIGURE 10: (a) Total energy operation versus maximum frequency for different threshold voltage V_T ; a low V_T can be used with a lower supply voltage resulting in low energy dissipation; the smallest leads to an energy saving of about 5x in comparison with high V_T at 1 MHz; (b) energy-delay product (EDP) for different V_T . It can be seen that the smallest value of V_T can be optimized compared with other values.

a lower leakage current, resulting in smaller total energy. In this analysis, the energy per operation of this system is given by [23]

$$E = \frac{1}{2} \cdot n \cdot C_L V_{DD}^2 \left(\alpha + \eta \cdot n \frac{I_{leak}}{I_{ON}} \right), \quad (2)$$

where n is the number of inverter stages, η is a technology-dependent parameter that represents delay degradation due to the slope of the input signal, and α is an activity factor. I_{leak} is the leakage current of a single inverter. All other variables are mentioned previously for DS-TFET. The equation reveals that a great deal about the energy depend on I_{leak} and I_{ON} , where $\alpha = 0.1$, $\eta = 1$, $C_L = 17$ fF, and I_{leak} and I_{ON} are extracted from TCAD simulations. The high threshold voltage requires a higher supply voltage for meeting performance indicators, so the overall dissipation also will be increased.

Sometimes it is important to take energy-delay product (EDP) into account for a sufficient level of performance in mobile devices. It can be seen clearly in Figure 10(b) that the highest V_T leads to maximum EDP. Due to higher energy and higher delay, the high V_T is unfit for low power applications. The low V_T is quite superior at lower supply voltages.

3.5. Effect of Variation in Oxide Thickness. It is observed in Figure 11 that the impact of the oxide thickness on the device performance of the DS-TFET and conventional TFET are studied. All other device dimensions and parameters are kept the same as in the previous case. The body thickness is 10 nm, gate length is 45 nm, drain region length $X_d = 25$ nm, gate-channel underlap is 0 nm, and gate-source overlap is 0 nm. The values of the oxide thickness used are 2 nm, 3 nm, and 4 nm. The effects of varying the value of the oxide thickness on the gate capacitance characteristics of the n-type DS-TFET are shown in Figure 11(a). It is evident in Figure 11(a) that an increase in the value of the oxide thickness results in

corresponding reduction of the gate capacitance. Shrinking of the oxide thickness enhances the Miller capacitance effects. The reason for this behavior is improvement ability of gate control over channel, which increases electron concentration in the channel for further V_{GS} . In particular, the carrier concentration is higher at the drain side than source side. The gate-to-drain C_{gd} dominates in on-state while gate-to-source C_{gs} in off-state.

In Figure 11(b), the delay curves of the DS and conventional TFET were shown. The delay reduces with increasing oxide thickness, due to thin oxide thickness leading to high current even near off-state condition in DS-TFET at $V_{GS} = V_{DS} = V_{DD} = 0$. Figure 11(c) shows that DS-TFET and conventional TFET have three different oxide thickness values. The thinnest oxide thickness produces the relatively higher on-state currents at lower supply voltages and the delay is calculated according to the $C_L V_{DD} / I_{ON}$. So the delay reduced with decreasing the oxide thickness. It can be seen in Figure 11(c) that the slimmest oxide DS-TFET consumes the least energy for operating frequency <100 MHz. The thickest oxide DS-TFET needs a higher supply voltage for the better performance leading to the higher energy dissipation per operation. Figure 11(d) shows the EDP values of three oxide thickness DS-TFET, the thickest oxide device consumes the highest static energy and dynamic energy, and the on-state current is the smallest one of them and the highest delay, resulting in very high EDP.

4. Conclusion

In summary, we have shown that the DS-TFET can improve the on-state current by dual source regions. The increased tunnel junction area leads to improving the on-state current. The drive current of heterojunction DS-TFET can exceed the MOSFET. Although heterojunction DS-TFET will produce a large parasitic capacitance which comes from Miller effect, this disadvantage is not obvious. In contrast, the reduction

FIGURE 11: (a) Gate capacitance C_{gg} as a function of V_{GS} for four different values of oxide thickness for DS n-TFET, (b) delay versus supply voltage for DS-TFET and conventional TFET for different oxide thickness, (c) total energy per operation versus the maximum frequency for DS-TFET and conventional TFET corresponding to the same other dimensions and parameters, and (d) EDP versus supply voltage for DS and conventional TFET for three different values of oxide thickness.

of EDP and total energy per operation of DS-TFET makes it a strong candidate. An ultra thin thickness of body and oxide also reduces the total energy per operation and EDP. DS-TFET simulations revealed that dual source regions can improve the on-state current and keep the excellent characteristics of the TFET device at the same time.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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