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Research Article

A Four Quadrature Signals' Generator with Precise Phase Adjustment

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A four-way quadrature signals generator with precise phase modulation is presented. It consists of a phase precision regulator and a frequency divider. The phase precision regulator generates two programmable currents by controlling the conduction of the tail current sources and then changes the currents into two bias voltages which are superimposed on the clock signals to adjust the phase difference of the four quadrature signals generated by the frequency divider, making the phase difference of 90 degrees. The four quadrature signals' generator with precise phase modulation has been implemented in a 0.18 μm mixed-signal and RF 1P6M CMOS technology. The size of the chip including the pads is 675 μm $*$ 690 μm. The circuit uses a supply voltage of 1.8 V, a bias current of 7.2 μA, and the bits of phase-setting input level $n = 6$ in the design. The measured results of the four orthogonal signals' phase error can reach $\pm 0.1^{\circ}$, and the phase modulation range can reach $\pm 3.6^{\circ}$.

1. Introduction

The method of integrated orthogonal signal generator is RC-CR phase-shift method, and the RC-CR phase-shift network can be achieved by the input signal phase shift of 45 degrees. In the literature [1], the design of *I*/*Q* generator is used in the S band, its unbalance amplitude is 0.1 dB, and the unbalance phase is 0.1 degrees. But this method cannot adjust the phase of the signals. The method of RC-CR network is complex, and once integrated, it cannot be used for phase error compensation. In addition, the capacitor and resistance should not be too large; otherwise integrated circuit is also difficult to be integrated in the chip. The second method often uses quadrature voltage-controlled oscillator cross coupling method. In the literature [2], a QVCO which is low in power consumption is manufactured and used in 2.4 GHz PLL. This design reduces power consumption and improves the noise coefficient, but the unbalance of *I*/*Q* phase is 2.21 degrees and the phase cannot be adjustable. Then the digital quadrature signal generator is used to generate orthogonal signals [3–6], but the phase error of the signal is not adjustable and compensated. In the previous study [7], the quadrature phase error caused by the mismatch of the capacitor is very large, and this phenomenon is more serious with the increase of the frequency. The more important problem is that the implemented integrated circuit is able to generate orthogonal signals, and the phase difference of the orthogonal signal is exactly 90 degrees in the early simulation stage. However, after the chip is processed, the phase difference often deviates from 90 degrees due to the limitation of the technology of integrated circuit production. Therefore, an integrated precise adjustment circuit structure is needed to compensate quadrature signals for the phase deviation caused by the integrated circuit process.

In this paper, an integrated four quadrature signals' generator is presented. The generator cannot only produce four orthogonal signals, but also can generate a programmable current by controlling the conduction of the tail current sources. The current is converted into a bias voltage superimposed on the clock signal to adjust the phase difference of the four signals, so as to make the phase difference be 90 degrees.

2. Circuit Design

As shown in Figure 1, the structure of the quadrature signals generator is composed of a phase precision regulator

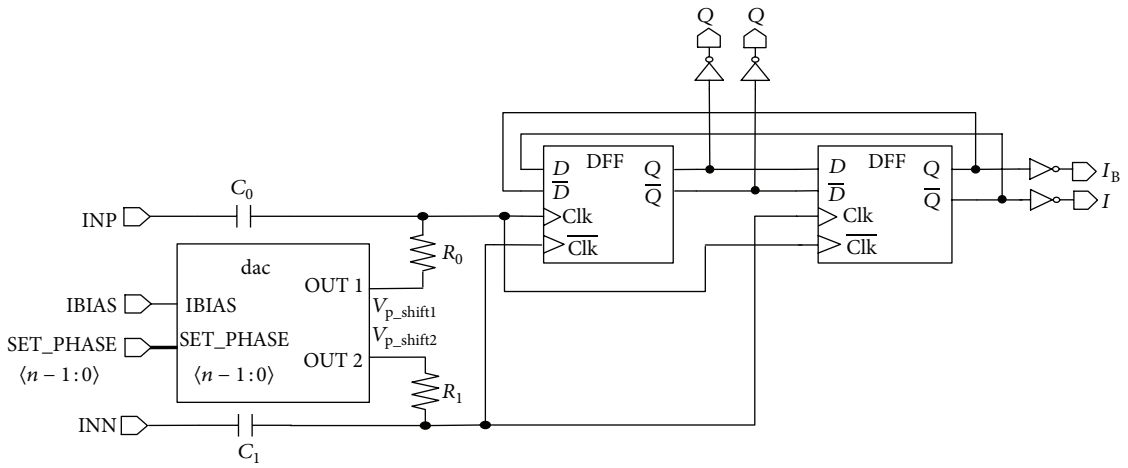

Figure 1: Circuit structure of the quadrature signal generator.

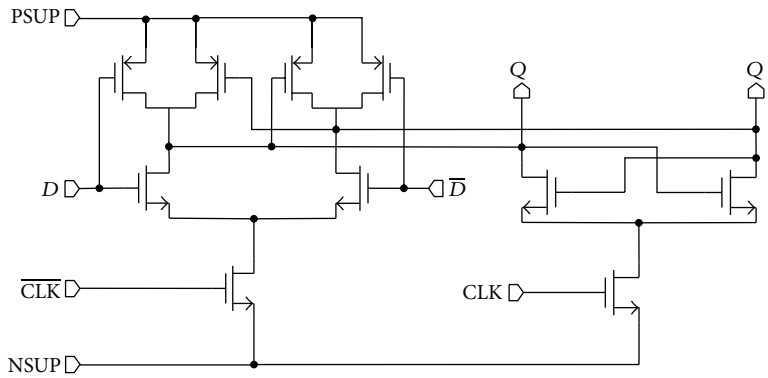

Figure 2: Circuit structure of *D* flip-flop (DFF).

unit (Ph_reg for short) and a frequency divider. The phase precision regulator unit can produce a programmable current by controlling the conduction of the tail current sources, and then the current can be converted into a bias voltage superimposed on the clock signal to precisely adjust the phase change. The frequency divider which consists of two *D* triggers (DFFs) is used to generate the four quadrature signals. The SET_PHASE$\langle n-1:0\rangle$ input level is represented by thick solid lines because it is an *n*-bit bus.

2.1. The Design of Divider. The frequency divider consists of two DFFs which are connected in the form of a two-stage ring with the differential input signal injected into the clock terminals [8]. As shown in Figure 1, the outputs of the first DFF are connected with the inputs of the second DFF, and the outputs of the second one connect back to the first one's input terminals which are in reversed polarity to achieve the extra phase shift of 180°. The clock terminals of the two DFFs are tied in reversed polarity and used to inject the differential input signal. The output signals can be taken from the data terminals of the second DFF; each output terminal's frequency is half of the input frequency.

The schematic of the DFF is shown in Figure 2. The cell of DFF contains two parts: the trigger part of the input signal is sent to the output and the storage part of the memory output logic level. The trigger part is realized by differential pairs; the lock part is realized by a cross coupling. The two parts are driven by a pair of clock signals, which are used to control the trigger circuit and the latch circuit, respectively [9].

The specific work process of the divider is as follows: when the input clock is a rising edge, the first DFF in Figure 1 is in the trigger state; that is to say, the output varies with the input. The second DFF in the lock state will remain the same state with the previous one, and its output will be sent back to the first DFF by reverse phase. When the input clock is a falling edge, the first DFF is in the lock state; the second one changes into the trigger state, and the state of its output will be locked in the first one. In this way, the time of a period of each DFF's output signal is the same as two periods of the clock signal, and the output frequency is just half of the input frequency,

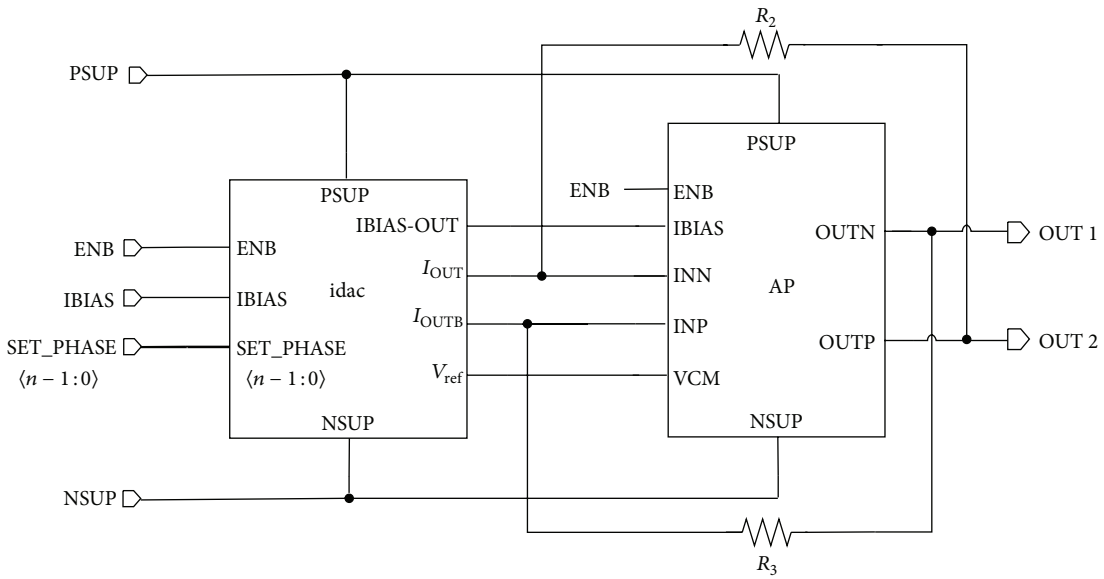

Figure 3: Circuit structure of the phase precision regulator unit.

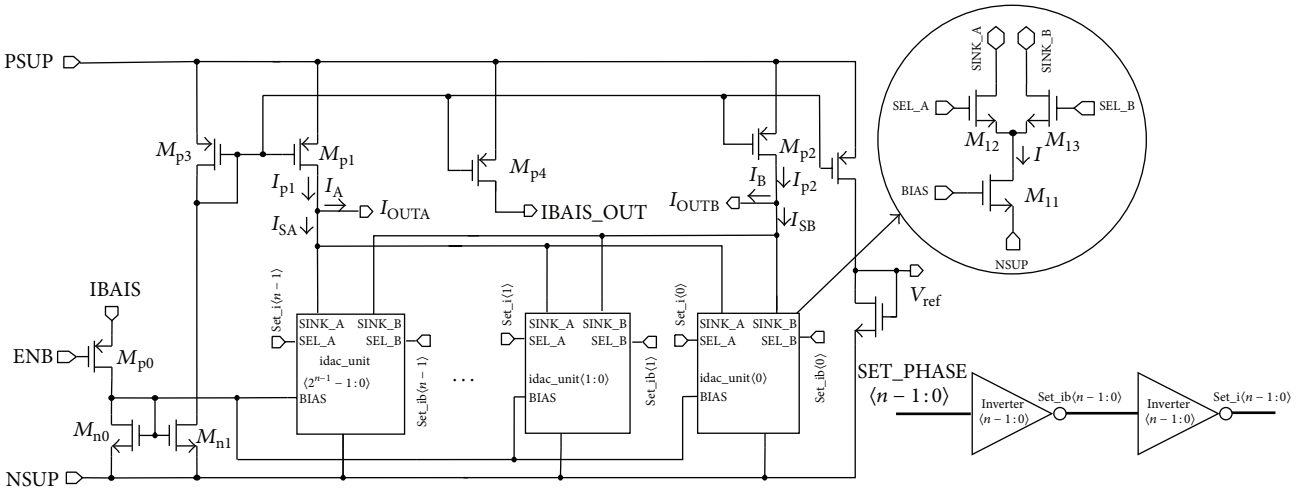

Figure 4: Structure of the programming current output cell.

thus achieving function of divide-by-2. The output terminals of the two DFFs are all used as the output signals, and then the four orthogonal signals are obtained.

2.2. The Design of Phase Modulator. The precise phase precision regulator unit can produce two programmable currents by controlling the conduction of the tail current sources, and then the programmable currents can be converted into two-way bias voltages by a COMS operational amplifier. The two-way bias voltages are superimposed on the clock signals to precisely adjust the phase change. Figure 3 shows the specific circuit of phase modulator unit, which consists of the programming current output cell (idac for short) and the current converting voltage cell. Two programmable currents are produced by n-bits phase-setting input level to control the conduction of the tail current sources in the programming current output cell. The current converting voltage cell is composed of a full differential CMOS amplifier (AP for short) and two resistors of R_2 and R_3.

The schematic of the idac is shown in Figure 4; the idac receives the external n-bits phase-setting input level of SET_PHASE$\langle n-1:0\rangle$ and generates two pair inverse strobe levels Set_i$\langle n-1,0\rangle$ and Set_ib$\langle n-1,0\rangle$ through the inverters. These pair levels are used to control the conductions of the tail current sources (idac_unit for short in Figure 4). The first bit phase-setting input signal (SET_PHASE$\langle 0\rangle$) generates two inverse strobe signals Set_i$\langle 0\rangle$ and Set_ib$\langle 0\rangle$ by the inverter

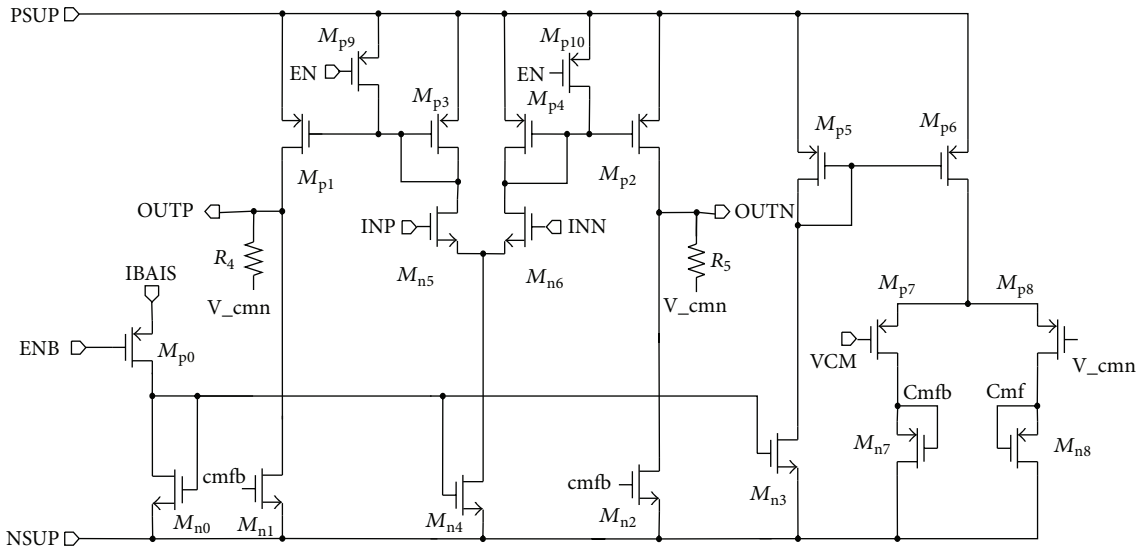

Figure 5: Structure of differential CMOS amplifier.

to, respectively, control the left and right branch of the current source (idac_unit⟨0⟩), the second bit phase-setting input signal (SET_PHASE⟨1⟩) generates two strobe signals Set_i⟨1⟩ and Set_ib⟨1⟩ by the inverter to, respectively, control two parallel left and right branches of the current sources (idac_unit⟨1 : 0⟩), and so on, and the n bit (SET_PHASE⟨$n-1$⟩) generates two strobe signals S_i⟨$n-1$⟩ and Set_ib⟨$n-1$⟩ by the inverter to, respectively, control 2^{n-1} parallel left and right branches of the current sources (idac_unit⟨$n-1:0$⟩), and the suspension points in Figure 4 are used to show the omitted idac_units from 2 to $n-2$. The left branch of the tail current source is turned on, and the right branch is turned off correspondingly; similarly, the right branch is turned on and the left branch is turned off. As a small map is shown in Figure 4, the left branch of the ith tail current module chooses the control terminal SEL_A to receive the ith bit strobe signal, the right branch of the ith tail current module chooses control terminal SEL_B to receive the ith bit signal of the inverting signal, the ith tail current module is composed of 2^{i-1} tail current sources in parallel, i is a natural number, and $1 \le i \le n$.

Assuming every branch of conduction current of each tail current source is I, when the highest bit of is 1, the others are 0 (or the highest bit is 0, and the others are 1) for the SET_PHASE⟨$n-1:0$⟩ in Figure 3, the current difference between I_A and I_B is minimum, and the value is I. Then I_A and I_B are converted into voltages by the current converting voltage unit, and the voltage difference is also the smallest. The minimum voltage difference is used to adjust and compensate the phase of the four output signals determining the accuracy of the circuit. When all bits of the SET_PHASE⟨$n-1:0$⟩ are 1 (or all bits are 0), the current difference between I_A and I_B is maximum, and the value is $(1+2+4+\cdots+2^{n-1})*I$, that is, equal to $(2^n-1)*I$, and the voltage difference is also the largest. The maximum voltage difference is used to adjust and compensate the phase of the four output signals determining the adjustment range of the circuit. When the value of I_A is increased, I_B is decreased. Assuming conduction current of M_{p1} is I_{p1}, M_{p2} is I_{p2}, and each tail current source is I, the external n-bits phase-setting input level of SET_PHASE⟨$n-1:0$⟩ is $k_{n-1}k_{n-2}\cdots k_1k_0$, and then

$$I_{SA} = \sum_{i=0}^{n-1} k_i \cdot 2^i \cdot I \quad (k_i = 1),$$
$$I_{SB} = \sum_{i=0}^{n-1} k_i \cdot 2^i \cdot I \quad (k_i = 0). \tag{1}$$

So the outcurrent of I_A and I_B is equal to

$$I_A = I_{p1} - I_{SA} = I_{p1} - \sum_{i=0}^{n-1} k_i \cdot 2^i \cdot I \quad (k_i = 1),$$
$$I_B = I_{p2} - I_{SB} = I_{p2} - \sum_{i=0}^{n-1} k_i \cdot 2^i \cdot I \quad (k_i = 0). \tag{2}$$

Yet, the sum of the two currents is constant, and its value is $(I_{p1} + I_{p2}) - (2^n - 1) * I$.

The output of the two programmable currents I_A and I_B is converted into two bias voltages through a full differential operational CMOS amplifier, the resistors R_2 and R_3, respectively. Because the two programmable currents' size and direction can be programmed with the selected external n-bits phase-setting input level of SET_PHASE⟨$n-1:0$⟩, the two-way bias voltages of OUT1 and OUT2 shown in Figure 3 are programmed. So in this design, a classic double-end differential CMOS amplifier is used as shown in Figure 5.

3. Results and Discussion

According to the simulations' results, the design can generate two programmable currents by controlling the conduction of

Table 1: The W/L values of the CMOS in Figure 3.

Device	W/L (μm)
M_{p0}	10/1
M_{p1}	12/1.2
M_{p2}	12/1.2
M_{p3}	12/1.2
M_{p4}	12/1.2
M_{n0}	3.2/2
M_{n1}	1.6/2
M_{11}	1.6/2
M_{12}	1/2
M_{13}	1/2

Table 2: The W/L values of the differential CMOS amplifier in Figure 5.

Device	W/L (μm)
M_{p0}	10/0.25
M_{p1}	100/1
M_{p2}	100/1
M_{p3}	20/1
M_{p4}	20/1
M_{p5}	40/1
M_{p6}	40/1
M_{p7}	40/1
M_{p8}	40/1
M_{p9}	10/0.25
M_{p10}	10/0.25
M_{n0}	20/3
M_{n1}	5/1
M_{n2}	5/1
M_{n3}	50/3
M_{n4}	20/3
M_{n5}	10/3
M_{n6}	10/3
M_{n7}	3/1
M_{n8}	3/1

the tail current sources and then changes the currents into two bias voltages superimposed on the clock signals to adjust the phase difference of the four signals, making the phase difference of 90 degrees.

In the design, the values of resistances are $R_0 = R_1 = 12\,\text{k}\Omega$, $R_2 = R_3 = 200\,\text{k}\Omega$, and $R_4 = R_5 = 100\,\text{k}\Omega$, respectively. The W/L values of the CMOS in Figure 3 are listed in Table 1. The W/L values of the differential CMOS amplifier in Figure 5 are listed in Table 2. Parameter settings and part of the simulation results are listed in Table 3.

For demonstration, the presented circuit has been fabricated in SMIC's 0.18 μm CMOS process with a 4 GHz phase-locked loop together. The chip microphotograph is shown in Figure 6, and the size of the chip including the pads is 675 μm $*$ 690 μm. A LC_tank voltage-controlled

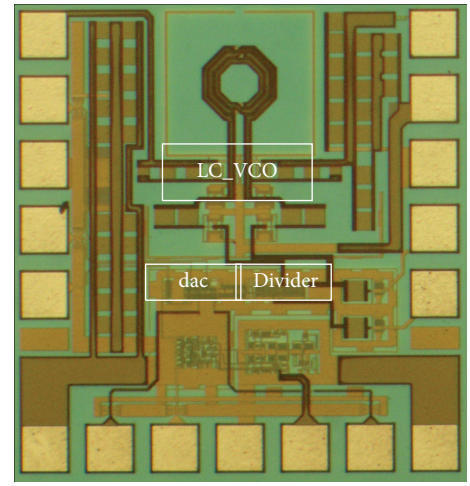

Figure 6: The microphotograph of the quadrature signal generator.

oscillator (LC_VCO) is used in the phase-locked loop. The used differential inductor has an inner diameter of 30 μm, a metal width of 8 μm, and the spacing of 1.5 μm. The value of the inductor is about 2.4 nH, and the effective quality factor is about 10 under the 4 GHz frequency. The range of the capacitor is about 0.3–0.68 pF. The tuning range of VCO is 300 MHz, from 3.85 GHz to 4.15 GHz, with the center frequency being about 4 GHz. The two output signals of the LC tank voltage-controlled oscillator are sinusoidal wave, and the signals are divided by four and used as the input clock signals of INN and INP shown in Figure 1. The circuit uses a supply voltage of 1.8 V, a bias current of 7.2 μA, and the bits of phase-setting input signal $n = 6$ in the design. There are no effective methods to measure the phase error because the present oscillography could not measure the phase error between four-channel several hundred MHz signals. The phase error is measured between every two of them based on the time domain outputs, the output four orthogonal signals' phase error precision can reach $\pm 0.1^\circ$, and the phase modulation range is $\pm 3.6^\circ$, but the phase difference in the simulation is about $\pm 2.7^\circ$. The main reason of the error is caused by different ways in the measurement and simulation; the signals' phase error cannot be directly measured because of the limitation of the instruments. The die bonding leads to error of measurement too.

4. Conclusions

In this paper, a four phase quadrature signals' generator with precise phase modulation is proposed. The design can generate two programmable currents by controlling the conduction of the tail current sources and then changes the currents into two bias voltages superimposed on the clock signals to adjust the phase difference of the four signals generated, making the phase difference of 90 degrees. It has been implemented in 0.18-μm CMOS process. The measurement result shows the proposed quadrature signal generator could achieve $\pm 0.1^\circ$ phase error, and the phase

Table 3: Parameter settings and results of the simulations.

SET_PHASE ⟨5 : 0⟩	IBIAS (μA)	I (μA)	I_{p1} (μA)	I_{p2} (μA)	I_A (μA)	I_B (μA)	V_{p_shift1} (mV)	V_{p_shift2} (mV)	Phase difference (°)
000000	7.2	0.72	23.2	23.2	23.14	−22.45	854.9	360.9	2.7
010000	7.2	0.72	23.2	23.2	11.55	−10.89	730.5	486.2	1.5
011000	7.2	0.72	23.2	23.2	5.75	−5.11	667.6	549.2	0.8
011011	7.2	0.72	23.2	23.2	5.03	4.38	643.9	572.9	0.3
011111	7.2	0.72	23.2	23.2	0.68	−0.04	612.4	604.1	0.1
100000	7.2	0.72	23.2	23.2	−0.04	0.68	604.5	612.4	−0.1
100100	7.2	0.72	23.2	23.2	−2.93	3.58	572.9	644.0	−0.3
101000	7.2	0.72	23.2	23.2	−5.83	6.47	541.4	675.5	−0.8
110000	7.2	0.72	23.2	23.2	−11.62	12.27	478.3	738.4	−1.6
111111	7.2	0.72	23.2	23.2	−22.46	23.13	360.9	854.9	−2.7

modulation range is ±3.6° with the bits of phase-setting input signal $n = 6$.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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