Research Article

Modified Tang and Pun's Current Comparator and Its Application to Full Flash and Two-Step Flash Current Mode ADCs

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A modification to an existing current comparator proposed by Tang and Pun has been presented. The circuit introduces a flipped voltage follower (FVF) which replaces the source follower input stage of the existing current comparator of Tang and Pun. This modification culminates into higher speed especially at lower currents and lower power dissipation. The application of the proposed current comparator has also been put forth by implementing a 3-bit current mode (CM) ADC and a two-step 3-bit CM ADC. The theoretical propositions are verified through spice simulation using 0.18 μm TSMC CMOS technology at a power supply of 1.8 V. Propagation delay, power dissipation, and power delay product (PDP) have been calculated for the proposed current comparator and process parameter variation has been studied. For both the implementations of ADCs, performance parameters, namely, DNL, INL, missing codes, monotonicity, offset, and gain errors, have been evaluated.

1. Introduction

Current comparator circuit finds application in a wide variety of applications like nonlinear current mode signal processing and analog to digital converters (ADCs). Besides, low level, high speed current detection is also required in different light and radiation sensing applications, or controllability and reconfigurability issues in E-beam testing of integrated circuits. Further, subthreshold CMOS current mode computation architectures also require efficient detection of low current levels. Another lucrative option is requirement of current detection in IDDQ VLSI testing approaches [1–7]. Hence, a considerable amount of effort has been expended by the circuit designers and researchers into the area of design of efficient current comparators.

The basic functionality of a current comparator is to determine which of the two currents (I_{in} or I_{ref}) is greater and to present that decision as one of two voltage levels, established by the output's (V_{out}) limiting values. The output value is typically interpreted as logic “1” and “0” for further processing [8]. One of the two currents is generally a constant

current called the reference current (I_{ref}) against which the input current is compared (I_{in}). This is shown by the following relation:

$$V_{\text{out}}(t) = \begin{cases} 1, & I_{\text{in}}(t) > I_{\text{ref}}(t) \\ 0, & I_{\text{in}}(t) < I_{\text{ref}}(t). \end{cases} \quad (1)$$

Numerous structures for current comparators have been put forth in the literature, of which the one proposed by Traff [9] (Figure 1(a)) can be considered a pioneering structure which adheres to all the characteristics desirable of a current comparator, namely, low input impedance, low-power dissipation, and moderate speed of operation.

It comprises a source follower input stage and a CMOS inverter. CMOS inverter provides positive feedback which helps achieve sufficient gain for amplifying small voltage variations at the input stage. This structure, however, suffers from a problem of a deadband region where in the input voltage to the inverter does not slew from rail to rail, making neither of the transistors in the source follower stage

FIGURE 1: (a) Traff's [9] current comparator; (b) Tang and Pun's [10] current comparator.

totally shutoff leading to nonzero DC power dissipation. To overcome this problem, a variety of modifications to the structure of Traff [9] have been presented in [10–17]. Of these, the one proposed by Tang and Pun [10] is the most significant one in terms of giving the fastest response at low input currents and resolution. Tang and Pun [10] modify the gain stage of Traff [9] by adding two more inverters (A_2) and (A_3) to its feedback path apart from already existing inverter (A_1) and source follower input stage M_{nf} and M_{pf} . A_2 and A_3 together act as a noninverting amplifier, in order to improve speed for low input currents. Circuit is depicted in Figure 1(b).

For a low input current, a small voltage change appears at the input node and node 1. However, amplification by A_2 and A_3 leads to significant change in the voltage at node 2, thus turning on input transistor M_{nf} or M_{pf} and activating the feedback loop. Hence the response time is considerably shortened.

In this paper, a modification to the circuit proposed by Tang and Pun [10] has been put forth. The input stage source follower has been replaced with a flipped voltage follower (FVF) cell. The authors have put forth a similar modification to Traff [9] in [18] and have obtained improved speed and power dissipation over the former. The similar approach has been adopted herein to modify Tang and Pun's [10] to develop a new current comparator structure. The proposed current comparator so developed has further been used to implement a 3-bit full flash and a two-step CM flash ADC.

2. The FVF Cell

The concept of FVF was put forth in [19]. The FVF, shown in Figure 2(a), is essentially a voltage follower with shunt feedback. It is low-power, low-voltage circuit having low impedance compared to basic source follower and current/voltage biasing. It employs two transistors M_1 and M_2 . The shunt feedback ensures that transistor M_2 remains always in on state independent of the power supply given to the

circuit. Further, due to current biasing the current through transistor M_1 is held constant and it also remains on [19, 20]. Thus change in output current does not affect the input current and V_{SG1} (which is a function of input current) remains almost constant across M_1 . This results in almost unity voltage gain or in other words output voltage follows input voltage. Further, since FVF can operate on very low supply voltage, it is a suitable structure of choice for design of low-power current comparator design.

The FVF can also be used as a current sensing cell, shown in Figure 2(b). Its operation can be explained as follows: When an input current is applied at node 1 with all transistors properly biased to work in the saturation region, then due to the shunt feedback provided by transistor M_2 , the impedance at the input node becomes very low and so the amount of current flowing into this node does not modify the value of the voltage developed at this node. Thus, the input node is capable of sourcing large current variations at the input and the FVF and then translates them into compressed voltage variations at output node 2.

3. Proposed Current Comparator

As mentioned before, Tang and Pun's [10] circuit is a high speed circuit capable of giving good response at lower currents. However, it cannot be considered a complete current comparator as it does not calculate the difference between the two currents (input and reference) but takes a precalculated current difference (I_{diff}) at its input. Hence, the performance parameters as quantified by Tang and Pun [10] are somewhat deficient and are set to alter when a current differencing unit is appended on the input side. Thus, in this paper a modification of Tang and Pun [10] has been put forth. This structure introduces twofold modification to Tang and Pun [10] by introducing the current differencing unit at the input side and the input source follower stage has been replaced with the FVF source follower stage to benefit from its advantages discussed in the previous section. Similar modification to Traff's [9] circuit has been proposed by the

FIGURE 2: (a) An FVF cell; (b) FVF current sensor [19].

FIGURE 3: Proposed current comparator.

authors in [20]. Figure 3 shows the circuit diagram of the implementation.

This implementation is a complete current comparator with the current differencing stage (Mc1-Mc12), gain stage (M1-M8), and the output stage (Mg1-Mg2). The current differencing unit accepts two currents I_{in} and I_{ref} and outputs current I_{diff} . The gain stage is a modification of the gain stage of Tang and Pun [10] wherein transistors (Mpf-Mnf) that form a source follower have been replaced by an FVF based source follower. The FVF source follower comprises transistors M1 and M2 and biasing current source (I_b) which keeps M2 on and a biasing voltage source (V_b).

This is followed by a CMOS inverter (Mpf-Mnf) connected to the FVF current sensor in the feedback loop with two passive elements, a resistor R and a capacitor C placed in series in this feedback loop. These together form the gain stage of the proposed current comparator. Finally, the

output stage is formed by a CMOS inverter Mg1-Mg2 that is connected to provide rail to rail swing at the output.

When I_{in} and I_{ref} are applied to the current differencing unit, it generates a current difference I_{diff} . This current applied to node Y of the gain stage is translated into corresponding voltage variations at node Z. When I_{diff} is negative, the voltage developed at node Y is small which leads to a high voltage at node Z due to the inverting action of the CMOS inverter M7-M8. Consequently, the output of the output stage, Mg1-Mg2, goes low and hence the overall output of the current comparator from the output stage, with rail to rail swing, is a low.

When a low I_{diff} is applied, it introduces a slowly rising voltage at node Y. This causes the output of the inverter M7-M8 to change slowly in response. Simultaneously, the current applied to node Y is translated into corresponding voltage variations at node "X". These small voltage variations

FIGURE 4: Output for proposed comparator for input current difference of $2 \mu\text{A}$.

at “X” are amplified by noninverting amplifier formed by M3-M4 and M5-M6, causing a change in the voltage at node Z which further activates the feedback loop, leading to faster switching. These inverters in the feedback path also serve to stabilize the voltage fluctuations at the output node V_{out} .

3.1. Simulation Results of the Proposed Current Comparator. The theoretical proposition is verified through SPICE simulations using $0.18 \mu\text{m}$ TSMC CMOS technology parameters and a supply voltage of 1.8 V . I_{in} of $3 \mu\text{A}$ with I_{ref} of $1 \mu\text{A}$ to obtain I_{diff} equal to $2 \mu\text{A}$ is used for all simulations. The functionality of current comparator is shown in Figure 4 along with that of Tang and Pun [10] under similar simulation conditions. The output voltage swing of 1.8 V is obtained with a propagation delay of 2.1 ns .

The variations of performance parameters, namely, delay, power dissipation, and power delay product (PDP) with input current difference, have been evaluated and depicted via plots below. Figure 6 depicts various plots for performance parameters versus input current difference, specifically variation of input current difference with respect to delay in Figure 5(a), power dissipation in Figure 5(b), and power delay product (PDP) in Figure 5(c). It is observed that the propagation delay reduces with increasing current difference due to faster charging/discharging of the node capacitance while the power dissipation increases with current. PDP follows a reducing pattern with increasing current. As can be clearly observed, the proposed comparator outperforms Tang and Pun’s [10] current comparator by being faster and power efficient thus offering a better PDP than the latter.

Process corner analysis was also carried out on the proposed comparator to study its behavior under extreme cases of process mismatch between PMOS and NMOS during manufacturing. The impact of parameter variations on the performance of the proposed comparator at different design corners is also studied and the corresponding results for delay and power dissipation are depicted in Figures 6(a) and 6(b), respectively. In this analysis, three corners exist, namely, typical, fast, and slow. Slow and fast corners exhibit carrier mobilities that are higher and lower than normal, respectively. Specifically, the corner FS represents fast NMOS and slow PMOS.

For the proposed current comparator, it is observed that the propagation delay is lower at the process corner FF while

the power dissipation is higher than at process corner TT. Similarly, for process corner SS, a higher propagation delay is observed while the power dissipation is lower than at process corner TT.

4. Current Mode Flash ADC

As an application of the proposed comparator, a 3-bit current mode (CM) flash ADC is implemented, as represented in Figure 7, wherein I_{in} and $I_{\text{ref}i}$ ($i = 1, \dots, 7$) represent input current and the reference currents of the i th comparator [21].

The value of $I_{\text{ref}i}$ is determined by the input current range and the number of bits (n) in ADC output

$$I_{\text{ref}i} = \frac{\text{Input current range}}{2^n - 1}. \quad (2)$$

The number of current comparators to be employed for 3-bit conversion is given by $2^3 - 1 = 7$. These current comparators receive progressively increasing reference currents ($I_{\text{ref}i}$) as per (2), and the input current (I_{in}) is mirrored to all the current comparators. Each comparator compares I_{in} to its respective reference current $I_{\text{ref}i}$. Hence all comparators perform the comparison in a single step in parallel, so this structure is also called a parallel ADC or a single step ADC. The output of the comparators represents a thermometer code which is then converted into the corresponding binary code by a 7×3 encoder block. The comparator outputs are C_7 (MSB) and C_6 to C_2 and C_1 (LSB). The encoder outputs are B_2 (MSB) and B_1 and B_0 (LSB), respectively.

A 7×3 CMOS encoder, shown in Figure 8, has been designed for thermometer to binary conversion which remains the same for all these CM flash ADCs.

The relation between comparator and encoder output is given by [21]

$$\begin{aligned} B_0 &= C_1 \oplus C_2 \oplus C_3 \oplus C_4 \oplus C_5 \oplus C_6 \oplus C_7, \\ B_1 &= \overline{C_4}C_2 + C_4C_6, \\ B_2 &= C_4, \end{aligned} \quad (3)$$

where $\overline{C_4}$ represents the complement of C_4 . The CMOS encoder circuit implemented is as shown in Figure 8.

4.1. Simulation Results of the CM Flash ADC. The functionality of the CM flash ADC has been demonstrated by simulations on PSPICE. The ADC response is shown in Figure 9 for ramp input, to evaluate the performance of the comparator in ADC application.

The ADC transfer characteristics are shown in Figure 10(a) plotted alongside the characteristics of an ideal ADC. The differential nonlinearity (DNL) is computed to be -0.15 LSB and is plotted as in Figure 10(b). It is clear that CM flash ADC I does not suffer from any missing codes and gives a monotonic response.

The CM ADC characteristics are redrawn in Figure 11(a) with a best fit line plotted alongside actual and ideal characteristics in order to compute integral nonlinearity (INL). The dotted line indicates the switching point where code

FIGURE 5: Variation of (a) delay, (b) power dissipation, and (c) power delay product versus current difference.

transitions should actually take place. The INL is calculated from Figure 11(a) and a maximum INL of -0.25 LSB is obtained, as plotted in Figure 11(b).

In order to compute the gain and offset error of this ADC, the best fit line for ideal and actual ADC transfer characteristics is plotted. The error at the first transition is evaluated to obtain the offset error, which in the current case is -0.1 LSB indicating that the first output transition code is obtained earlier than that expected ideally. The gain error is given by the difference in slope of actual best fit line and the ideal best fit line, which is also found to be 0.1 LSB for this implementation. Figure 11(c) depicts both these errors.

5. Two-Step Flash ADC

Another application of the proposed current comparator, a two-step flash ADC, is presented herein. Flash ADCs are usually the architectures of choice whenever there is a need for a fast conversion. This is so because the conversion is performed in one step; hence they can achieve very fast

conversion rates. However, they suffer from a drawback that the number of comparators to be employed increases exponentially with the increasing number of bits at the output. Since, for N -bit conversion, $2^N - 1$ comparators are necessary, hence the value of N increases, so does the number of comparators, thus making flash ADC a hardware extensive structure. To overcome some of these limitations of flash architecture and to take advantage of its high speed, two-step (semi-flash) architecture is often employed. Although popular in voltage mode, only a few applications of the same have been reported in CM [22–24].

The two-step method employs a coarse quantization in first step and a fine quantization in second step to obtain the desired resolution without extensively increased hardware. However, the speed is compromised as the output appears in two steps instead of parallel.

A 3-bit two-step CM flash ADC architecture is presented herein that produces the higher order 2 bits through coarse quantization and 1 bit (LSB) through fine quantization. The schema is illustrated in Figure 12.

FIGURE 6: Effect of process corner variation on (a) delay and (b) power dissipation.

FIGURE 7: A 3-bit CM flash ADC.

FIGURE 8: 7x3 CMOS encoder.

FIGURE 9: CM flash ADC output for ramp input.

FIGURE 10: (a) CM flash ADC transfer characteristics and (b) DNL versus output code.

A two-step 3-bit CM ADC comprises 4 current comparators, a 3×2 encoder, a 2-bit DAC, and a current differencing unit. This scheme gives the obvious advantages in terms of the reduced hardware. For a CM flash ADC, the number of comparators required is 7 which is reduced to 4 in this schema. The encoder size is also down to 3×2 as against 7×3 in the CM flash architecture. Even though a DAC and a subtractor have been included, yet the overall reduction in the total chip area outweighs the addition of these components.

The conversion takes place in two stages, with most significant bits, B_2 and B_1 , being generated in the first stage while the LSB, B_0 , is generated in the second stage depending on the output values obtained from the first stage.

In the first stage, it is required to obtain 2 bits at the output; hence, as in a CM flash ADC, $3 (2^2 - 1 = 3)$ current comparators are required. These current comparators compare the input current I_{in} to a progressively increasing

reference current I_{refi} , where the value of I_{refi} is determined as follows. A step size is calculated as

$$\text{Step} = \frac{I_{in \max} - I_{in \min}}{2^N - 1}, \quad (4)$$

where $(I_{in \min}, I_{in \max})$ is the input current range.

Based on the value of Step, I_{refi} is calculated as

$$\begin{aligned} I_{ref1} &= \text{Step} \times 2^1, \\ I_{ref2} &= \text{Step} \times 2^2, \\ I_{ref3} &= \text{Step} \times (2^1 + 2^2). \end{aligned} \quad (5)$$

The comparison of I_{in} against the respective I_{ref} by the three current comparators results in a 3-bit thermometer code. This code is then converted into corresponding binary code with the help of a 3×2 encoder which finally produces the two

FIGURE 11: (a) CM flash ADC transfer characteristic with best fit line, (b) INL versus output code, and (c) ideal and actual best fit line.

FIGURE 12: Two-step 3-bit CM flash ADC architecture.

higher order bits B_2 and B_1 . The relation between comparator and encoder output is given by

$$\begin{aligned} B_1 &= \overline{C_2}C_1 + C_3, \\ B_2 &= C_2, \end{aligned} \quad (6)$$

where $\overline{C_2}$ represents the complement of C_2 . The CMOS encoder circuit implemented is as shown in Figure 13.

In the second stage, the outputs from first stage B_2 and B_1 are converted into an analog signal given by I_o through a DAC. The value of I_o depends upon the combination of B_2B_1 as per Table 1.

A 1-bit DAC as employed for the purpose is shown in Figure 14(a) and its exemplary output is depicted in Figure 14(b). For 2 bits, two such structures are employed.

The DAC output I_o is then subtracted from I_{in} through a current differencing circuit identical to that used in the

FIGURE 13: 3×2 CMOS encoder.

FIGURE 14: (a) 1-bit DAC and (b) output response.

TABLE 1: DAC outputs.

B_2	B_1	I_o
0	0	0
0	1	$\text{Step} \times 2^1$
1	0	$\text{Step} \times 2^2$
1	1	$\text{Step} \times (2^1 + 2^2)$

design of the proposed current comparator. The output of this current differencing circuit serves as the input current for the

current comparator of second stage or 1-bit fine flash ADC. The 1-bit flash ADC for generating the LSB B_0 is simply a current comparator that compares the value of I_{in2} with I_{ref0} given by

$$I_{ref0} = \text{Step} \times 2^0. \quad (7)$$

The result of this comparison produces the LSB, hence completing the 3-bit conversion process. The second stage does not require an encoder in the present scenario as the output obtained is a single bit, that is, either a "0" or a "1." Had the number of bits required from the second stage been

FIGURE 15: Output of a two-step CM flash ADC based on proposed comparator.

FIGURE 16: (a) Transfer characteristics of two-step flash ADC using proposed comparator and (b) DNL versus output code.

TABLE 2: Step and I_{refi} values for $I_{in} = 2.5 \mu A$.

Step	I_{ref1}	I_{ref2}	I_{ref3}	I_{ref0}
$(3.5 - 0) / (2^3 - 1)$	0.5×2^1	0.5×2^2	$0.5 \times (2^1 + 2^2)$	0.5×2^0
0.5	$1 \mu A$	$2 \mu A$	$3 \mu A$	$0.5 \mu A$

more, an encoder would also have been required. Hence, the schema gets modified based on the required resolution of the ADC.

5.1. Simulation Results of the CM Flash ADC. The results are verified through simulations using PSPICE. For the purpose of simulations, the input current range has been taken to be $0-3.5 \mu A$. Hence, the various values as calculated using the relations described in (5) and (7) are as given in Table 2.

The values of I_o as obtained are $1 \mu A$, $2 \mu A$, and $3 \mu A$ for B_2B_1 “01,” “10,” and “11,” respectively.

A step input current value $I_{in} = 2.5 \mu A$ is applied to these ADCs. For this input, $C_3C_2C_1 = “011”$ and the encoder output $B_2B_1 = “10.”$ Also, as per Table 1, the value of I_o is $2 \mu A$. This value of I_o is then subtracted from I_{in} ($2.5 \mu A$) to obtain I_{in2} ($= 0.5 \mu A$). Finally, I_{in2} is compared to I_{ref0} by 4th current

comparator and an output “1” is obtained as B_0 (LSB). Hence for $I_{in} = 2.5 \mu A$ the ADC output obtained is “101.” The circuit response to the input current, $I_{in} = 2.5 \mu A$, is recorded in Figure 15.

The DNL and INL for this implementation of two-step CM flash ADC is found to be higher than its full flash counterpart. This is due to the residual inaccuracy that arises when output of one stage is cascaded to the next. The inaccuracy from first stage gets propagated to the next stage, leading to larger inaccuracy, thereby affecting the DNL and INL of the overall architecture [25].

In this case the DNL is found to be -0.3 LSB while INL of -0.5 LSB is obtained. Figures 16(a) and 16(b) illustrate the transfer characteristics of the two-step CM flash ADC and DNL versus output code curve of the same, respectively.

The INL calculation with respect to the best fit line has been depicted in Figure 17(a) while Figure 17(b) shows the variation of INL with respect to the output code.

Figure 17(c) depicts the best fit lines for ideal and actual transfer characteristics of this ADC to evaluate the offset and gain errors. An offset error of 0 LSB is observed at the first output code transition indicating that the first code appears at the same instance as ideally expected. The gain error is given

FIGURE 17: (a) Transfer characteristics with best fit line for two-step flash ADC using proposed comparator and (b) INL versus output code.

by the difference in slope of actual best fit line and the ideal best fit line at the last transition, which is found to be 0.1 LSB for this ADC.

6. Conclusion

A high speed, power efficient modification of Tang and Pun's current comparator employing FVF based input stage has been proposed. Performance of the proposed current comparator is compared to that of Tang and Pun's and the former outperforms the latter in terms of propagation delay, power dissipation, and PDP. The proposed current comparator has been employed to implement a 3-bit CM flash ADC and a two-step 3-bit flash ADC. The ADC performance parameters for both the implementations have been evaluated and are found to be satisfactory.

Competing Interests

The authors declare that they have no competing interests.

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