Research Article

A Mixed-Signal Programmable Time-Division Power-On-Reset and Volume Control Circuit for High-Resolution Hearing-Aid SoC Application

Chengying Chen ¹, Liming Chen,¹ and Jun Yang²

¹School of Opto-Electronic and Communication Engineering, Xiamen University of Technology, Fujian, Xiamen 361024, China

²School of Automation, Foshan University, Foshan 528000, China

Correspondence should be addressed to Chengying Chen; chenchengying363@163.com

Received 16 September 2017; Accepted 29 January 2018; Published 18 April 2018

Academic Editor: M. Jamal Deen

Copyright © 2018 Chengying Chen et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

A mixed-signal programmable Time-Division Power-On-Reset (TD-POR) circuit based on 8-bit Successive Approximation Analog-to-Digital Converter (SAR ADC) for accurate control in low-power hearing-aid System on Chip (SoC) is presented in this paper. The end-of-converter (EOC) signal of SAR ADC is used as the mode-change signal so that the circuit can detect the battery voltage and volume voltage alternately. And the TD-POR circuit also has brown-out reset (BOR) detection capability. Through digital logic circuit, the POR, BOR threshold, and delay time can be adjusted according to the system requirement. The circuit is implemented in SMIC 0.13 μm 1P8M CMOS process. The measurement results show that, in 1 V power supply, the POR, BOR, and volume control function are accomplished. The detection resolution is the best among previous work. With 120 Hz input signal and 15 kHz clock, the ADC shows that Signal to Noise plus Distortion Ratio (SNDR) is 46.5 dB and Effective Number Of Bits (ENOB) is 7.43 bits. Total circuit power consumption is only 86 μW for low-power application.

1. Introduction

With the development of VLSI integrated circuits, SoC becomes more and more complex, which not only consists of transitional analog circuits, but also comprises registers, memory, and Digital Signal Processing (DSP) circuits. When SoC is powered up, some of their internal nodes are with intermediate metastable states. Therefore at the initial stage of operation, a Power-On-Reset (POR) circuit is needed. The POR signal should hold circuits in the reset state until the power supply reaches a steady-state level when all the circuits can operate correctly. And, in many applications, when supply voltage suddenly drops, the SoC may malfunction. The POR circuit also needs to generate a brown-out reset (BOR) signal for warning or reset. The parameter definition of POR and BOR is shown in Figure 1.

V_{POR} and V_{BOR} are POR and BOR thresholds, respectively, which determine the system to enter or leave the stable state. DT_{POR} and DT_{BOR} are the delay time to generate the POR and BOR pulse when the supply voltage reaches V_{POR} or drops

under V_{BOR} , respectively. DT_{POR} and DT_{BOR} must be set long enough to confirm all the modules have entered steady or reset state. T_{BOR} and T_{POR} are the POR and BOR pulse width. As long as the DT_{POR} and DT_{BOR} meet the system specification, T_{POR} and T_{BOR} have no specific requirements. Transitional POR circuits are pure analog circuit that are based on delay cell and Schmitt Trigger [1–4]. Delay time is set by resistor and capacitor of delay cell occupying large chip area. The resistance and capacitance devices are affected by temperature, voltage, and other parameters in the process of integrated circuit, and the uncertainty of the delay time can be easily caused. At the same time, the fixed POR and BOR threshold are generated by the bandgap-based reference, which has a large temperature drift. So it can greatly affect the detection accuracy of the POR and BOR voltage that can hardly meet the high-resolution requirement.

The zinc-air battery that supplies hearing-aid SoC has a large voltage variation from 1.4 V to 0.7 V. When supply voltage reaches or drops to the right threshold, to ensure the accurate power-on control and low-voltage warning,

FIGURE 1: Parameter definition of POR and BOR.

the POR with ADC must be needed. Moreover V_{POR} and V_{BOR} as well as DT_{POR} and DT_{BOR} should be programmable due to battery characteristic. Meanwhile the customers may adjust the volume of hearing-aid device according to the environment and their hearing condition. And the volume adjustment usually has 32 stages. For precision, an 8-bit ADC with 256 quantized steps is used to divide the adjustment stages. Since the power determines the operation duration of hearing-aid SoC and both supply voltage and volume voltage are 1V, to minimize the power consumption and realize accurate control, a mixed-signal programmable TD-POR and volume control circuit based on SAR ADC for hearing-aid SoC is presented in this paper. The EOC signal of SAR ADC is used as the mode-change signal so that the circuit can detect the battery voltage and volume voltage alternately, which reduces both circuit size and total power consumption.

2. System Design Considerations

Figure 2 shows the architecture of the proposed TD-POR and volume control circuit, which consists of Time-Division input stage, 8-bit SAR ADC, clock generator, LDO, and digital logic circuit. The input stage comprises a MUX, two resistors (R_1 , R_2), and a MOS capacitor. MUX controlled by EOC signal inputs battery voltage (bat_level) and volume voltage (vc_level) alternately. The ratio of R_1 and R_2 is 2:3. Since in 1V power supply the voltage range of battery and volume is 0-1V, the two resistors' mechanism reduces the voltage detection range to 0-0.6V to minimize the detection error. And the MOS capacitor in input stage is used to provide a

channel for high frequency power supply ripple to ground and relieve the noise effect.

A complete SAR ADC conversion cycle requires 12 clock cycles, where three clock cycles are for sampling, eight cycles are for a binary searching, and half cycle is for EOC signal. Common mode voltage 0.5V and reference voltage 0.6V are provided by the LDO circuit. Clock generator provides 15kHz frequency signal for ADC. EOC is divided into two outputs: one is input to the clock port of a D flip-flop. And the output of the D flip-flop controls input stage of MUX which completes the input switching. At the same time the output of the D flip-flop goes through an inverter and then generates Time-Division multiplex flag signal Vc_bat_mux . And Vc_bat_mux is output to the digital logic circuit (when Vc_bat_mux is high, the input voltage signal is the volume signal; when Vc_bat_mux is low, the input voltage signal is the battery signal). The second output of EOC goes through a delay buffer to clock ports of eight D flip-flops, which maintains the ADC 8-bit output data for a conversion cycle. Meanwhile, the output of the delay buffer is delayed by seven clock cycles and generates a digital logic read flag signal $Data_en$, to ensure the output can be read by digital logic circuit correctly. Finally the 8-bit ADC output codes $Out\langle 7:0 \rangle$ are maintained by D flip-flops for a SAR ADC conversion cycle until the next EOC signal arrives.

The inputs of digital logic circuit are 8-bit ADC output code, $Data_en$, Vc_bat_mux , 4 bit V_{POR} , and 2 bit V_{BOR} . The final outputs of digital logic circuits are POR counting signal cnt_en and POR (BOR) signal $Soft_rst$. Firstly V_{POR} is set after initialization. When the battery voltage starts to rise and exceeds V_{POR} , cnt_en starts counting. If the voltage is greater than V_{POR} and lasts for 30 ms, $Soft_rst$ turns to high value; when the battery voltage drops to V_{BOR} and also lasts for 30 ms, $Soft_rst$ turns to low value and makes system enter the reset state. According to signal Vc_bat_mux , TD-POR circuit determines whether the battery voltage or volume voltage is read at this time. When Vc_bat_mux is high, the 8-bit ADC output codes will be output to the DSP for volume control. And when Vc_bat_mux is low, the circuit runs into the POR mode. Timing relationships of $Data_en$, $Out\langle 7:0 \rangle$, and Vc_bat_mux are shown in Figure 3, $vc0$, $vc1$, ... represented the volume voltage, and $bat0$, $bat1$, ... indicated the battery voltage.

3. Circuit Design

The core of POR circuit is an 8-bit SAR ADC as shown in Figure 4, including sample/hold circuit, analog-to-digital converter (DAC), comparator, successive approximation logic circuit, and timing generator [5-9].

Figure 5 shows the circuit of 8-bit charge redistribution DAC. To meet the requirement of full-swing input, only one sampling capacitor (C_s) of 32 times unit capacitor is adopted [10].

The DAC has two phases as sampling phase and charge redistribution phase. When DAC is in sampling phase, the switches $S_0 \sim S_7$ are connected with GND. The switch S_{sample} is connected with V_{IN} . And S_{vcm} is also on, so the

FIGURE 2: Block diagram of Time-Division Power-On-Reset and volume control circuit.

FIGURE 3: Analog circuit outputs timing.

FIGURE 4: Block diagram of SAR ADC.

FIGURE 5: DAC structure.

FIGURE 6: Comparator structure and circuit.

lower plate and the upper plate of C_s are connected with V_{IN} and V_{CM} , respectively. Therefore the output of DAC is

$$V_x = \frac{Q_x}{C_t} = \frac{32C(v_{cm} - v_{in}) + v_{cm}(7C//1C + 31C)}{7C//1C + 63C} \quad (1)$$

$$= -\frac{256}{511}v_{in} + v_{cm}.$$

When DAC is in charge redistribution phase, the Most Significant Bit (MSB/7th bit) is initialized as "1" and the switch S_7 is connected to reference voltage V_{REF} . At this time if the input voltage (V_{IN}) is greater than half of V_{REF} , the comparator output is "0" and the MSB stays as "1"; otherwise the MSB changes to "0." After that the 6th bit is initialized as "1" and S_6 is connected to V_{REF} . Then the 6th bit can be "1" or "0" which depends on the output of comparator. The DAC needs eight cycles until the Least Significant Bit (LSB) is determined. And the DAC output is

$$V_x = \frac{256}{511} \left(-v_{in} + \sum_{i=1}^8 \frac{b_i}{2^{9-i}} v_{ref} \right) + v_{cm}, \quad (2)$$

where b_i is the i bit output of DAC.

The comparator is shown in Figure 6, which comprises three preamplifiers and an output latch. The three preamplifiers with input offset reduction and output offset reduction techniques can relieve the effect of offset voltage efficiently. The output latch is adopted to change the differential output into single output and hold the output [11, 12].

SAR logic circuit is the most important part of SAR ADC. It realizes the feedback control of DAC. A complete ADC conversion requires twelve clock cycles, including two sampling

cycles, nine successive approximation cycles, and one end-signal generation cycle. The SAR logic circuit comprises D flip-flops, inverters, AND gates, and JK flip-flops, as shown in Figure 7. $F_0 \sim F_7$ are 8-bit SAR logic registers made up of JK flip-flops. FS , GA , and GB constitute the start-up circuit, and timing generator consists of $FA \sim FJ$. EN is start-up signal lasting for two clock cycles. V_c is the comparator output. EOC is the end-of-converter signal. $D_7 \sim D_0$ are DAC input signal and $b_7 \sim b_0$ are the digital output of ADC [13].

The timing of POR signal is shown in Figure 8. The signal sample is a three-cycle sampling signal. EN is the start-up signal of SAR logic circuit. And reset and lat are the reset signal of preamplifier and latch, respectively.

4. Experiment Result

The proposed TD-POR circuit has been implemented in $0.13 \mu\text{m}$ CMOS technology with 1 V supply. The chip is shown in Figure 9. The power consumption and the core chip area are $86 \mu\text{W}$ ($28 \mu\text{W}$ @ LDO, $25 \mu\text{W}$ @ SAR ADC, $20 \mu\text{W}$ @ oscillator, and $13 \mu\text{W}$ @ others) and 0.175 mm^2 (0.675 mm^2 including IO cells), respectively. Figures 10 and 11 show the measurement results. When the input signal V_{p-p} is 800 mV, the input frequency is 120 Hz and the clock frequency is 15 kHz, the FFT spectrum of ADC output signal is analyzed, the SNDR is 46.5 dB, and ENOB reaches 7.43 bits. As shown in Figure 11(a), when the voltage exceeds V_{POR} (800 mV), cnt.en turns to high value and starts counting. When its counting exceeds 30 ms, which meets the POR condition, Soft_rst turns to high value and completes the power-on process. In Figure 11(b) when the battery voltage drops below V_{BOR} (910 mV), and cnt.en counts for 30 ms; Soft_rst turns to low value to reset the system.

FIGURE 7: SAR logic circuit.

FIGURE 8: Timing of POR circuit.

FIGURE 10: FFT measurement result of SAR ADC.

FIGURE 9: Chip of the proposed circuit.

The performance summary of the proposed Time-Division Power-On-Reset and volume control circuit is given in Table 1, and the performance comparisons with published

POR circuits are also listed. The circuit designed in this paper is the only one POR circuit, which can be configured with V_{POR}/V_{BOR} and delay time, and has high flexibility. It also has the highest detection accuracy. But due to the ADC-based structure the chip area is larger than other circuits.

In order to optimize power consumption, because the frequency of both POR and volume control signal is low, a suitable clock signal frequency is used to reduce DAC activity, thus decreasing the dynamic switching power. On the other hand, near-threshold transistors are adopted to design preamplifiers and comparators that save much power than their saturation opponents. Since the power dissipation of traditional analog volume control circuit is in hundreds of microwatts, our work puts forward a Time-Division multiplexing way, which completes the two functions of POR/BOR

FIGURE 11: Function of measurement: (a) Soft_rst for a POR event; (b) Soft_rst for a BOR event.

TABLE 1: Comparison with previous work.

Parameters	This work	[1]	[2]	[4]
Process	CMOS 0.13 μm	CMOS 0.18 μm	CMOS 0.5 μm	CMOS 0.25 μm
Supply	1 V	1.8 V	1.8–5 V	2.5 V
BOR detection	Yes	Yes	Yes	No
$V_{\text{POR}}/V_{\text{BOR}}$	Programmable	Fixed	Fixed	Fixed
Delay time (30 ms in this paper)	Programmable	Fixed	Fixed	Fixed
ADC function	Yes	No	No	No
Other functions	Volume control	No	No	No
Detection resolution	<4 mV	NA	NA	NA
Power consumption	25 μW (core)	1.8 μW	115.5 μW	125 μW
Active size	0.175 mm^2	0.012 mm^2	0.001925 mm^2	0.0396 mm^2

and volume control through a single circuit, and it also has excellent power consumption and detection performance.

5. Conclusion

A mixed-signal programmable TD-POR and volume control circuit for hearing-aid SoC is proposed in this paper. It uses the EOC signal of SAR ADC as the mode-change signal that makes circuit detect the battery voltage and volume voltage alternately. And the POR and BOR function are both included. The mixed-signal structure ensures flexible configuration of $V_{\text{POR}}/V_{\text{BOR}}$ and delay time, which greatly improve the stability of the application system. The circuit is implemented in SMIC 0.13 μm 1P8M CMOS process. The measurement results show that, in 1 V power supply, the POR, BOR, and volume control function are accomplished. With 120 Hz input frequency and 15 kHz clock frequency, the ADC shows that SNDR is 46.5 dB and ENOB is 7.43 bits. Total circuit power consumption is 86 μW . And the circuit shows the best detection resolution among all references.

Conflicts of Interest

There are no conflicts of interest related to this paper.

Acknowledgments

This work is supported by the National Natural Science Foundation of China (Grant no. 61704143), Young and Middle-Aged Teacher Education Research Project of Fujian Province (Grant no. JAT170428), and High-Level Talent Project of Xiamen University of Technology (Grant no. YKJ17019R).

References

- [1] H.-B. Le, X.-D. Do, S.-G. Lee, and S.-T. Ryu, "A long reset-time power-on reset circuit with brown-out detection capability," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 11, pp. 778–782, 2011.
- [2] K. Shu, E. Sánchez-Sinencio, J. Silva-Martínez, and S. H. K. Embabi, "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 866–874, 2003.
- [3] ADM709 Data Sheet, Analog device, Power Supply Monitor With Reset.
- [4] T. Yasuda, M. Yamamoto, and T. Nishi, "A power-on reset pulse generator for low voltage applications," in *Proceedings of the 2001 IEEE International Symposium on Circuits and Systems, ISCAS 2001*, pp. 598–601, Australia, May 2001.

- [5] X. Han, Q. Wei, H. Yang, and H. Wang, "A single channel, 6-bit 410-MS/s 3bits/stage asynchronous SAR ADC based on resistive DAC," *Journal of Semiconductors*, vol. 36, no. 5, Article ID 055010, 2015.
- [6] R. Ma, W. Bai, and Z. Zhu, "An energy-efficient and highly linear switching capacitor procedure for SAR ADCs," *Journal of Semiconductors*, vol. 36, no. 5, Article ID 055014, 2015.
- [7] Z. Zhu, Y. Xiao, and X. Song, " V_{CM} -based monotonic capacitor switching scheme for SAR ADC," *IEEE Electronics Letters*, vol. 49, no. 5, pp. 327–329, 2013.
- [8] Y. Zhu, C.-H. Chan, and U.-F. Chio, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, 2010.
- [9] L. Qin, *Research and design of 11-bit SAR ADC based on reused terminating capacitor switching procedure. [Master thesis]*, Zhejiang University, 2012.
- [10] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "A 1- μ W 10-bit 200-kS/s SAR ADC with a bypass window for biomedical applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, 2012.
- [11] P. Harpe, E. Cantatore, and A. van Roermund, "A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/conversion-step," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3011–3018, 2013.
- [12] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1V 3.8 μ W 100kS/s SAR ADC with time-domain comparator," in *Proceedings of the 2008 IEEE International Solid State Circuits Conference, ISSCC*, pp. 246–237, USA, February 2008.
- [13] N. Verma and A. P. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1196–1205, 2007.