Hindawi
Journal of Electrical and Computer Engineering
Volume 2018, Article ID 7245039, 12 pages
https://doi.org/10.1155/2018/7245039

Research Article

A Novel Hybrid T-Type Three-Level Inverter Based on SVPWM for PV Application

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Received 22 January 2018; Revised 6 April 2018; Accepted 17 April 2018; Published 3 June 2018

Academic Editor: Yongheng Yang

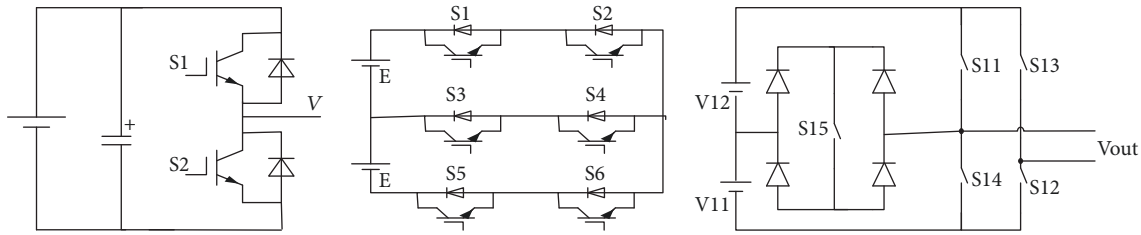
We describe several, recently reported, new topologies and compare them with each other, in order to find out the optimal multilevel grid-connected inverter topology. Then, we classify these topologies according to the basic unit which predecessors proposed. Eventually, we propose the hybrid T-type inverter topology structure, which is composed of two best basic units. This structure takes full advantage of the two components, to reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system. At the same time, the space vector pulse width modulation (SVPWM) method is used to simulate the proposed topology in the MATLAB/SIMULINK platform, while the loss of each semiconductor switch is calculated using MELCOSIM software. The results show that the proposed structure is superior to the most widely used topology, i.e., the diode clamped and the T-type three-level circuits.

1. Introduction

Nowadays, the contradictions between the consumption pattern of the traditional petrochemical energy and the economic development and environmental protection are becoming more and more prominent. People gradually realize the importance of taking sustainable development road, vigorous developing, and utilizing of the renewable energies. Among the renewable energies, the solar energy represents the largest and the most commonly distributed resource. The photovoltaic power generation technology using the solar cells effectively absorbs the solar energy and changes it into electricity. The grid-connected inverter is the key component and important equipment in a photovoltaic grid-connected system.

In the design of general inverters, synthetically considering the cost-effective factors, insulated-gate bipolar transistor (IGBT) represents the most employed device. However, due to the nonlinearity of the IGBT's conduction voltage drop, it does not significantly increase with the increase of current, thus ensuring that the inverter still presents a relatively low loss and high efficiency at the maximum load condition. However, since the European efficiency is mainly related to the efficiency of the inverter at different light-load, the aforementioned characteristics of the IGBT represent the disadvantage of the photovoltaic grid-connected inverter. For light loads, the turn-on voltage drop of the IGBT does not significantly reduce, which in turn reduces the European efficiency of the inverter. In contrast, due to linear conduction voltage drop of the MOSFET, it provides lower turn-on voltage drop for light loads. Considering the excellent dynamic characteristics and high frequency work ability, MOSFET becomes the first choice for photovoltaic inverting [1].

Three-level inverter has been widely used in the middle and high voltage large capacity AC speed regulating fields, since its output has higher power quality, lower harmonic contents, better electromagnetic compatibility, lower switching losses, and other advantages. However, it still suffers from some key problems, including the simplification of the three-level algorithm, neutral point voltage control in the overmodulation region, and the stability of the system at high voltage. In view of the above problems, this paper studies



(a) Basic unit A (b) Basic unit B (c) Basic unit C

Figure 1: Basic unit of the inverter.

the structure and principle of the three-level inverter, the control of the neutral point voltage of the capacitor, and the realization of the SVPWM algorithm.

In this paper, we study novel T-type inverter topology in PV system using SVPWM control algorithm. The structure is organized as follows: Section 2.1 introduces basic cells of the new multilevel PV inverters and classifies them. Section 2.2 presents and compares new types of multilevel inverters. Section 2.3 analyzes and compares switch losses and conversion efficiency of diode clamped T-type and proposed hybrid T-type. Section 2.4 details SVPWM control algorithm. Section 3 gives simulation results. Finally, Section 4 concludes the paper.

2. Materials and Methods

2.1. Basic Unit. Inverter basic unit refers to the minimum component that meets the demands of the topological multilevel grid-connected inverter. Odeh [2] proposed one basic concept of the basic unit of multilevel grid-connected inverter.

As shown in Figure 1(a), after achieving the basic unit, it may be extended in form of series-parallel and parallel-series connections to present higher voltage levels. Odeh [3] analyzes the connection between the topologies of the multilevel grid-connected inverters and proposes a regular pattern that is followed when general multilevel grid-connected inverter topology simplifies to other multilevel grid-connected inverter topology. For example, the main switches must be all maintained, all switching devices must be deleted symmetrically, diodes and capacitors must be distributed symmetrically, and so on. With the development of power electronic devices, in order to unify the pressure drop of the power electronic switch transistors, a more practical basic unit is put forward.

Figure 1(b) shows the stacked commutation cells or three-pole cells. As the employed conduction strategy, one of the two transistors in the outer leg is in a frequent switching state only during half-cycle, while the other transistor is switched only once during the fundamental wave period, which greatly reduces the switching loss. This conduction strategy also avoids the voltage-equalization problem caused by the simultaneous turn-on and turn-off of the series devices. Figure 1(c) shows the structure of a multilevel inverter basic unit reported by Draxe et al. [4]. This inverter is formed using five switches with antiparallel diodes, where S11 to S14 are arranged as the traditional CHB inverter, while, however, S15 is added to increase the output voltage levels by selecting the appropriate voltage source. This structure produces higher voltage levels with minimum number of switches by optimizing the circuit layout and reducing the gate drive circuitry.

Recently reported inverter topologies aim to reduce the number of the power electronic devices to improve the conversion efficiency. Figure 2 shows the classification of the inverters based on their topologies. As we see from this figure, the largest portion of the proposed inverter topologies formed by the basic unit A, due to its relatively simple construction. The topologies composed of basic units B and C have not yet appeared because of their complex basic constitution unit.

The basic unit of the inverter consists of a DC power supply and a pair of switches. By using the same basic unit, taking Figure 1(a), for example, in the form of series-parallel combinations a new circuit topology, as shown in Figure 3, called single phase H-bridge topology, is obtained. Or by series-parallel combinations between different basic units also a new one is got. For instance, three parallel basic units A and one basic unit B constitute the three-level T-type inverter topology, as shown in Figure 4. Different multilevel inverters can be obtained by multiseries and multiparallel connections of multiple basic units. And the construction of the other topologies in Figure 2 can be deduced by the same analogy.

2.2. New Type Inverter Topology. The work in [5] proposed the split capacitor H-bridge (SC-HB) inverter topology. Adding a simple DC-DC converter, this topology overcomes the capacitance-voltage balance problem, while reducing the leakage current, with improved efficiency. The work in [2] presented the improved cascaded H-bridge topology which consists of a half-bridge level latching circuit and a main inverter H-bridge. Thus, it reduces the number of the devices, switching loss, and harmonic content. An asymmetric cascaded H-bridge topology, with different, and proportional, DC voltage source values is reported in [4]. This reduces the capacity and number of the devices, as well as the costs. A sine-wave pulse width modulation (SPWM) three-phase multilevel inverter topology may be achieved by inserting two auxiliary switches in each phase bridge to change the basic two-level to three-level inverter to synthesize higher levels [3]. In comparison with traditional diode clamps, flying

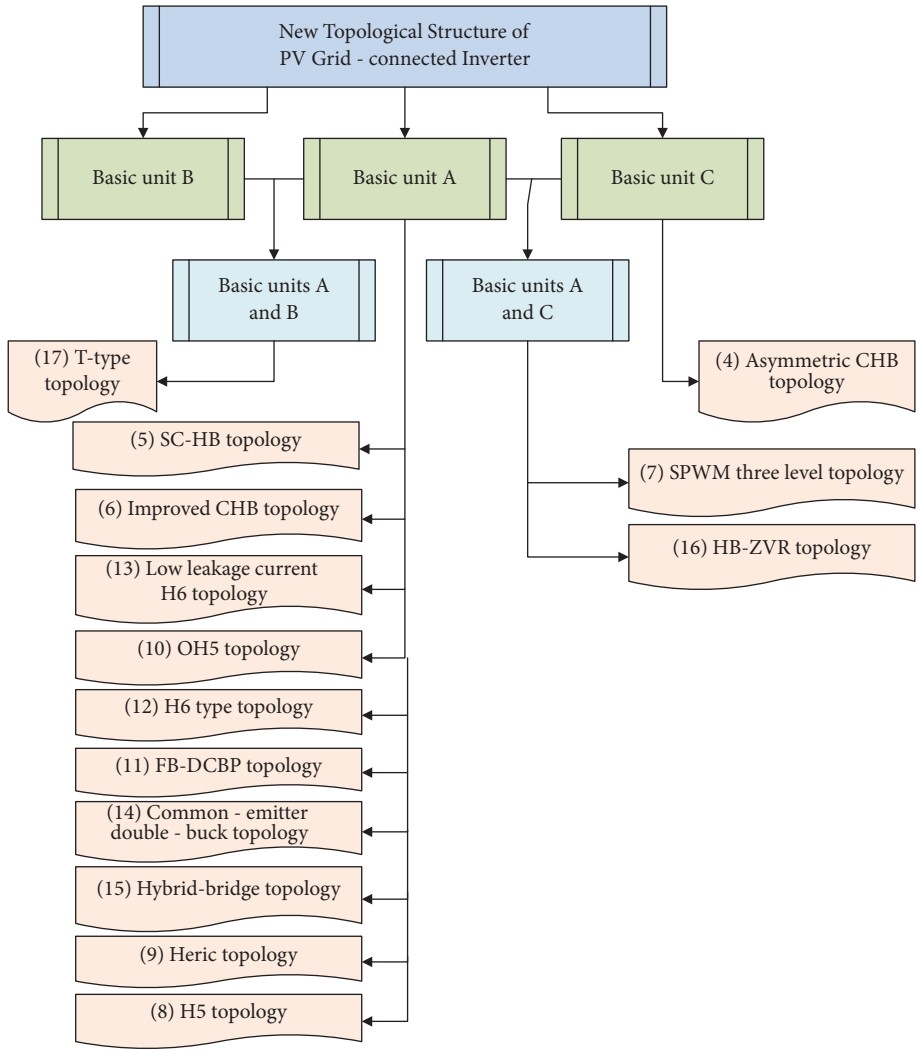
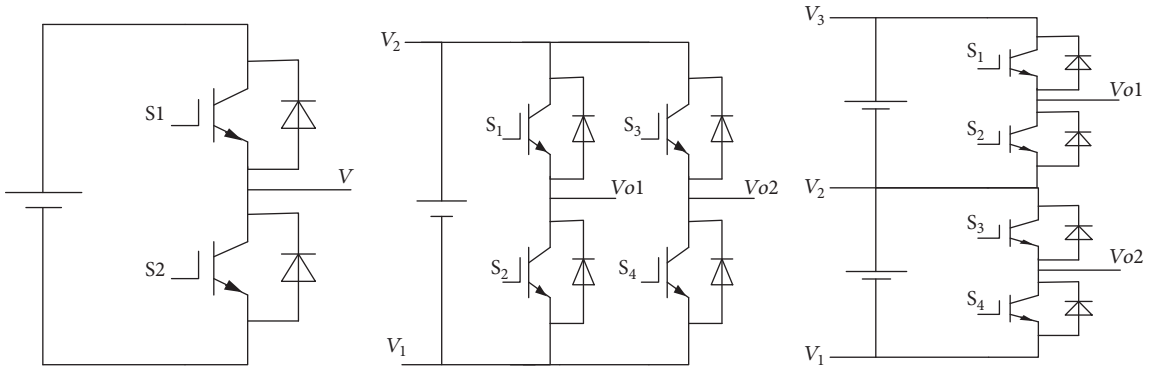


Figure 2: Per-phase circuit configuration of the conventional multilevel inverter.



(a) Basic unit A (b) Parallel-connection (c) Series-connection

Figure 3: Parallel-series-connection topology of the same basic units.

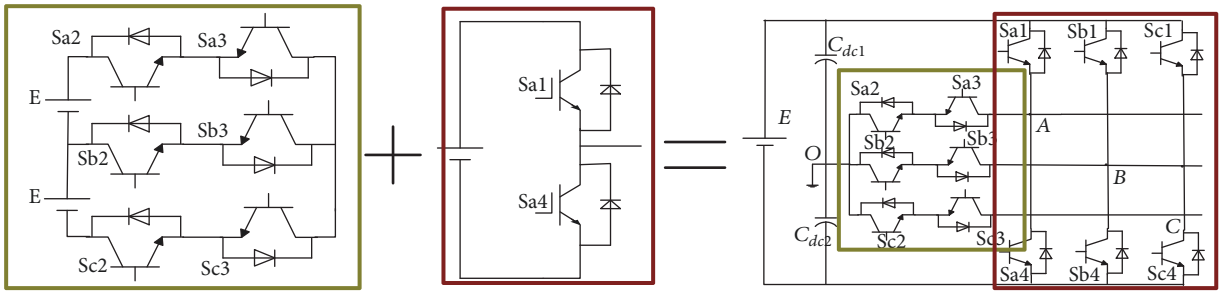


Figure 4: Parallel-series-connection topology of the different basic units.

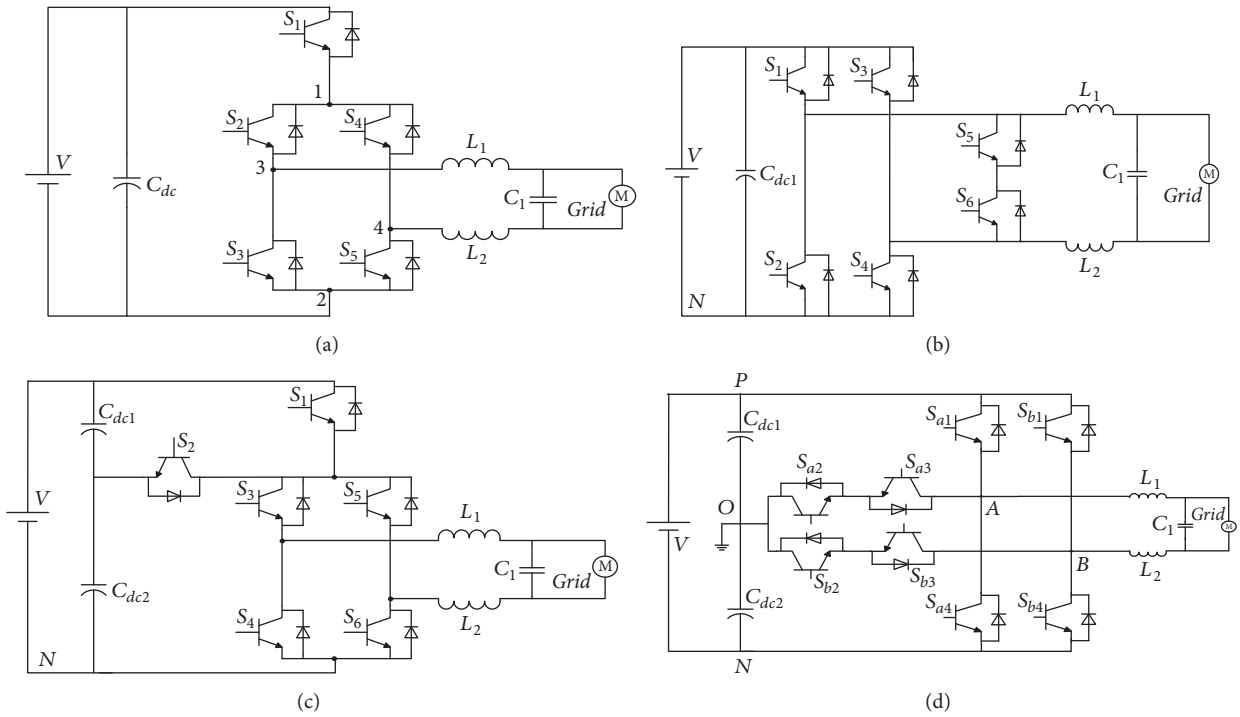


Figure 5: Some new topology structure. (a) H5 topology, (b) Heric topology, (c) OH5 topology, and (d) T-type topology.

capacitors, and cascaded H-bridge inverters, this topology uses only a DC power supply and lower power electronics providing the same number of the levels.

Figure 5(a) shows the H5 topology [6], composed of a freewheeling circuit by adding a high frequency switch in the positive end of the DC input side, where the efficiency may reach up to 98.1%. However, it suffers from big loss and heat and unbalanced thermal stress. Figure 5(b) shows the structure of the Heric topology [7], where a new freewheeling circuit is added, which itself is composed of a set of bidirectional switch branches on the AC side, based on the traditional full-bridge inverter topology. The efficiency of this topology may reach more than 98%. The OH5 topology is shown in Figure 5(c) [8], which uses a switch and capacitor to form the bidirectional clamping circuit on the basis of the H5 topology, which greatly inhibits the leakage current, and improves the conversion efficiency. However, in such a structure, the clamping circuit is constrained by the dead time of the switch, and a large on-state loss is presented. The work in [9] proposes the FB-DCBP topology, which achieves the complete elimination of the leakage current by adding two controllable switch and clamp diodes in the DC side to format the clamping circuit. The leakage current suppression capability of this topology is stronger than that of the H5 and Heric topologies but suffers from large on-state loss and high number of devices, providing the maximum efficiency of 97.4%.

H6-type topology is proposed in [10], and it is a variant of the Heric topology. It does not require setting dead time between the switches of the same bridge arm and does not pass through the body diode of the switch. Therefore, all switches may be formed by MOSFET, but the topology requires extra two freewheeling diodes, so the cost is increased. Moreover, the efficiency is lower than the Heric topology, and the efficiency is up to 97.6%. The low-leakage current H6 topology is reported in [11], which is a compromise between the H5 and Heric topologies. A new freewheeling circuit is formed based on the H5 topology by adding a switch to make the number of switches through two

half-frequency cycles of the network current at power transfer mode not the same, yielding reduced on-state loss. The efficiency of the H6 topology is lower than that of the Heric topology and higher than that of H5 topology. The common mode is inferior to H5 topology and superior to Heric topology. A common emitter double BUCK topology may be considered [12], composed of four controllable switches and two diodes. The leakage current of this structure is basically zero, and there is no high frequency dead zone between the switches. In addition, this structure presents no breakthrough phenomenon, high reliability, and small switching loss, where the efficiency may reach more than 98.5%. However, the topological magnetic component utilization is low and cannot output reactive current.

The hybrid bridge topology proposed in [13] consists of six controllable switches and two freewheeling diodes. This topology moved the switch on the AC side of the Heric topology to the middle of the bridge arm A, similar to H6-type topology. HB-ZVR (H-bridge zero-voltage state rectifier) topology is proposed in [14], introducing an AC bypass circuit, which itself is composed of a IGBT and a group of diode rectifiers, which is clamped to the midpoint of the two capacitors on the DC bus, to achieve low common mode current and high efficiency inverter topology. The HB-ZVR topology solves the problem that bidirectional switches S5 and S6 of the Heric topology cannot turn on, and this topology will always find a way in the bidirectional switch. Figure 5(d) shows the T-type inverter topology [15], formed by a set of switches Sa3/Sa4 as a bidirectional switch to achieve the main switch Sa1/Sa2 clamping function. It uses the clamp diodes or clamp bit capacitance to improve the midpoint clamping circuit, reducing the number of devices and uneven distribution of the loss. In the topological selection, T-type three-level circuit leverages many advantages of the nonisolation technology as well as the multilevel technology. Therefore, it is very suitable for the photovoltaic grid-connected power generation occasions; however, it is required to effectively suppress the circuit leakage current and system efficiency.

By comparing the above different new topologies, we see that the proposed multilevel inverter topology optimizes the performances of the inverter by adding auxiliary/clamping circuit, using hybrid switch or asymmetric structure.

Figure 6 shows the topology of the hybrid T-type inverter, which is on the basis of T-type structure and composed of nine MOSFET switches, i.e., Sa2, Sb2, Sc2, . . ., Sa4, Sb4, Sc4. We choose IGBT for Sa1, Sb1, and Sc1, since the reverse recovery ability of the body diode in the field effect transistor is poor; therefore they act in low frequencies. The high frequency MOSFET semiconductor switches, i.e., Sa2, Sb2, Sc2, . . ., Sa4, Sb4, Sc4, provide good switching characteristics and low on-resistance. Moreover, due to the low speed characteristics of the built-in diode of MOSFETs, MOSFET cannot be used in the upper bridge arm. We take advantage of the two devices, to reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system.

2.3. Loss Analysis of the Proposed Topology. The high power inverter works in high voltage and large current situations,

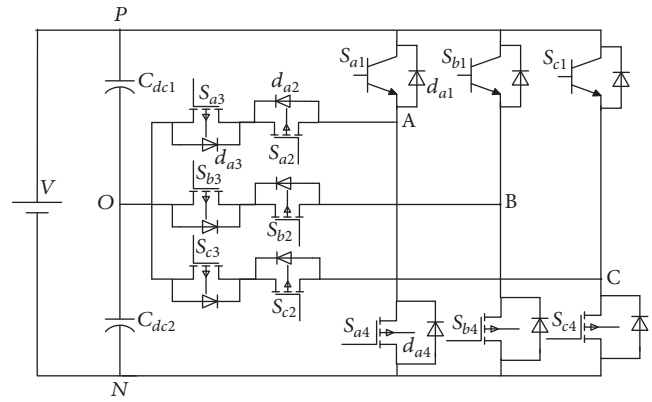


Figure 6: The proposed hybrid T-type inverter.

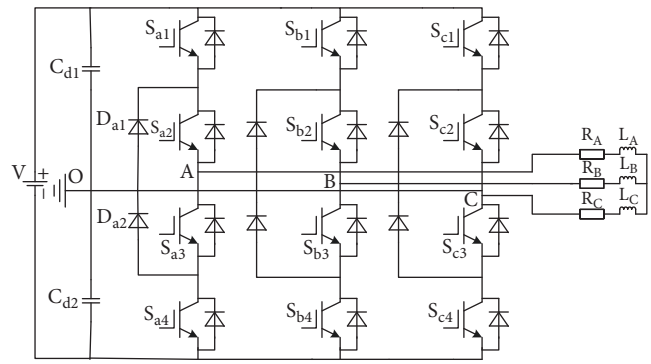


Figure 7: Diode clamped three-level inverter.

where various losses caused by the opening device are relatively large. Besides, optimization of the switching characteristics of the power electronic devices yields bigger conduction losses of the system, especially for soft switching technology, where the switching loss of the power electronic devices is reduced, and the source of the power loss is converted to the conduction loss [16]. Therefore, it is a key step to accurately calculate the state loss for the design of grid-connected inverter systems. Take A phase of Figures 6 and 7 as an example, we compare the various losses of diode clamped (Figure 7) and hybrid T-type (Figure 6) inverter losses and their conversion efficiency. We assume that the output current of the grid-connected inverter is an ideal sine wave; the output voltage of the inverter integrates the conduction period in the period T. Then, the conduction losses per device may be expressed as

$$P_{s_{a1}} = \frac{1}{2\pi}\left[\int_0^{\pi-\theta} d(\omega t)\, U_{\text{com}}(i)\left(I_{\text{com}} \sin(\omega t)\, d(\omega t)\right)\right] \quad (1)$$

where $P_{s_{a1}}$ is the conduction loss of the per device, $d(\omega t)$ is the duty cycle, $U_{\text{com}}(i)$ represents the conduction voltage drop of the IGBT, I_{com} denotes the conduction current peak of the IGBT, and ω is the angle speed. The integral interval from 0 to π-θ is a chopper phase of the semiconductor switch Sa1 in

a fundamental period. The conduction loss of the antiparallel diode in the IGBT reads

$$P_{da1} = \frac{1}{2\pi}\int_{\pi-\theta}^{\pi}\left(-m * \sin\left(\omega t + \phi\right)\right)\left[U_{od}I_{\text{com}}\sin\left(\omega t\right) + R_{od}\left(I_{\text{com}}\sin\left(\omega t\right)\right)^2\right]d\left(\omega t\right) \quad (2)$$

where P_{da1} is the conduction loss of the antiparallel diode in the IGBT, m is the modulation index, Φ is the output power factor angles, and R_{od} and U_{od} are the conduction pressure drop constants of the antiparallel diode.

When IGBT/MOSFET is turned off, the current flows from the clamped diodes and then reads the following clamped diode conduction loss:

$$\begin{aligned} P_{Da1} = {} & \frac{1}{2\pi}\int_{0}^{\pi-\theta}\left(1 - m * \sin\left(\omega t + \phi\right)\right) \\ & \cdot\left[U_{dt}I_{\text{com}}\sin\left(\omega t\right) + R_{dt}\left(I_{\text{com}}\sin\left(\omega t\right)\right)^2\right]d\left(\omega t\right) + \frac{1}{2\pi} \\ & \cdot\int_{0}^{\pi-\theta}\left(1 + m * \sin\left(\omega t + \phi\right)\right)\left[U_{dt}I_{\text{com}}\sin\left(\omega t\right) + R_{dt}\left(I_{\text{com}}\sin\left(\omega t\right)\right)^2\right]d\left(\omega t\right) \end{aligned} \quad (3)$$

where U_{dt} and R_{dt} are the conduction pressure drop constants of the clamped diode.

We considered the DC side voltage of 700 V, carrier frequency fc of 5 kHz, gate resistance of 1.65 ohm, output frequency equal to 60 Hz, modulation rate of unity, and power factor of 0.8. We used MELCOSIM software to simulate the loss. Table 1 presents the calculated loss of different components.

In Table 1, the power losses of Sa1 and Sa4 as well as Sa2 and Sa3 IGBT switches are identical. The four antiparallel diode power dissipations, da1, da2, da3, and da4, are also identical. Moreover, clamping diodes, Da1 and Da2, have the same loss. Table 2 lists the overall loss of the two topologies, which may be calculated based on the number of components contained in two topologies. This table also presents the total power of the inverter, which is 10 kW, and the conversion efficiency of each topology.

The conversion efficiency is lower than 90% because of the higher switching frequency. We chose the frequency of 10 Khz MOSFET, and the switching frequency is relatively high; at the same time the switching loss itself is higher than at power frequency, so the conversion efficiency is lower than 90%.

Table 3 shows the comparison between the NP and T-type three-level inverters.

2.4. SVPWM Control Method. The theoretical basis of the SVPWM is the mean equivalent principle, that is, combining the fundamental voltage vectors in a switching cycle to make the average value equal to the given voltage vector. At a certain moment, the voltage vector rotates into a certain region, which may be achieved by a different combination over time of two adjacent nonzero vectors and zero vectors that make up this region. The action time of the two vectors

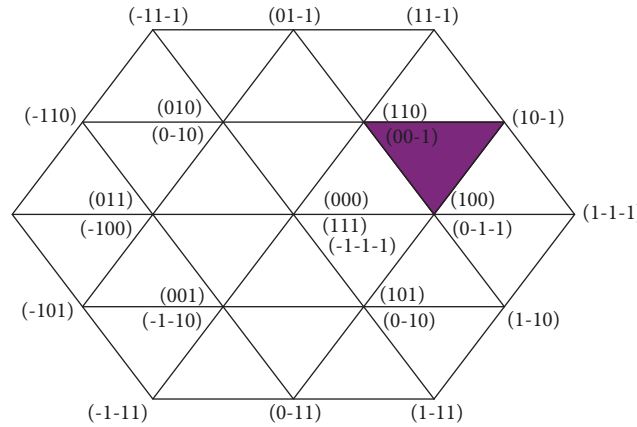


Figure 8: Three-level space vector diagram.

is repeatedly applied in one sampling period, so that it controls the action time of each voltage vector. This rotates the voltage space vector in accordance with the circular trajectory and approaching ideal flux circle through the actual magnetic flux, generated by different switching states of the inverter. Then, it determines the inverter switch state by the comparison, at the end form of the PWM waveform.

SVPWM presents lower total harmonic distortion (THD) compared to other control strategies, and it may refine the steady and dynamic state performances of the PV grid-connected system, simultaneously. Meanwhile, output results of the inverters with SVPWM control strategy provide better power quality than that of the inverters with other control strategies. The SVPWM control strategy with three-phase three-level voltage source inverter is effective and feasible [17]. The detailed equations of the SVPWM strategies based on the proposed topology are as follows.

In this paper we used decomposition hexagon method.

Idea: decompose the multilevel space vector into a combination of multiple two-level space vectors to achieve greatly simplified PWM calculation method.

The three-level space vector diagram is shown in Figure 8. Any reference vector must fall within a small triangle. The vertex of this triangle is the basic voltage vector that composes this reference vector.

The reference vector falling into the shadow in Figure 8 can be decomposed into an offset vector and a two-level vector, as shown in Figure 9.

Steps

2.4.1. Sector Judgments. Based on Clark's transformation, the normalized output vectors transformed from abc to $\alpha\beta$ reference frame may be expressed as

$$\begin{pmatrix} V_\alpha \\ V_\beta \\ V_o \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} V_A \\ V_B \\ V_C \end{pmatrix} \quad (4)$$

Table 1: The loss of each device in hybrid T-type inverter.

Switch type	device	Loss (W)		
		Conduction loss	Switching loss	Total loss
IGBT	S_{a1}	90.45	26.46	116.92
	S_{a2}	31.78	1.03	32.82
Freewheeling diode	d_{a1}	40.59	0.47	41.07
Clamped diode	D_{a1}	2.23	9.93	12.17

Table 2: The power loss and conversion efficiency of two topologies.

component	The number of DC	Loss (W)			conversion efficiency
		IGBT	diode	Total loss	
NPC	1	998.88	310.72	1309.6	0.8690
Hybrid T-type	1	898.44	319.44	1217.88	0.8782

Table 3: Similarities and differences of diode clamped and T-type three-level circuit topologies.

Compared items	Diode clamped three-level inverter	T-type three-level inverter
Switch pressure	Sa1~Sa4: 0.5 UPV	Sa1/Sa2: Upv; Sa3/Sa4: 0.5 Upv
Commutation path	Long commutation path and short commutation path	All paths are consistent
Efficiency	The higher switching frequency (>16 kHZ) increases efficiency	The lower switching frequency (<16 kHZ) increases efficiency
Modulation strategy	Traditional control strategy of current PI loop	Traditional control strategy of current PI loop
Number of components	4 switches plus 2 diodes	4 switches
Drive power	4 groups	3 groups

Table 4: The relations between N and the sector where V_{ref} is located.

N	1	2	3	4	5	6
sector	II	VI	I	IV	III	V

where V_α, V_β, V_o are voltages on the two-phase stationary coordinate system and V_A, V_B, V_C are voltages on the three-phase stationary coordinate system.

We define $N = A+2B+4C$, and the value of N determines in which sector the reference vector V_{ref} is located. So the relations between N and the corresponding sector are shown in Table 4.

2.4.2. Basic Vector Dwell Time Calculation. We assume V_{ref} is located at sector I, which yields the following equation:

$$\begin{aligned} V_\alpha T_s &= T_1 \left|V_1\right| + T_2 \left|V_2\right| \cos\frac{\pi}{3} \\ V_\beta T_s &= T_2 \left|V_2\right| \sin\frac{\pi}{3} \\ T_s &= T_1 + T_2 + T_{0,7} \end{aligned} \tag{5}$$

where T_s is the sampling period; T_1, T_2, and T_0 represent the dwell times of the basic vectors V_1, V_2, and V_0, respectively.

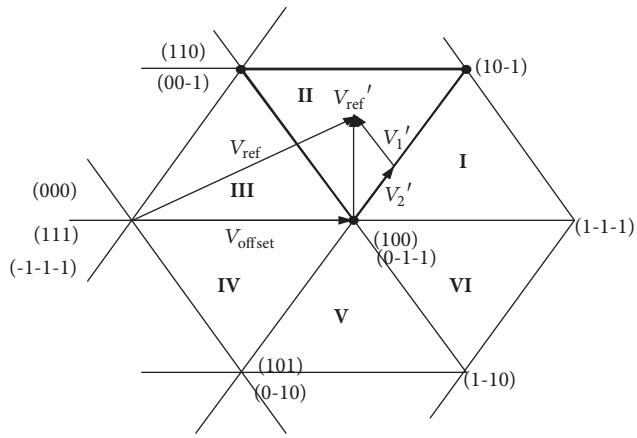


Figure 9: Decomposed two-level space vector diagram.

According to the above expressions, we can obtain the following equation:

$$\begin{aligned} T_1 &= \frac{\sqrt{3}T_S}{2V_{dc}}\left(\sqrt{3}V_\alpha - V_\beta\right) \\ T_2 &= \frac{\sqrt{3}T_s V_\beta}{V_{dc}} \\ T_{0,7} &= T_s - T_1 - T_2 \end{aligned} \tag{6}$$

Table 5: The relations between vector dwelling time and its sector.

sector	I	II	III	IV	V	VI
T_1	Z	Y	-Z	-X	X	-Y
T_2	Y	-X	X	Z	-Y	-Z

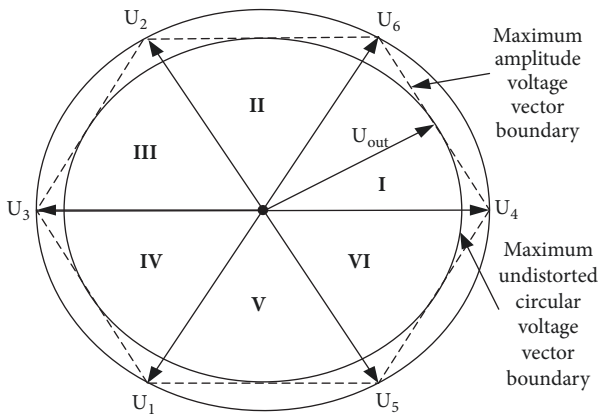


Figure 10: Voltage vector amplitude boundary in SVPWM mode.

Following the same principle, the dwell time of each vector, we achieve V_{ref} of different sectors. To facilitate the solution, we may define it as (7). The value of T_1 and T_2 at different sectors could be set according to Table 5.

$$X = \sqrt{3}\frac{T_S}{V_{dc}}V_\beta$$
$$Y = \frac{T_s}{V_{dc}}\left(\frac{\sqrt{3}}{2}V_\beta + \frac{\sqrt{3}}{2}V_\alpha\right) \quad (7)$$
$$Z = \frac{T_s}{V_{dc}}\left(\frac{\sqrt{3}}{2}V_\beta - \frac{\sqrt{3}}{2}V_\alpha\right)$$

2.4.3. Vector Switching Point Calculation. When the synthesized voltage vector endpoint falls between the regular hexagon and the circumscribed circle, as shown in Figure 10, the overmodulation has occurred and the output voltage will be distorted. So we use a proportional scaling algorithm to control the overmodulation. The vector dwell time that first occurs in each sector is defined as T_{Nx}, and the vector dwell time that occurs after is defined as T_{Ny}. When $T_x + T_y \leqslant T_{\text{NPWM}}$, the vector endpoint is within the regular hexagon and no overmodulation occurs. When $T_{\text{Nx}} + T_{\text{Ny}} > T_{\text{NPWM}}$, the vector endpoint is beyond the regular hexagon and overmodulation occurs. The output waveform will be seriously distorted and must take the following measures.

Suppose that the nonzero vector dwell time is T'_{Nx}, T'_{Ny}, when the endpoint of the voltage vector trace is pulled back to the inscribed circle of the regular hexagon, and then there is a proportional relationship:

$$\frac{T'_{Nx}}{T_{Nx}} = \frac{T'_{Ny}}{T_{Ny}} \quad (8)$$

Therefore, T'_{Nx}, T'_{Ny}, T_{N0}, T_{N7} can be obtained by the following formula:

$$T'_{Nx} = \frac{T_{Nx}}{T_{Nx} + T_{Ny}}T_{N\text{PWM}}$$
$$T'_{Ny} = \frac{T_{Ny}}{T_{Nx} + T_{Ny}}T_{N\text{PWM}} \quad (9)$$
$$T_0 = T_7 = 0$$

According to the above process, the action time of two adjacent voltage space vectors and zero-voltage vectors in each sector can be obtained. The operation relationship is shown in Figure 11 when U_{ref} is in sector I. After the U_{ref} sector and the corresponding effective voltage vector are determined, according to the PWM modulation principle, the value of each corresponding comparator is calculated, and the operation relationship is as follows:

$$t_{\text{aon}} = \frac{\left(T_s - T_x - T_y\right)}{2}$$
$$t_{\text{bon}} = t_{\text{aon}} + T_x \quad (10)$$
$$t_{\text{con}} = t_{\text{bon}} + T_y$$

Other sectors follow the same above principle.

Here, T_{cm1}, T_{cm2}, T_{cm3} denote the transistor's switching time. And the relation between sector switching point and its appropriate sector is tabulated in Table 6.

3. Results and Discussion

This study put forward a novel hybrid T-type inverter topology which is composed of basic units A and B on the basis of previous research studies. We established a three-phase three-level hybrid T-type photovoltaic grid-connected inverter topology model, which is shown in Figure 12, using MATLAB platform. Considering the A-phase bridge leg, for example, it consists of one half-bridge IGBT, one half-bridge MOSFET, and two neutral point MOSFETs. Switches Sa1 and Sa2 work in the mutual intermittent state, and switches Sa3 and Sa4 only work near the current zero-crossing point with high frequency. This topology is rather suited for the photovoltaic nonisolated AC system applications.

The topological structure is on the basis of T-type structure, changing the nine switches into MOSFET, i.e., Sa2, Sb2, Sc2 $\cdots$ Sa4, Sb4, and Sc4. We choose IGBT for Sa1, Sb1, and Sc1; since the reverse recovery ability of the body diode in the field effect transistor is poor, therefore they act in low frequencies. The high frequency MOSFET semiconductor switches, i.e., Sa2, Sb2, Sc2, . . ., Sa4, Sb4, Sc4, provide good switching characteristics and low on-resistance. Moreover, due to the low speed characteristics of the built-in diode of MOSFETs, MOSFET cannot be used in the upper bridge arm. We take advantage of the two devices, to reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system.

Regarding the topology selection, the three-level circuit combines the advantages of the nonisolation and multilevel

Table 6: The relationship between the vector switching point and its corresponding sector.

sector	I	II	III	IV	V	VI
T_a	T_{bon}	T_{aon}	T_{aon}	T_{con}	T_{con}	T_{bon}
T_b	T_{aon}	T_{con}	T_{bon}	T_{bon}	T_{aon}	T_{con}
T_c	T_{con}	T_{bon}	T_{con}	T_{aon}	T_{bon}	T_{aon}

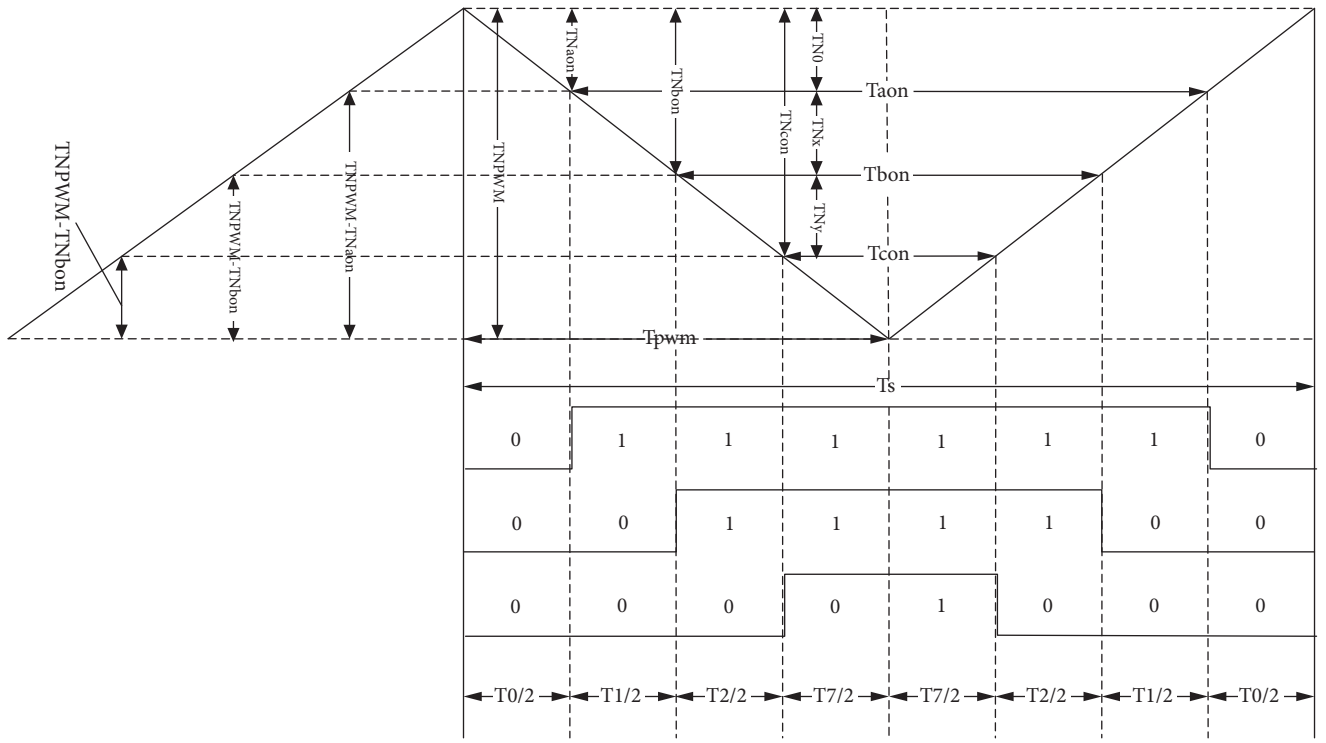


Figure 11: Operation relationship when U_{ref} is in sector I.

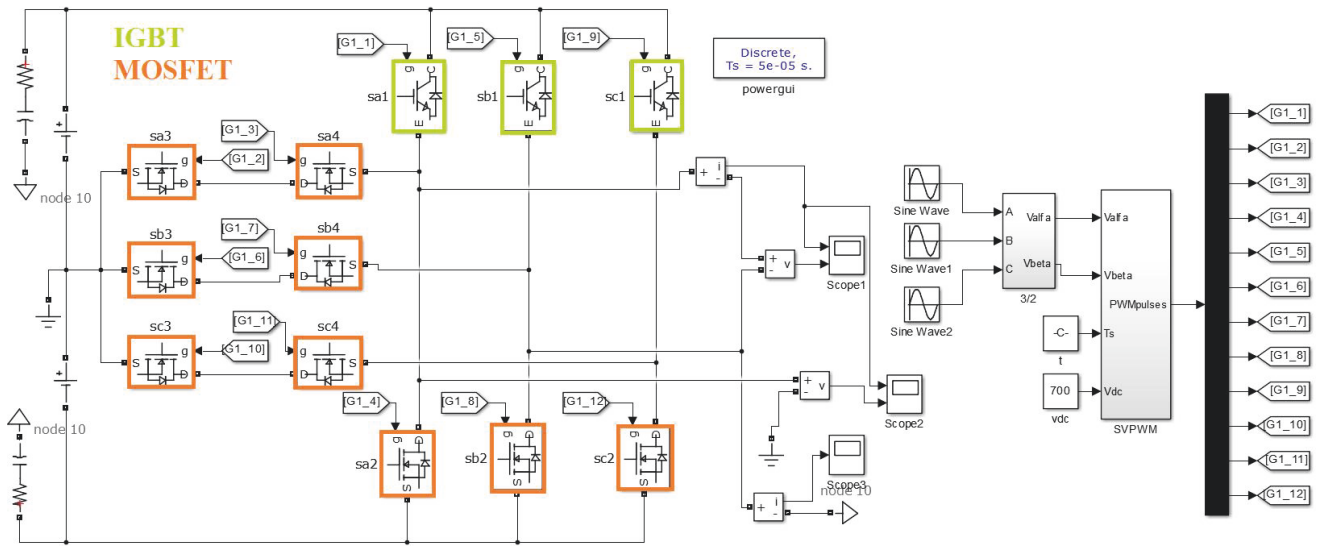


Figure 12: The simulation model of the SVPWM controlled novel T-type three-phase three-level inverter.

Table 7: The classification of the influence of the switching state of the short and medium vectors on the direction of the neutral point current.

Positive short vector switching status	io	Negative short vector switching status	io	Medium vector switching status	io
100	ia	211	- ia	210	ib
221	ic	110	- ic	120	ia
010	ib	121	- ib	021	ic
122	ia	011	- ia	012	ib
001	ic	112	- ic	102	ia
212	ib	101	- ib	201	ic

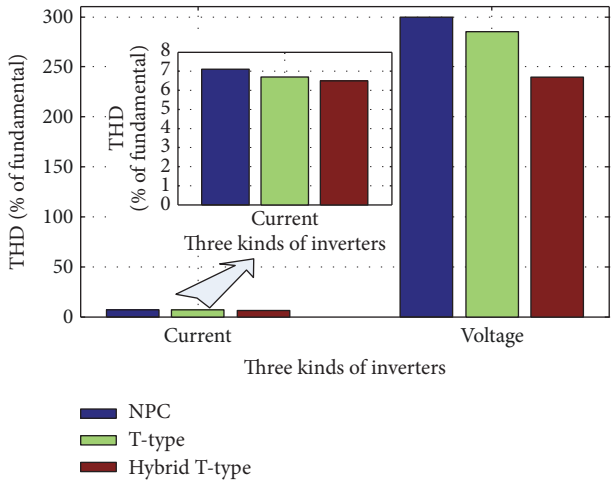


Figure 13: The current and voltage THD comparison of three types of inverters.

technologies, which is very suitable for the photovoltaic grid-connected power generation.

System simulation parameters are as follows: The DC-link voltage is 700 V, with the frequency of 50 Hz, the value of the support capacitor reads 3300 uF, with the AC-side inductance of 3 mH, the AC-side resistance is 0.1 Ω, and the switching frequency is 10 kHz. The value of the stray capacitance is 10e−6 F, and the small resistor is connected in parallel with the stray capacitance of $R = 10e - 6$ ohm.

Table 7 shows the neutral point current when the positive and negative short vector and medium vector act. It can be seen that positive and negative short vector and medium vectors will cause neutral voltage fluctuations.

The neutral point voltage control method is based on the SVPWM. According to the influence of the medium and short vectors on the neutral point voltage offset and by selecting the appropriate switching state and the most suitable switching sequence for the neutral point voltage, the midpoint voltage offset during each control cycle has been minimized.

So selecting the excellent transistor sequence is really important. To solve this problem we run through all the transistors in every possible combination and permutation on the condition of the following switch rules.

(1) The switching states of the devices in every bridge leg are independent. (2) The switching states of any two adjacent switches of each bridge leg are complementary (e.g., if Sa1 is turned on, then Sa2 must be switched off). (3) According to the principle of complementarity, if the switching state of any of the devices in the same bridge leg is determined, the state of the other switching devices of that bridge leg can also be confirmed [18].

The influence of harmonic current on the power grid is greater than the harmonic voltage and it is the fundamental cause of most of the problems, and the neutral voltage fluctuations are proportional to the amount of the harmonic current. So, as can be seen from Table 8, giving comprehensive consideration, choose the following optimal transistor sequence: Sa1-Sa3-Sa4-Sa2-Sb1-Sb3-Sb4-Sb2-Sc1-Sc3-Sc4-Sc2.

The control method is achieved by the SVPWM with 12 trigger pulses. Switching sequence reads Sa1-Sa3-Sa4-Sa2-Sb1-Sb3-Sb4-Sb2-Sc1-Sc3-Sc4-Sc2.

Figure 13 shows the output voltage and current harmonic content of the three types of inverter topology structure, using SVPWM control method. From Figure 13 we could see that current and phase voltage THD (total harmonic distortion) of the NPC inverter is the biggest, the T-type inverter is the middle one, and the proposed hybrid T-type is the smallest one. Meanwhile, the amplitude of the three kinds of inverter current harmonics is not obvious; however, the voltage THD results of the three kinds of inverter are sharply comparable.

The topology and control strategy of the two circuits are the same, except the devices used. The T-type topology consists of 12 IGBTs, while the hybrid T-type topology consists of 9 MOSFETs and 3 IGBTs. And the off-delay time and dead time of the IGBT are longer than those of the MOSFET.

Although the proportion of dead time is often very small relative to one switching cycle, the dead zone will make the three-phase control system deviate from the ideal mathematical model. When the switching frequency becomes higher, the dead-zone effect will gradually accumulate, and when it accumulates to a certain degree, it will distort the AC-side voltage waveform, which will affect the waveform quality of the input current. It will also cause fluctuations in the DC voltage, which degrades the accuracy of the entire system. In addition, the dead time can cause common mode voltage waveform distortion, resulting in higher harmonics [19]. So the THD of the novel T-type inverter is the lowest.

From Figure 14 we see that the common mode current of the proposed novel T-type inverter is smaller than the previous T-type inverter topology. In conclusion the proposed

Table 8: Comparison of output parameters under various switching sequence (simulation time: 0.1 s).

Sequence of the transistors	Power factor	Current harmonics%	voltage harmonics%
Sa1- Sa2- Sb1- Sb2- Sc1- Sc2- Sa3- Sa4- Sb3- Sb4- Sc3- Sc4	0.7209	27.27	158.99
Sa1- Sa2- Sb1- Sb2- Sc1- Sc2- Sa4- Sa3- Sb4- Sb3- Sc4- Sc3	0.7263	21.73	236.75
Sa1- Sc2- Sb1- Sa2- Sc1- Sb2- Sa3- Sa4- Sb3- Sb4- Sc3- Sc4	0.647	11.61	149.13
Sa1- Sc2- Sb1- Sa2- Sc1- Sb2- Sa4- Sa3- Sb4- Sb3- Sc4- Sc3	0.6158	7.81	224.95
Sa1- Sa2- Sa3- Sa4- Sb1- Sb2- Sb3- Sb4- Sc1- Sc2- Sc3- Sc4	0.5799	0.63	156.03
Sa1- Sa2- Sa4- Sa3- Sb1- Sb2- Sb4- Sb3- Sc1- Sc2- Sc4- Sc3	0.447	0.92	230.51
Sa1- Sa3- Sa4- Sa2- Sb1- Sb3- Sb4- Sb2- Sc1- Sc3- Sc4- Sc2	0.7132	6.61	248.44
Sa1- Sa4- Sa3- Sa2- Sb1- Sb4- Sb3- Sb2- Sc1- Sc4- Sc3- Sc2	0.6225	6.91	158.98

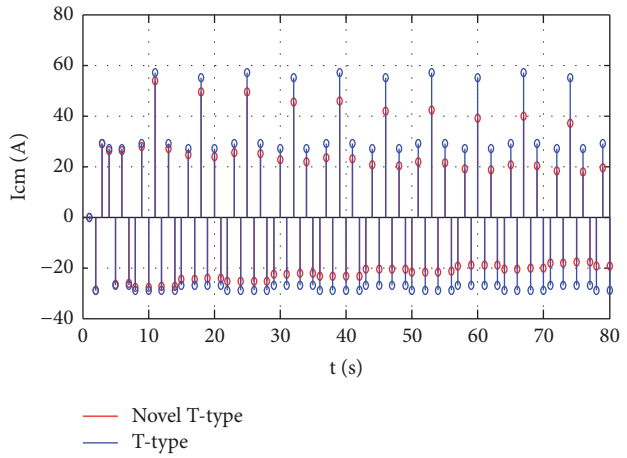


Figure 14: The obtained CM-current of the novel and previous T-type inverters.

hybrid T-type inverter has priority compared to the NPC and T-type inverter.

The instantaneous common mode voltage and ground leakage current could be given by the following equation:

$$u_{cm} = \frac{u_{AN} + u_{BN} + u_{CN}}{3}$$
$$i_{cm} = C\frac{d_{u_{cm}}}{dt} \quad (11)$$

where u_{AN}, u_{BN}, and u_{CN} are the pulse voltages between the branch midpoint and the dc bus minus terminal, respectively

It can be seen from the equation that the common mode current i_{cm} is proportional to the change rate of the common mode voltage u_{cm}.

According to the above interpretation it can be got that the dead time of the proposed topology is the shortest because of the smallest number of IGBTs compared with the other two topologies, so that the common mode voltage and current are also the smallest.

4. Conclusions

We introduced a variety of new multilevel photovoltaic grid-connected inverter topologies, compared them with each other, and classified them according to the basic unit which predecessors proposed. We proposed the hybrid T-type inverter topology, which is composed of two best basic units. This structure makes full advantages of the two devices, which leads to reducing the harmonic content and power loss of the converter and improving the conversion efficiency of the system. By comparing the new topology, the new multilevel inverter topology is formed by the basic constituent elements to increase the auxiliary/embedded circuit or with a hybrid switch or with asymmetric structure to optimize the inverter performance. We use the space vector pulse width modulation (SVPWM) method to build the SIMULINK models of the proposed hybrid T-type and NPC three-level inverter in the MATLAB software and compare them with each other. The simulation results show that the proposed topology presents lower output harmonics than the NPC topology. We then provided further loss analysis for these two topologies, using the MELCOSIM software to calculate the loss of different components in each topology as well as the total power loss. The outcome is that the loss of the T-type topology is significantly lower than that of the NPC topology, and the conversion efficiency is higher than that of the NPC topology. Moreover the simulation results show that the common mode current of the proposed novel T-type inverter is smaller than the previous T-type inverter topology.

The proposed inverter topology has a certain practicality and economy to meet the actual needs.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

All the authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

The work was supported by the National Natural Science Foundation of China (Grants no. 51667020 and no. 61364010), the Outstanding Doctor Graduate Student Innovation Project of Xinjiang University (no. XJUBSCX-2016018), and Graduate Student Innovation Project of Xinjiang Uygur Autonomous Region (no. XJGRI2017025).

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