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Research Article

A High-Input Voltage Two-Phase Series-Capacitor DC-DC Buck Converter

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A high-input voltage 2-phase series-capacitor (2-*pscB*) DC-DC buck converter is theoretically analyzed, designed, and implemented. A new design approach for an automatic current sharing scheme was presented for a 2-phase series-capacitor synchronous buck converter. The series-capacitor voltage is used to achieve current sharing between phases without a current sensing circuit or external control loop as each phase inductor charges and discharges the series capacitor to maintain its average capacitor voltage constant. A novel isolated gate driver circuit to accommodate an energy storage capacitor is proposed to deliver isolated gate voltages to the switching transistors. An I^2 control scheme that uses only one feedback path control for the four gate drivers is proposed to enable higher voltage conversion. An experimental 110-12 V 6 A load prototype converter was designed, and its current sharing characteristics were experimentally verified.

1. Introduction

Two-phase series-capacitor buck converters were introduced to power laptops as low-voltage, high-current voltage regulator modules (VRMs) as well as nonisolated point-of-load (POL) converters [1–3]. Automatic current sharing is important to distribute heat generation in multiphase switching topologies at full load without the need to use current sensing circuit or external control loop between phases. Current sharing implementation for multiphase switching converter topologies is reported in [4–8]. The automatic current sharing concept is the main feature of this double step-down buck topology where the series capacitor was utilized to accomplish current sharing. 2-*pscB* is a unique converter topology that combines the benefits of a switch capacitor circuit as a DC source and a two-phase buck converter [9–11]. Usually, these converters are used as low-voltage (<12 V) POL voltage regulators [12].

In this work, a high-voltage input (110 V) 2-*pscB* converter is theoretically analyzed, designed, and implemented to examine the capability of current sharing at a higher voltage level and its impact on overall efficiency [13]. A new design methodology, without using fudge factors or constants compared to previous designs [14], is used to implement an automatic current sharing scheme. The practical implementation of the 2-*pscB* converter is a challenging task due to the complexity of gate driver galvanic isolation due to timing mismatch between phase A switches. The two conventional bootstrap structures as shown in paper [1] are unsuitable for higher input voltages, and bootstrap diode isolation is not adequate to provide stability to gate driver reference voltage because voltage swing is common due to charging and discharging of the series capacitor between the phase A gate drivers. A new isolated gate driver circuit to accommodate an energy storage capacitor is proposed to deliver isolated gate voltages to the switching transistors. An I^2 control scheme that enables higher voltage conversion is proposed that uses only one feedback path control to drive the 4 gate drivers. An experimental 110-12 V at 6 A load prototype converter was designed, and its current sharing characteristics were experimentally verified to show that a higher input voltage is possible compared to low input voltage [14, 15] using an integrated circuit controller driving internal FETs of TPS54A20. Figure 1(a) shows the two-phase

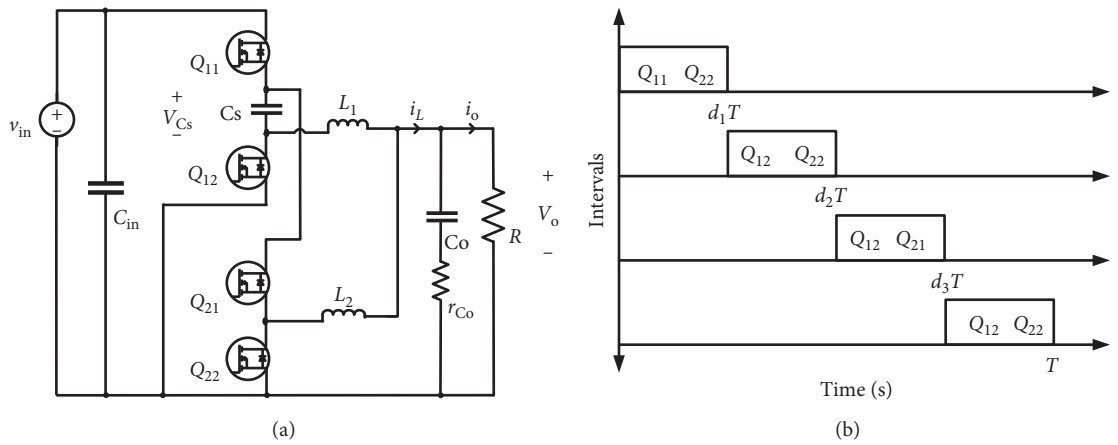


Figure 1: (a) Circuit schematic of the 2-*pscB* converter and (b) switching intervals.

series-capacitor buck converter with automatic current sharing.

The outline of the paper is as follows. Section 2 describes the fundamentals of this topology. Section 3 derives the main parameters for the 2-*pscB* converter. Section 4 describes the isolated gate driver circuit design. Section 5 presents the proposed control scheme. Section 6 presents the simulation results using *LTspice*. Section 7 shows the experimental prototype and characterization results to illustrate the functionality and performance of the 2-*pscB* converter. Sections 8 and 9 provide discussion and the summary.

2. Analysis of the 2-pscB Converter

A 2-*pscB* converter has four switching intervals: the first switching interval D_1T with Q_{11} and Q_{22} switching on, the second and fourth switching intervals D_2T and $(1-d_3)T$ with Q_{12} and Q_{22} switching on, and the third switching interval D_3T with Q_{12} and Q_{21} switching on. Figure 1(b) shows the four switching intervals and the switching devices that are switched on during these intervals. Hence,

$$\begin{aligned}(d_2 - d_1)T &= D_2T,\\ (d_3 - d_2)T &= D_3T,\\ (1 - d_3)T &= (1 - D_1 - D_2 - D_3)T,\end{aligned} \tag{1}$$

where T is the switching period. At steady state, during the first switching interval, the high-side switch of phase A, switch Q_{11}, is switched on, and the inductor current flowing through inductor L_1 charges the series capacitor Cs [3, 9]. The duty cycle is given as

$$\frac{V_o}{V_{in}} = \frac{d_1(d_3 - d_2)}{d_1 + d_3 - d_2} = \frac{D_1D_3}{D_1 + D_3}, \tag{2}$$

where d_1, d_2, and d_3 represent switching intervals for the series-capacitor buck modes. When these intervals are the same, $D_1 = D_2 = D_3 = D$. Hence,

$$\frac{V_o}{V_{in}} = \frac{D}{2}. \tag{3}$$

To achieve the current sharing balance between the two phases, the switching voltage nodes must be the same. Hence,

$$\frac{V_{cs}}{V_{in}} = \frac{d_1}{d_1 + d_3 - d_2} = \frac{D_1}{D_1 + D_3}. \tag{4}$$

From equations (2) and (4) at steady-state conditions,

$$\frac{V_o}{V_{cs}} = D_3. \tag{5}$$

3. Derivation of Design Parameters

A new design approach for an automatic current sharing scheme is presented for the 2-*pscB* converter. The series-capacitor voltage is used to achieve current sharing between phases without a current sensing circuit or external control loop as each phase inductor charges and discharges the series capacitor to maintain its average capacitor voltage constant. Design parameters are derived and experimentally validated.

The main switches of both phases are driven at 180° phase shifts and with a duty ratio of less than 50%. The inductor currents are defined as

$$I_{L1_{max,min}} = I_{R_1} \pm \frac{1}{2}\left[\frac{V_o}{L_1}(1 - D_1)T\right] = I_{R_1} \pm \frac{\Delta i_{L_1}}{2}, \tag{6}$$

$$I_{L2_{max,min}} = I_{R_2} \pm \frac{1}{2}\left[\frac{V_o}{L_2}(1 - D_3)T\right] = I_{R_2} \pm \frac{\Delta i_{L_2}}{2}, \tag{7}$$

where $I_{L1_{max,min}}$ and $I_{L2_{max,min}}$ are the maximum and minimum values of phase A and B inductor currents. I_{R1} and I_{R2} are the average load currents at phase A and B, respectively. In this 2-*pscB* converter, the total average output inductor current is the sum of both the average phase inductor currents. For a complete current sharing, the peak-to-peak ripple current of a single phase is

$$\Delta i_{L_1} = \Delta i_{L_2} = \left[\frac{1}{L}\left(\frac{V_{in}}{2} - V_o\right)T_{on}\right], \tag{8}$$

where $T_{\text{on}} = D_1 T = D_3 T$. As such, a larger L and smaller T_{on} will yield a smaller ripple current. The total average output current in terms of i_L will be

$$I_{\text{out}} = \frac{I_{L\max} + I_{L\min}}{2} = I_{R_1} + I_{R_2}. \tag{9}$$

The total inductor current at zero condition is equal to the minimum value $I_{L\min}$, when Q_{11} is off in modes II and IV:

$$I_{L_{\min}} = i_L(0) = I_{L1_{\min}} + \frac{2}{3} I_{L2_{\max}} = \frac{5}{6} I_{\text{out}} + \frac{1}{2} \frac{V_o T}{L} \left[\frac{2}{3}(1 - D_3) - (1 - D_1) \right]. \tag{10}$$

When the load current contributed by each phase is at complete current sharing condition, $I_{R_1} = I_{R_2} = (1/2) I_{\text{out}}$, the maximum inductor current value will be at full charging of series capacitor in phase A and at fully discharging in phase B.

$$\begin{aligned} I_{L_{\max}} &= i_L(d_1 T) = I_{L1_{\max}} + \frac{1}{3} I_{L2_{\max}} \\ &= I_{R_1} + \frac{1}{3} I_{R_2} + \frac{1}{2} \frac{V_o T}{L} \left[\frac{1}{3}(1 - D_3) + (1 - D_1) \right] \\ &= \frac{2}{3} I_{\text{out}} + \frac{2}{3} \left[\frac{V_o}{L} (1 - D) T \right]. \end{aligned} \tag{11}$$

Thus, the peak-to-peak inductor current ripple is

$$\begin{aligned} \Delta i_L &= I_{L1_{\max}} - I_{L1_{\min}} - \frac{1}{3} I_{L2_{\max}} \\ &= \frac{V_{\text{o}}}{6} \left(\frac{1}{L f_{\text{sw}}} (5 - 6 D_1 + D_3) - \frac{1}{R} \right) \\ &= \frac{5}{6} \left[\frac{V_{\text{o}}}{L} (1 - D) T \right] - \frac{1}{6} I_{\text{out}} \\ &= \frac{1}{6} \left[5 \Delta i_{L_{\text{phase}}} - I_{\text{out}} \right], \end{aligned} \tag{12}$$

where $\Delta i_{L_{\text{phase}}}$ is phase A or B average current ripple at full current sharing. At continuous current mode (CCM) operation, $I_{L_{\min}}$ is a positive value. During current sharing, when $L_1 = L_2$, $I_{L_{\min}} > 0$, we have

$$\frac{5}{3} I_{R_1} - \frac{V_{\text{o}} T}{L} \left(\frac{(1 - d_1)}{2} - \frac{(d_2 + 1 - d_3)}{3} \right) > 0. \tag{13}$$

The critical value for the two-phase inductors is then

$$L_{\text{critical}} > \frac{R}{5 f_{\text{sw}}} (1 - 3D_1 + 2D_3). \tag{14}$$

The phase inductance should be within 1.5 to 2 times the critical inductance given in equation (14) to yield a good efficiency. Note that the efficiency of the converter increases with increasing inductance with performance degradation in its transient response. To avoid this effect, the inductance value should be chosen to provide reasonable efficiency and good transient response. As such, the output inductor value can be expressed in terms of its current ripple as

$$L > \frac{5 R V_{\text{o}} (1 - D)}{f_{\text{sw}} [6 R \Delta i_L + V_{\text{o}}]}. \tag{15}$$

The instantaneous capacitor charge stored in one half of the switching period can be used to determine its output capacitance value as shown in Figure 2.

$$\Delta Q = \frac{1}{2} \left(\frac{T}{4} \right) \frac{\Delta i_L}{2} = C_{\text{o}} \Delta V_{\text{o}}, \tag{16a}$$

$$\text{or } \frac{\Delta V_{\text{o}}}{V_{\text{o}}} = \frac{T}{96 C_{\text{o}}} \left(\frac{T}{L} (5 - 6 D_1 + D_3) - \frac{1}{R} \right). \tag{16b}$$

Hence, during a complete current sharing,

$$C_{\text{o}} > \frac{1}{96 f_{\text{sw}} (\Delta V_{\text{o}} / V_{\text{o}})_{\max}} \left(\frac{5}{L f_{\text{sw}}} (1 - D) - \frac{1}{R} \right). \tag{17}$$

Using the maximum and minimum output capacitor current expressions:

$$\Delta i_{C_{\text{o}}} = \frac{1}{R + r_{C_{\text{o}}}} (R \Delta i_L - \Delta v_{\text{o}}). \tag{18}$$

For smaller output capacitor parasitic resistance $r_{C_{\text{o}}}$ and smaller Δv_{o}, $\Delta i_{C_{\text{o}}} \cong \Delta i_L$.

Series-capacitor voltage, V_{Cs}, acts as an internal feedback loop quantity to adjust the current sharing for the two phases. As such, if the inductor currents are not equal, the series-capacitor voltage would drift up or down and a smooth charging balance could not be maintained [16, 17]. This is because the average capacitor voltage remains constant only when the charge and discharging period balance exists. Inductor currents i_{L1} and i_{L2} charge and discharge the series capacitor Cs, respectively. Figure 3 shows a simplified mathematical representation of 2-*pscB* converter with its internal current sharing mechanism resulting from the series-capacitor voltage V_{Cs} including parasitic components. In steady-state conditions during automatic current sharing, the two inductor currents should be equal, and then the average series capacitor voltage will be constant as well with approximately half the input voltage across it, and the series capacitor acts as a dc voltage source for the third interval. Hence,

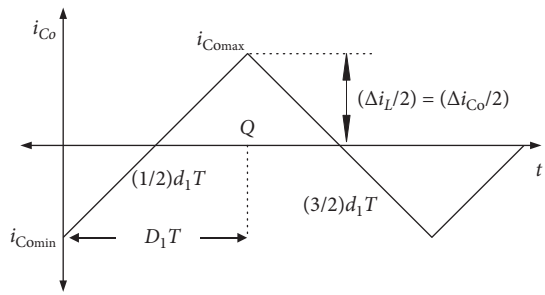


Figure 2: Instantaneous output capacitor circuit.

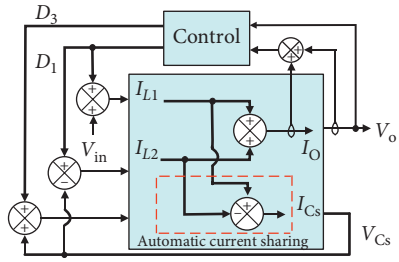


Figure 3: Self-balancing technique for 2-*pscB* converter.

$$\begin{aligned} d_1\left(V_{in} - V_{cs}\right) - V_{cs}\, D_3 &= 0, \\ \text{Mode I: } \langle i_{Cs}\rangle &= \langle i_{L_1}\rangle, \\ \text{Mode II, IV: } \langle i_{Cs}\rangle &= 0, \\ \text{Mode III: } \langle i_{Cs}\rangle &= -\langle i_{L_2}\rangle, \text{where} \\ \langle i_{Cs}\rangle &= \langle i_{L_1}\rangle D_1 - \langle i_{L_2}\rangle D_3 = 0. \end{aligned} \tag{19}$$

Using the i_{Cs} waveform shown in Figure 4, if $I_{\min D1}$ can be neglected, the minimum Cs value can be generalized and expressed at complete current sharing as

$$\Delta Q = D_1 T\, I_{\min D1} + \frac{1}{2}\, D_1 T \frac{\Delta i_{L_1}}{2} = \mathrm{Cs}\, \Delta V_{Cs}, \tag{20}$$

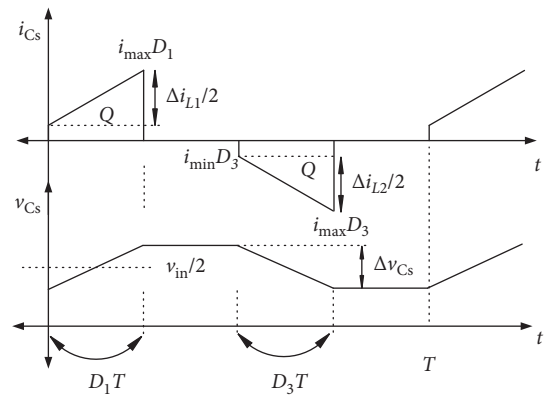


Figure 4: Series-capacitor current and voltage at steady state.

$$\mathrm{Cs} = \frac{D_1 V_o\left(1 - D_1\right)}{4 f_{sw}^2 L_1\, \Delta V_{Cs}} + \frac{D_1 T\, I_{\min D1}}{\Delta V_{Cs}}, \tag{21}$$

$$\mathrm{Cs} > \frac{D^2\left(1 - D\right)}{4\, L\, f_{sw}^2 \left(\Delta V_{Cs}/V_{Cs}\right)_{\max}}. \tag{22}$$

The above equations enable design parameters such as Cs, Co, and Δi_L to be determined.

One of the technical advantages of multiphase is that the combined output ripple (total ripple) is less than the ripple current in each inductor (phase ripple). This occurs due to driving the phases out of phase. In case of the 2-*pscB* converter at interleaving, the phases with a proper timing circuitry, ripple current reductions can be easily achieved even under unbalanced current sharing since the series-capacitor voltage can compensate for the current difference for certain limits that results in much less output voltage ripple. Assuming all the ripple voltage is caused by the capacitance of the output capacitor, the approximated peak to the peak value of the total output current ripple to be filtered by the output capacitor is

$$\Delta i_{L,2pscB} = \frac{v_o\left(1 - 2D\right)}{L f_{sw}} \left\{ \frac{N\left(D - (m/N)\right)\left(\left((2m+1)/N\right) - 2D\right)}{D\left((1/2) - D\right)} + \frac{N\left(D - (m/N)\right)\left(\left((2m+1)/N\right) - 2D\right)}{D\left((1/2) - D\right)} \right\}, \tag{23}$$

$$K_{RCM} = 2\left(1 - \frac{m}{N * D}\right)(2m + 1 - N * 2D), \tag{24}$$

where K_{RCM} is output current ripple cancellation multiplier, N is the number of the phases, and floor function returns the greatest integer value less than the argument.

$$m = \mathrm{floor}\left(N * D\right), \tag{25}$$

where $(m+1)/N \geq D \geq m/N$, $N \geq m \geq 0$.

Figure 5 shows that at certain duty cycle (D) value, there is a total cancellation of the ripple current according to the above constraints. For example, total ripple current cancellation for a 2-phase converter occurs beyond a duty cycle of 0.25, whereas for a 4-phase converter, this total ripple current cancellation occurs at duty cycle beyond 0.125 and between a duty cycle of 0.25 and 0.375 as shown in Figure 5.

4. A Novel Isolated Gate Driver

Figure 6 shows the gate driver circuit using a *UCC27531* gate driver to accommodate adding a series capacitor between switches Q_{11} and Q_{12} of the phase A [18], where

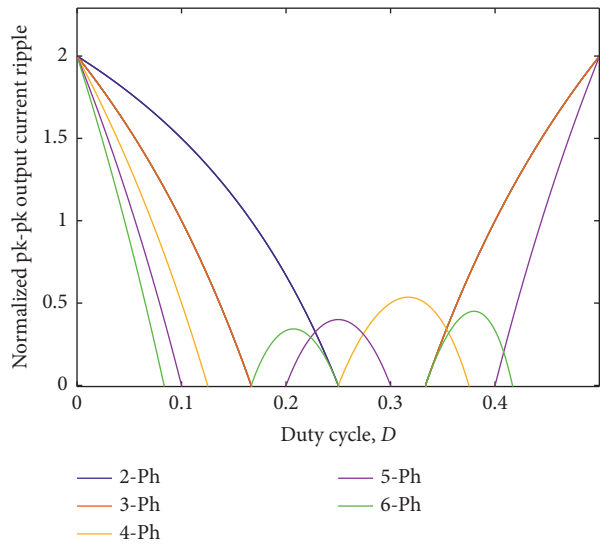


Figure 5: Normalized output inductor ripple versus duty cycle.

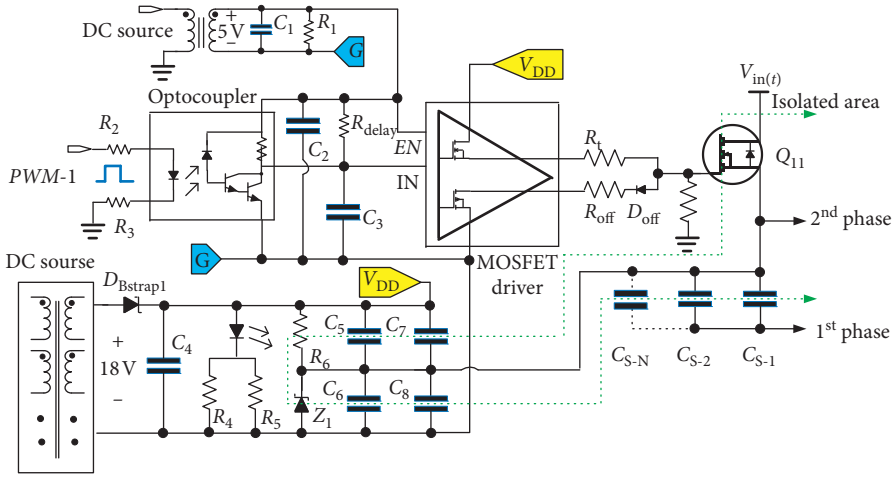


Figure 6: Circuit schematic of gate driver circuit for Q_{11}.

the gate reference voltage for the isolated high-side switch is the positive side of Cs, whereas the gate voltage for the low-side switch circuit requires a different isolation loop since its reference voltage is ground. As such, an isolation scheme must encompass the entire high-side switch circuit because inserting a series capacitor will introduce a time delay between the gate voltages of the two switches.

This will interfere with the synchronization of the switching time and voltage level. Isolation scheme is required to isolate the ground loops; this means there should be no direct conduction path between the high-side driver and the synchronous rectifier switch driver due to the voltage storage element of Cs. The anode of bootstrap diodes, D_{Bstrap1}, is commonly connected to a driver source V_{DD}. Therefore, bootstrap capacitors C_5 to C_8 are charged by a voltage difference between the driver source voltage V_{DD} and the series-capacitor voltage V_{Cs} during the on-times of the Q_{12} switch through the bootstrap diode D_{Bstrap1}. Since the four bootstraps diodes are isolated using an isolated DC source, the gate voltages of the main switches Q_{11} and Q_{21} are enough to charge the bootstrap capacitors. As such, phase B uses the same gate drivers as phase A. To reduce the cost of the four matched bootstrap capacitors for each gate driver, C_5 to C_8, two of them can be eliminated. For voltage higher than 12 V, external FETs are used for better heat distribution and isolation [15]. The gate driver should be located as close to the MOSFETs as possible. In this way, self-inductance and self-resistance of the traces will be reduced to minimize voltage spikes and reduce EMI. For a complete current sharing, dead time must be the same for both phases. In the proposed circuit, there are two ways to adjust the dead time between the high-side signal and low-side signal using two variable resistors before and after the optocoupler. Current sink loops for the high-side switches are not similar in each phase as illustrated in Figure 7. dV/dt occurs on the MOSFET drain when the MOSFET is already held in its off state by the gate driver. The current created by this dV/dt

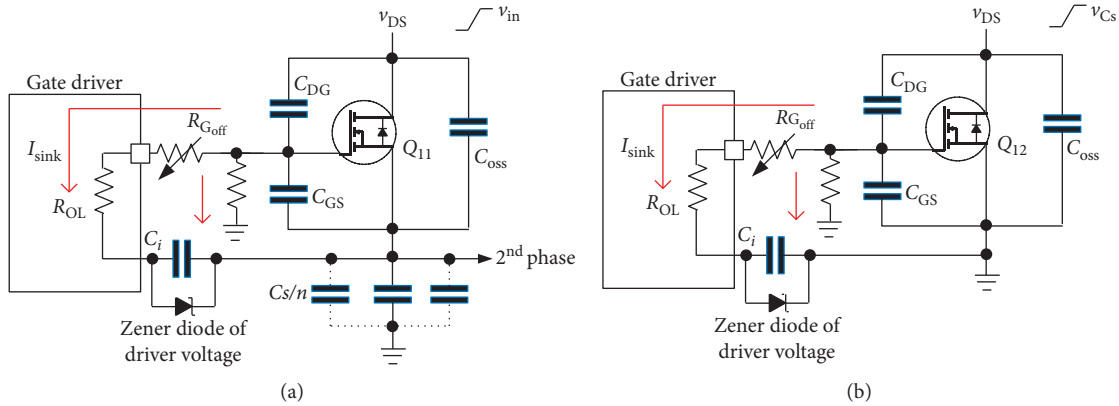


Figure 7: Phase A current sink loops: (a) top switch and (b) bottom switch.

charges the C_{gd} Miller capacitance and is shunted by the pull-down stage of the driver.

If the pull-down impedance is not sufficiently low, then a voltage spike can appear in the V_{gs} of the MOSFET. The upper limit for the voltage at the EN node is 5 V. This complete gate circuit contains 4 bootstrap diodes at the output terminals of the power supply fly-back transformer.

5. An I^2 Control Scheme for 2-*pscB* Converter

The objective of the feedback compensation loop is to enable its closed-loop converter to possess adequate line and load regulations with a low output voltage overshoot. Multiphase current sharing two loops control was proposed in [19, 20]. Converter control to output transfer function at full current sharing is

$$G_{vD}(s) = \frac{R}{2R + r_L} \frac{v_{in}\left(\left(s/\omega_{\varnothing}\right) + 1\right)}{\left(s^2/\omega_o^2\right) + \left(s/Q_o\omega_o\right) + 1}, \tag{26}$$

where

$$\omega_{\varnothing} = \frac{R}{C_o r_{Co}}, \qquad \omega_o = \sqrt{\frac{2R + r_L}{LC_o\left(R + r_{Co}\right)}}, \tag{27}$$

$$Q_o = \frac{\sqrt{LC_o\left(2R + r_L\right)\left(R + r_{Co}\right)}}{\left(L + RC_o r_L + C_o r_{Co} r_L + 2RC_o r_{Co}\right)}. \tag{28}$$

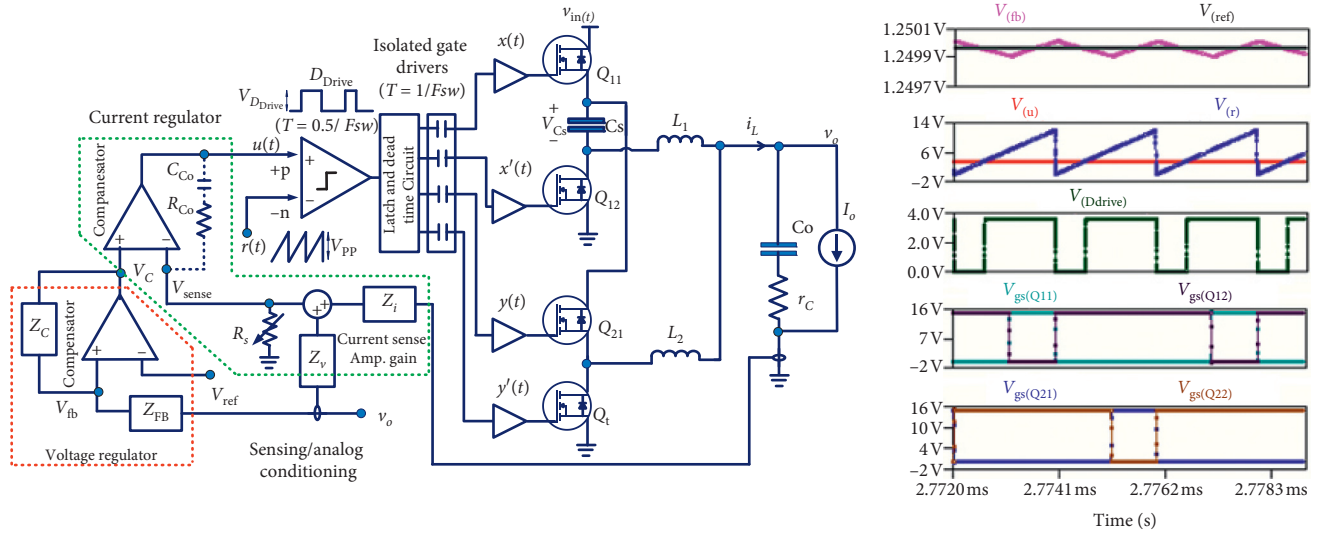
To obtain a well-regulated average output voltage signal, switching frequency must be greater than ten times the resonant frequency for small output voltage ripple ($f_{sw} \approx 20 f_o$ recommended). The natural output impedance (Z_{out}) of output filter peaks at the converter resonant frequency ($f_o = 12$ kHz). Therefore, the unity-gain crossover frequency (f_c) must be higher than the resonance frequency to yield a sufficient gain margin to suppress its ringing effect, maintain constant series-capacitor voltage, and obtain a sufficient phase margin. If the equivalent series resistance (ESR) of the capacitor that dominates its impedance at higher frequencies is neglected, then the peak resonance occurs at

$$\left|Z_{out-Max}\right| = R\sqrt{\frac{2Z_o^2 + r_L^2}{\left(2/Z_o^2\right)\left(Z_o^2 + Rr_L\right)^2 + r_L^2}}, \tag{29}$$

where $Z_o = \sqrt{L/C_o}$ is the characteristic impedance of the filter.

For a converter that has a long series capacitance charging period, an enhanced I^2 current control scheme is used to compare the sum of the output current (with a current sensing gain Z_i) and analog current of its output voltage feedback line (with a current sensing gain Z_v) to the output voltage of the compensated error amplifier. The enhanced I^2 control can achieve a fast load transient response at a constant frequency. The equivalence series resistance (ESR) of the output capacitors or i_L is used as the current sensing resistor as shown in Figure 8(a) where the inner loop uses the inverting input signal voltage V_{sense} across the sensing resistor R_s generated by both output current i_o and feedback as a proportional feedback control variable and the outer loop uses the control signal V_C generated by compensating the errors between the output voltage v_o and the reference voltage V_{ref} in the error amplifier. The sensing voltage V_{sense} in the inner loop contains the information of both the feedback output voltage and inductor current when V_{sense} reaches the value of V_C. The comparator changes the state at its output $u(t)$ which compares with the oscillator ramp signal $r(t)$ at twice the switching frequency. This allows the logic latch circuit to generate two pulses at half the oscillator frequency. The logic latch and delay time circuit consist of logic gates and galvanic isolation of (10–50) MBd to produce four signals with a maximum 50% duty cycle that can be controlled by only D_{Drive} signal variations. An RC inverting negative feedback circuit can be added to the current regulator (comparator) to accurately control the overall current regulator gain. The error amplifier uses a PID compensator with a V_{ref} of 1.25 V.

A single feedback control loop with one modulator for the two phases gives several advantages over conventional schemes [7, 13, 19] such as immunity against sensing inaccuracies which potentially reduces the complexity and



(a) (b)

Figure 8: Enhanced I^2 control scheme: (a) circuit and (b) waveforms of the control parameters.

the number of components and size of the controller and minimizes the time propagation delay and voltage drop to enable the generation of two duty cycle pulses D_1 and D_3 within one ramp signal period. As such, no offline or online calibration is needed to achieve optimum efficiency. Figure 8(b) shows the waveforms within the compensator loop where $x'(t) \triangleq 1 - x(t)$, $y'(t) \triangleq 1 - y(t)$.

As shown in Figure 9, the ramp signal frequency is twice the converter switching frequency to generate two-phase pulses. During a step response, the controller decreases the current passing through the load to minimize the current surge as seen in Figure 10(a). As can be seen, a low overshoot voltage is due to fast-direct feedback loop action where series-capacitor charging starts instantaneously at zero time; at the same time, its soft start feature allows the output voltage to ramp up in a controlled manner minimizing output voltage overshoot during startup as shown in Figure 10(b). The step response has only a small effect on maintaining automatic current sharing balance as shown in Figure 10(c), where i_{L1} is decreased by switching off Q_{11} to achieve a predetermined overshoot voltage magnitude as well as to enable the soft start feature. As such, it eliminates the need to monitor and precharge the series-capacitor voltage. The simulated Matlab waveforms shown in Figure 10 verify the analytical and design methods.

6. Simulation Work

Using derived equations (12) to (22), the converter parameters for the desired load and output ripples are determined. The specifications for the 110/12 V dc 2-*pscB* converter are listed in Table 1. A two-phase series-capacitor buck converter is simulated using *LTspice*. The simulation efficiency reaches 98.7% for a perfect dead time implementation in the steady-state operation.

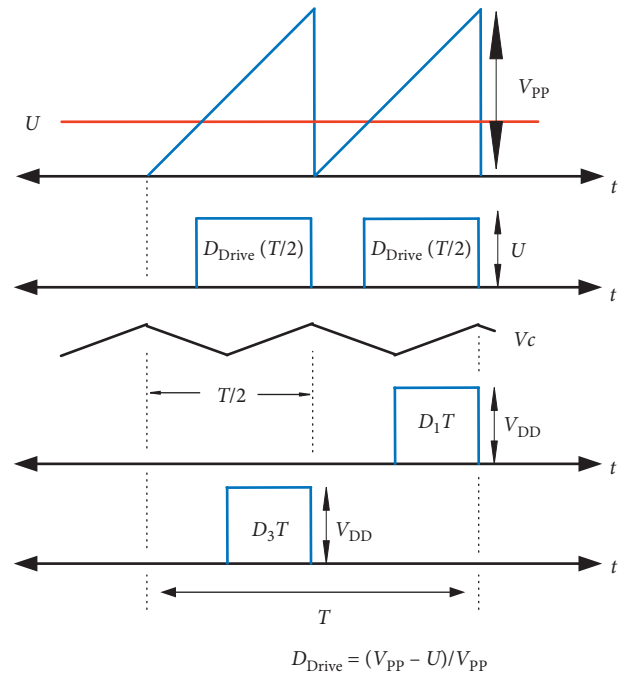


Figure 9: Generation of the control pulses, D_{Drive}.

Figure 11(a) shows the waveforms for V_{ds} and I_{ds} of Q_{11} during the D_1T interval. As can be seen, both V_{ds} and V_{Cs} are 55 V. Its drain current, which is also the phase A inductor current, increases linearly to charge the series capacitor to its maximum voltage. Figure 11(b) shows the switching losses of Q_{11}. Current spikes occur during the switching transitions of both Q_{11} and Q_{22}. The total switching losses are 40 W during a 4 ns switching period. Figure 11(c) shows I_g where the gate currents are less than 1.5 A and 2.5 A during the rising and falling edges of the gate pulses.

Figure 12 shows the series-capacitor voltage, current, and two-phase inductor current waveforms during steady-

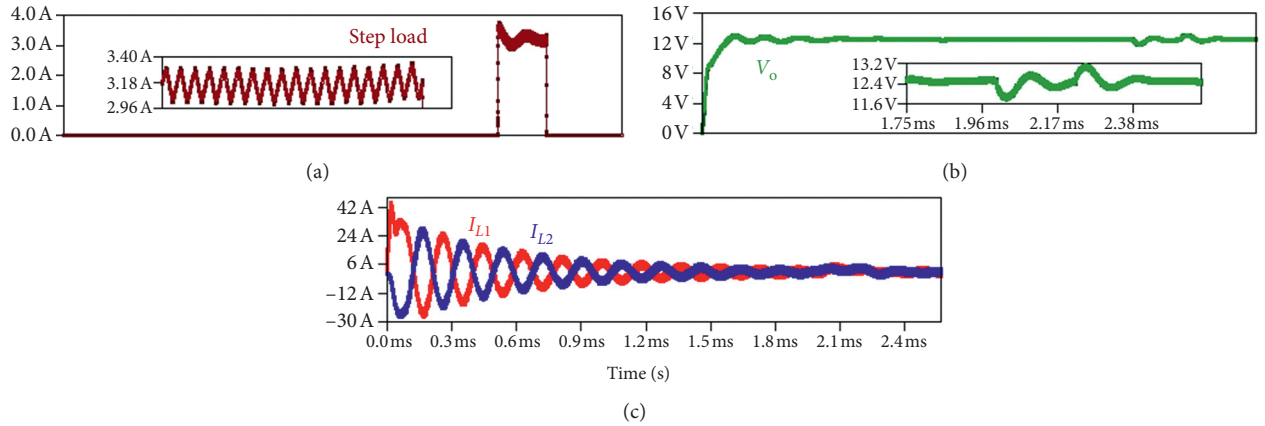


Figure 10: Simulated transient response with (a) step load, (b) output voltage, and (c) inductor currents of the converter.

Table 1: 2-*pscB* converter experimental evaluation parameters.

Component	Abbreviation	Value
Series capacitor	Cs	9 μF
Phase inductors	L_1 and L_2	10 μH
Output capacitor	Co	>80 μF
Switching frequency	F_{sw}	250 kHz
Input voltage	V_{in}	110 V
Output voltage	V_o	12.5–13.5 V
Stray components	r_{Cs}	20 mΩ
Stray components	r_{on}, r_{L1}, r_{L2}	<20 mΩ
Output power	*Po*	<75 W

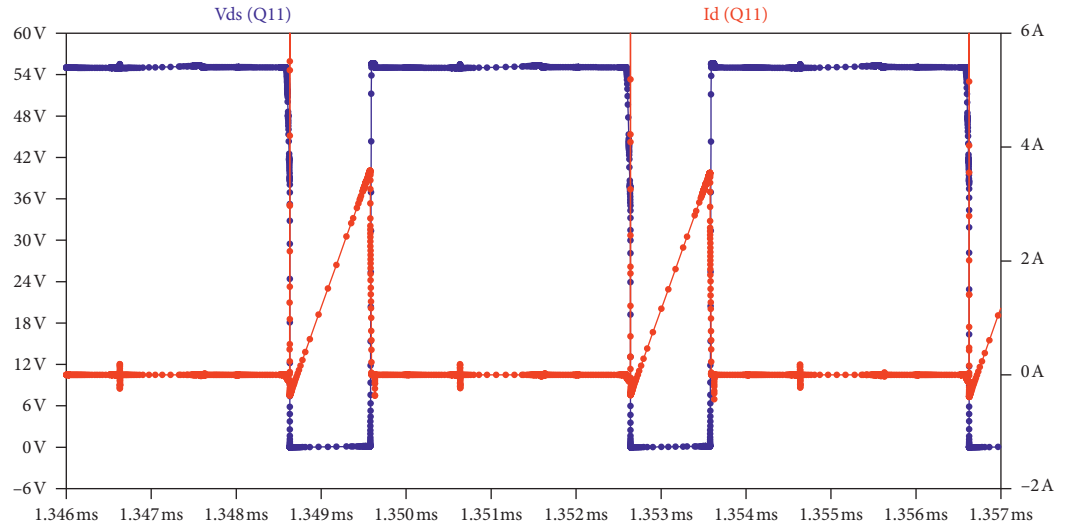


Figure 11: Continued.

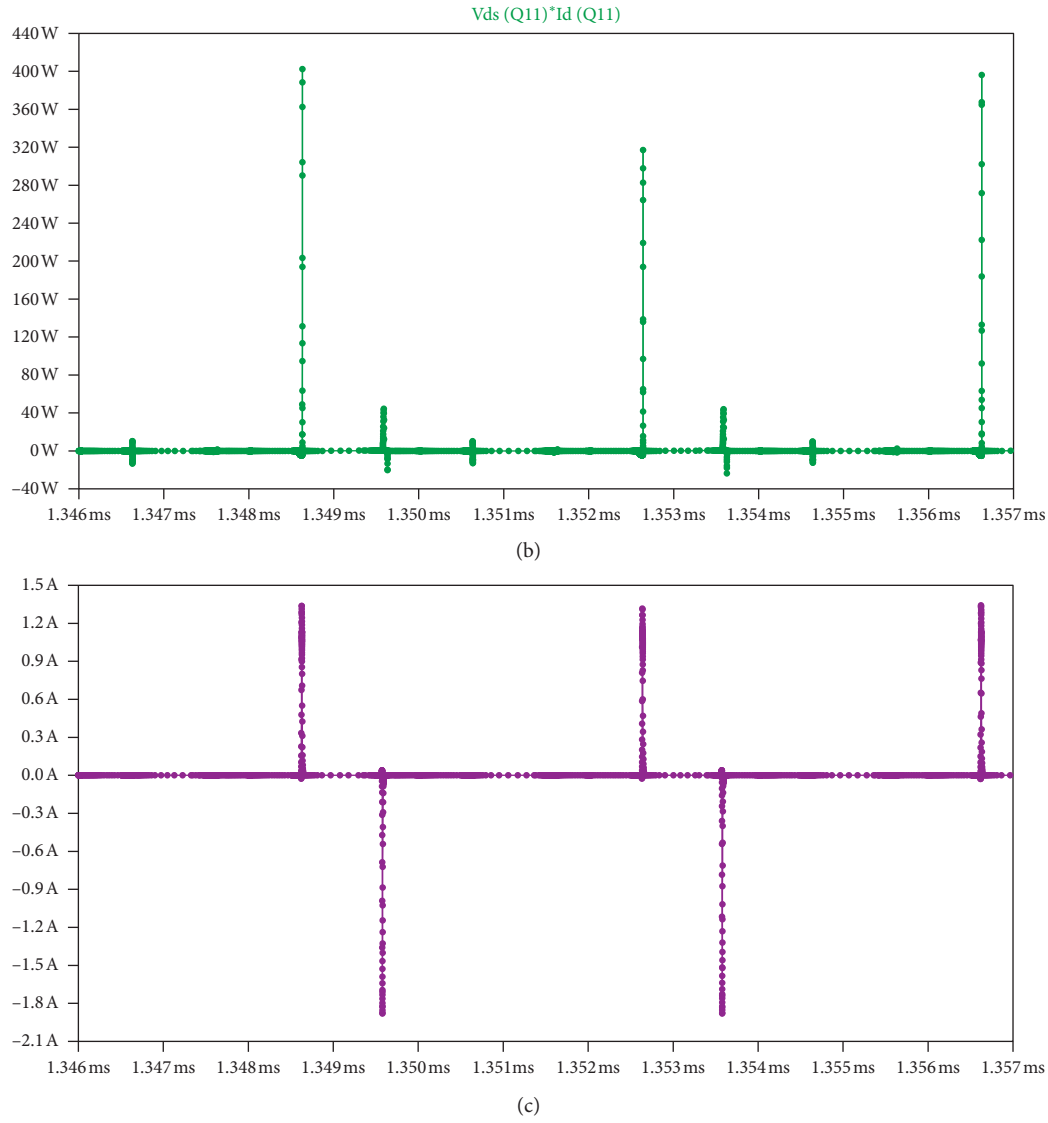


Figure 11: Waveforms of (a) V_{ds} and I_d of Q_{11}, (b) switching losses of Q_{11}, and (c) gate current (source and sink) I_g of Q_{11}.

state operation. As can be seen from Figure 12(a), the average V_{Cs} maintains its value at exactly half of the input voltage with a voltage ripple of less than 0.5 V. The output voltage ripple can be controlled by the size of the output filter. The average charging and discharging currents for the series capacitor are similar as shown in Figure 12(b); this verifies the steady-state operation of the 2-*pscB* converter. Figure 12(c) shows the inductor currents i_{L1} and i_{L2}; the two inductor currents have identical magnitudes, and they are 180° out of phase at steady-state operation.

7. Experimental Results

The component selections for the 2-*pscB* converter are first justified. For a 2.54 cm long and 40-mil wide printed circuit board (PCB) copper trace, the parasitic inductance is about 8 nH. The parasitic inductance of a 0.4 mm diameter via a 1.6 mm thick PCB is 1.2 nH [21, 22]. The self-resistance calculations of all traces are performed using the *Autodesk Eagle software*. The parasitic resistance, r_{Cs}, can be reduced to half the value by using two parallel aluminum electrolytic capacitors of 4.5 μF with a dissipation factor of 0.3 for the two series capacitors Cs_1 and Cs_2. The total ESR of the two parallel capacitors is

$$\text{ESR} = \frac{\tan\delta}{2\omega Cs} = 0.02\Omega \quad \text{at } 250\,\text{kHz}. \tag{30}$$

Two ERU (16) helically wound choke inductors with a DC resistance of 3.7 mΩ and a current saturation of 18.3 A are used for the phase inductors. A total of four IPB530N15N3 power MOSFETs are required to implement the 2-*pscB*, and an additional power MOSFET (Si7898) is used for the fly-back converter to provide or serve as a component power supply as shown in Table 2 [23].

This fly-back converter is used to supply four isolated 18V to drive the gate of four MOSFETs at a frequency of 323 kHz. A Tektronix P5200 Differential Probe 50X/500X attenuation was used to measure voltages as shown in

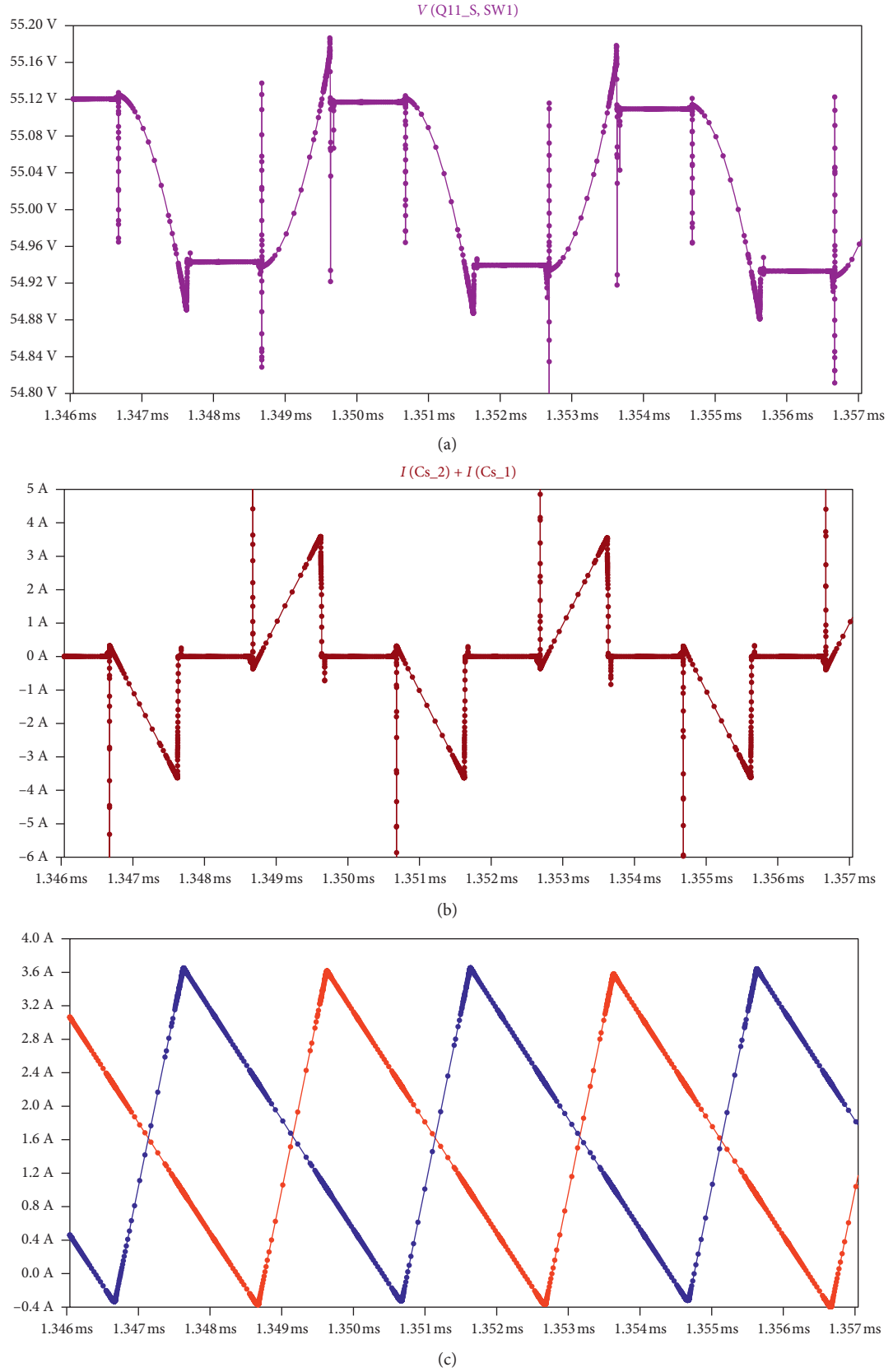


Figure 12: Waveforms of (a) series-capacitor voltage, V_{Cs}, (b) series-capacitor current, I_{Cs}, and (c) inductor currents, I_{L1} and I_{L2}.

Table 2: 2-*pscB* converter MOSFETs.

MOSFET	C_{iss}	V_{DS}	R_{DS} (on)$_{max}$	I_D
IPB530N15N3	667 pF	150 V	53 mΩ	21 A
Si7898 (fly-back)	900 pF	150 V	85 mΩ	4.8 A

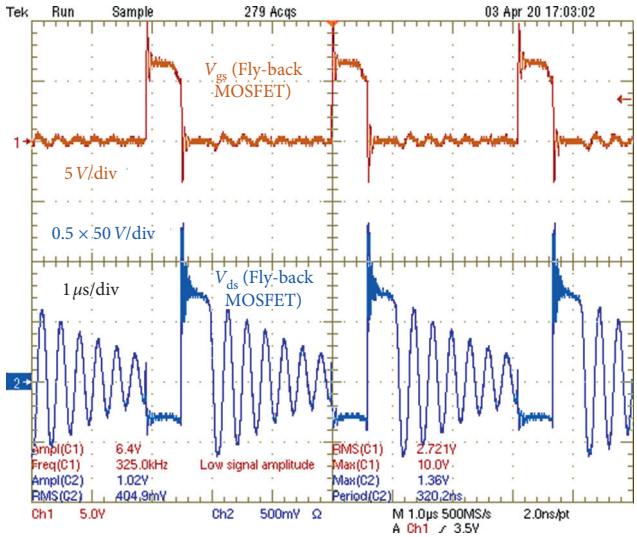


Figure 13: Fly-back gate driver signal, V_{gs} (top waveform), and drain source voltage, V_{ds} (bottom waveform), at the transformer input.

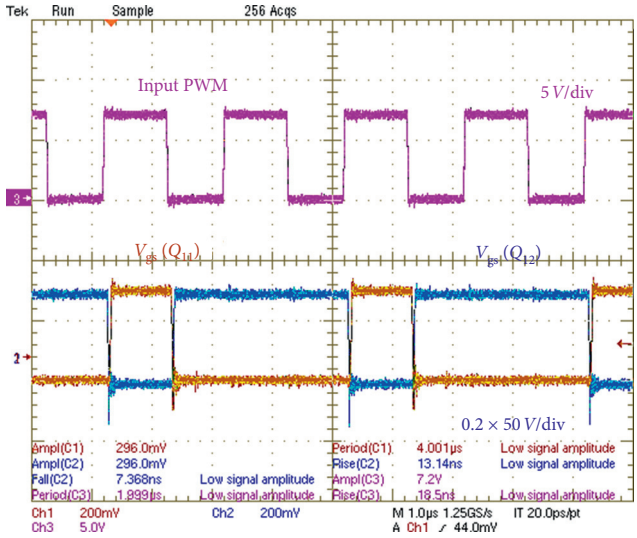


Figure 14: Input PWM signal, D_{Drive} (top waveform), and the gate-source voltages of Q_{11} and Q_{12} (bottom waveforms).

Figure 13. The evaluation model (EVM) input 5 V PWM signal with twice the switching frequency and a double duty cycle to generate four signals through the latch circuit. Input signal and phase A generated gate driver signals are shown in Figure 14. The input PWM signal (D_{Drive}) will be at 500 kHz at 50% duty or less to generate four signals at 250 kHz at 25% duty cycle or less. As such, controlling the four gate signals becomes easier and can be achieved with only the main input

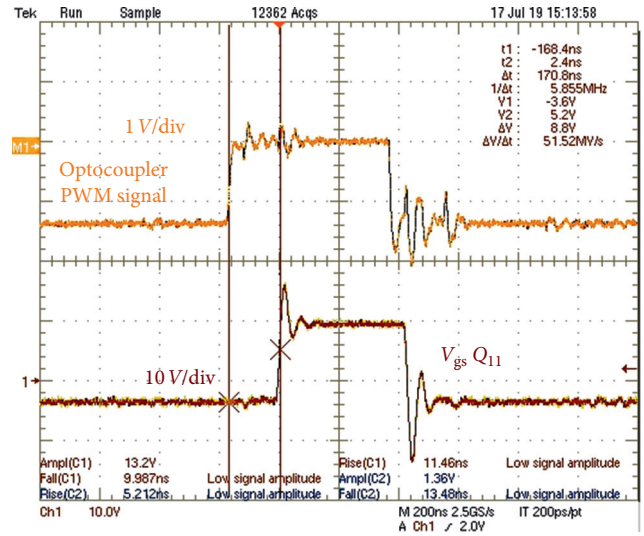


Figure 15: Signal delay between the optocoupler PWM input signal and the gate-source voltage of Q_{11}.

PWM signal. Signal delay time between the optocoupler input and MOSFET gate is measured to be 170 ns which includes the rise time and first propagation delay time as shown in Figure 15. The time delay is 57 ns to include both the fall and second propagation delay times. This difference is caused by the PCB conductors which can be reduced by a better PCB layout as well as a multilayer structure to separate the power conductors from the ground conductors. To achieve the required dV/dt, the gate driver must deliver the gate charge Q_{gd} in 20 ns or less. This means a gate current of $I_g = 3$ nC/20 ns = 0.15 A or higher is needed. However, the MOSFET gate-source current reaches 1.2 A and the sink current is less ($Q_{gd} = 3$ nC maximum, dV_{ds}/d$t = 20$ V/ns) as shown in Figure 16 which is almost similar to the simulated gate current value for a $R_{g(on)\ (ext.)} = 2\,\Omega$, $R_{g(off)\ (ext.)} = 0$ (Figure 11(c)). Figure 17 exhibits the typical waveforms of V_{ds} versus V_{gs} for MOSFET Q_{21} of phase B. Figure 18 shows the node voltages V_{sw1} and V_{sw2} at a switching frequency of 250 kHz. As can be seen, these node voltages have a variation of within 0.5 V. As stated earlier, these node voltages must be the same at full current sharing. Any difference or any small variation is caused by dead time, trace width, and length unbalance of the two phase paths or it can be the result of switching speed due to the different charging and discharging time for the MOSFET's input capacitors (C_{gs}). Since the switch node voltage slope is caused by the load current, as such, the slope of V_{sw1} is affected by the charging period of both Cs and Co. This is because V_{sw2} charges only Co, and then a slope difference can be seen. To eliminate this difference, the value of Cs must be chosen carefully in terms of inductance variations, zero dc bias inductance, saturation profiles, and converter layout and *Cs* position.

Figures 19 and 20 show the series-capacitor current, i_{Cs}, and inductor currents, i_{L1} and i_{L2}, at a resistive load current of 2.4 A, respectively. The phase A inductor current (i_{L1}) has a slightly higher peak-to-peak ripple, due possibly to slope difference and converter layout parasitic inductance. The

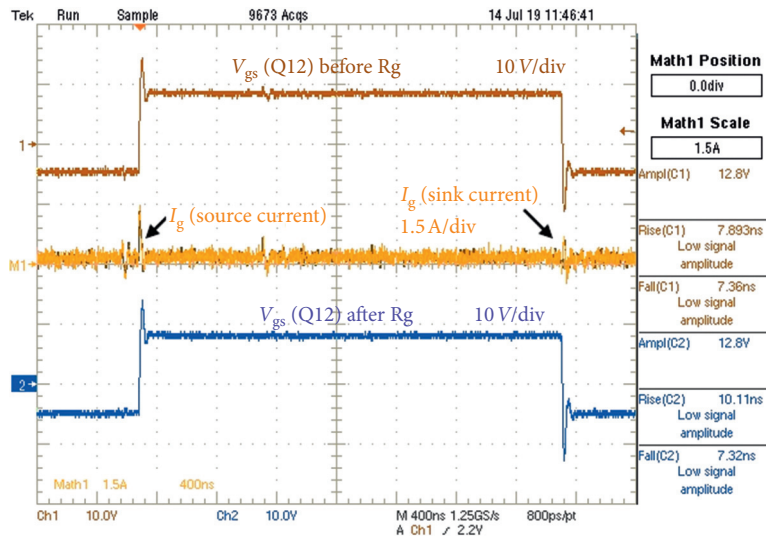


Figure 16: Gate-source voltages of Q_{12} measured before gate resistor R_g (top waveform) and after R_g (bottom waveform).

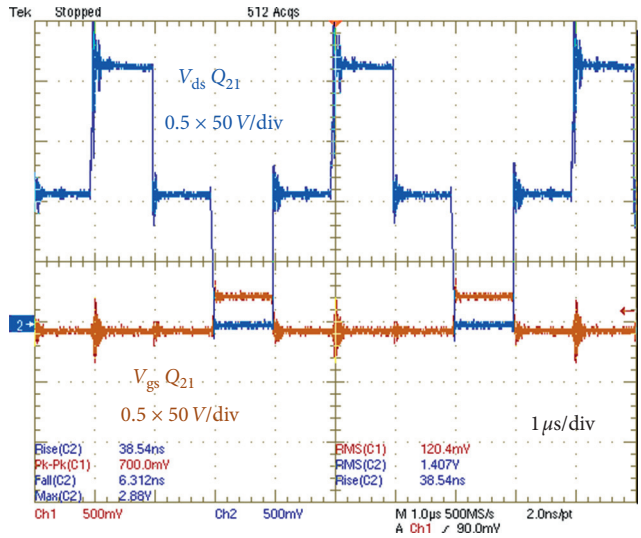


Figure 17: Typical waveforms of V_{ds} and V_{gs} for Q_{21}.

maximum efficiency achieved from this prototype converter is 92% at a load current of 3.38 A and an input current of 442 mA despite the peak-to-peak ripple of about 270 mA due to charging and discharging of both Cs and Co. Prototype is shown in Figure 21. Maximum output power of 73 W with an efficiency of 91% was achieved at a full load current of 6 A. The experimental and simulated efficiency results are illustrated in Figure 22.

8. Discussion

Due to PCB trace drop voltages and layout mismatch of the two phases, there is an expected small variation between the simulation and measured efficiency results. Moreover, wires and component parasitic circuit elements also have a negative impact. Dissipation curves show a normal increase with increasing load currents. Even though there is a small trace resistive unbalance between the two phases, its current sharing mechanism is still functioning well. Because of the above, the node voltage at V_{sw2} is nearly 0.5 V less than that at V_{sw1}. Otherwise, losses are very low when current sharing condition is achieved. For some cases, to reduce losses and provide protection to the MOSFET switches, there is a need to add time delay control circuit to precharge the series capacitor to half of its nominal voltage to protect the converter and reduce the charging current surge before switching on the converter.

Using only one PWM signal input of the latch logic circuit may give an advantage for the closed-loop circuit and simplify the control scheme where the control loop frequency and duty cycle should be twice the actual switching

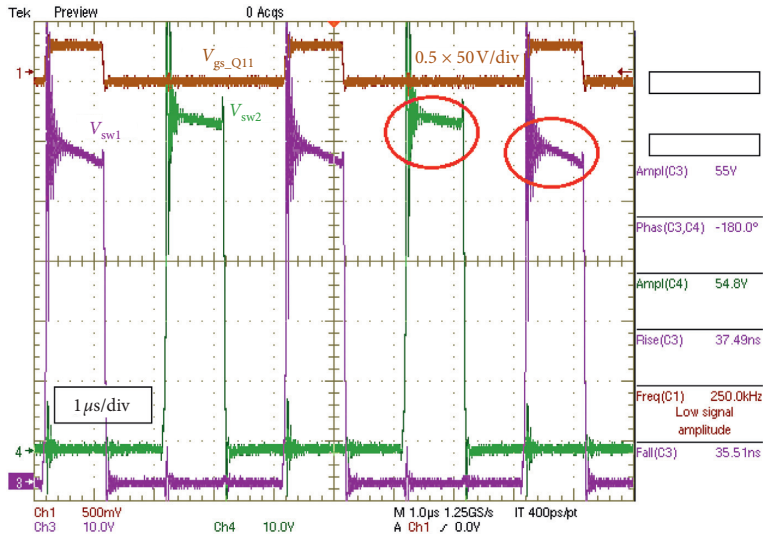


FIGURE 18: Gate pulses of Q_{11} (top waveform) and V_{sw1} and V_{sw2} at 250 kHz (bottom waveforms).

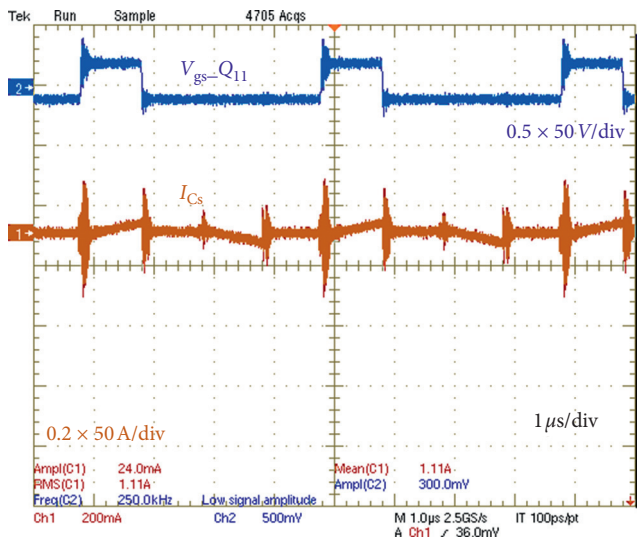


FIGURE 19: Series-capacitor current I_{Cs} at 250 kHz.

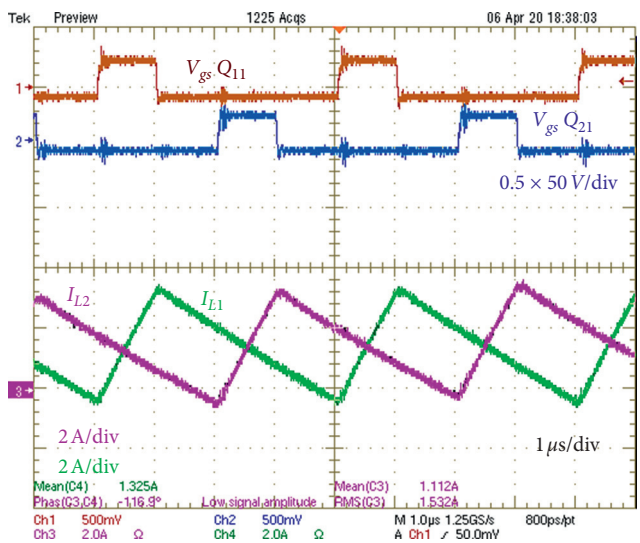


FIGURE 20: Inductor currents, I_{L1} and I_{L2}, at a load current of 2.4 A.

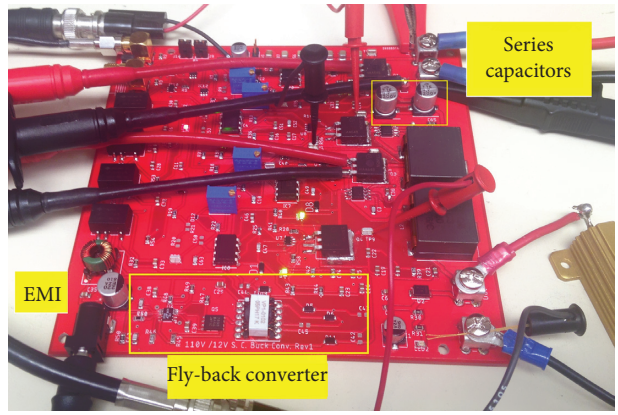


Figure 21: Prototype of the 110 V/12 V/6 A 2-*pscB* converter.

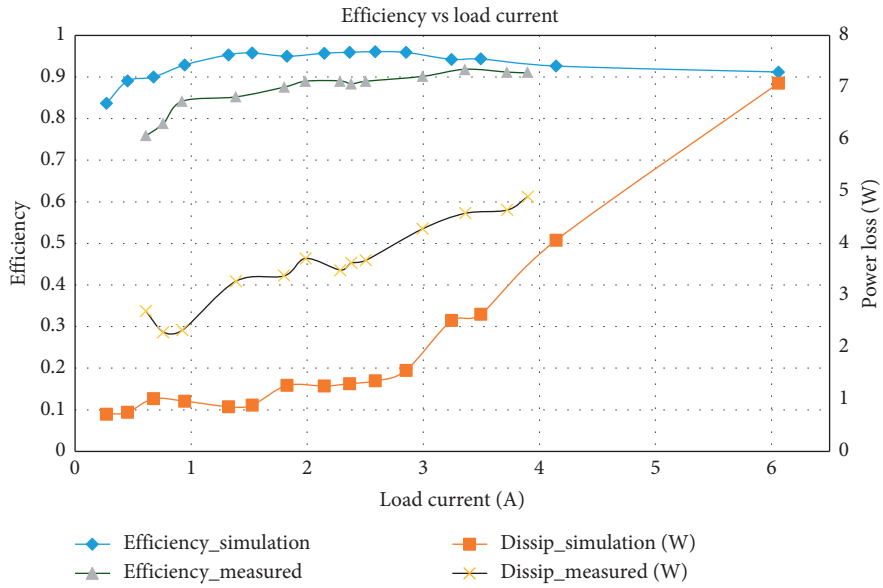


Figure 22: Simulated and experimental efficiencies versus load currents.

frequency. Since the main switches of both the phases are driven at 180° phase shift and with a duty ratio of less than 50%, a push-pull controller can be implemented to achieve this range. Note that the other two MOSFETs for the synchronous rectifier switches (lower side) are just complementary switches. According to Ampere's Law, the physical phase current loop forms a magnetic field in proportion to the output shared current and the phase loop area. This field can couple with other circuit loops such as control circuit (per Faraday's law) with more coupling at higher frequencies, resulting in harmful crosstalk. But this is not the case of this topology since the first and the third mode current loops are nearly opposite in direction and the field will be cancelled out. In this circuit, there is tendency to avoid extra "band-aid" circuitry like snubbers to reduce line current distortion and losses. The proposed 2-*pscB* converter shows a good performance suitable for high-frequency dc/dc applications with high step-down ratios such as those in EV dc power converters and laptop power suppliers. These applications are restricted by physical size, heat dissipation, and inductor variations.

9. Summary

A new theoretical approach to design an automatic current sharing scheme was presented for a 2-phase series-capacitor synchronous buck converter. The effects of its phase unbalance and parasitic circuit elements were discussed. An I^2 current feedback controller was used to regulate the output voltage as well as to balance the two-phase inductor currents.

Experimental results were presented for an 110 V/12V, 6A, 250 kHz 2-*pscB* converter with a new multiphase isolated gate driver.

Data Availability

The simulation and experimintal data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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