Journal of Electrical and Computer Engineering

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Special Issue on

Interconnect Modeling, Design, and Optimization for Design Closure and Emerging Technologies

CALL FOR PAPERS

Realized in the last design step of IC design flow, interconnect has deep impacts on chip characteristics from several aspects, such as timing, power, reliability, parasitics, and design for manufacturability (DFM), where design closure is regarded to successfully meet the requirement in all aspects. The design and optimization of interconnect play a major role in a successful modern VLSI chip design. In this special issue, we solicit original research papers with technical breakthrough in wide topics of interconnect modeling, design, and optimization for design closure and emerging technologies.

Interconnect modeling has been a promising method to analyze and predict the characteristics of interconnect as a foundation for further optimization procedures, especially in 3D IC, carbon nanotube interconnect (CNT), and silicon photonics for next-generation technologies.

The challenges of congestion during the design flow emerge due to the following facts: (i) increased use of embedded IPs and memories that may block metal layers, (ii) smaller die size that can lower manufacturing cost, and (iii) the demand to increase yield. Routability-driven placement attempts to conduct more accurate routing estimation during placement to tackle these challenges.

Signal wire routing and optimization has been under investigation at three different levels, that is, global routing, track routing, and detailed routing. Design closure and DFM issues are two main concerns for signal wire routing of modern designs. Routing with optimized objectives and postrouting optimization, such as gate sizing, buffer insertion, redundant-via insertion, and multipatterning lithography decomposition, have become two research mainstream techniques in signal wire design and optimization.

Clocking wire is another type of interconnect that heavily influences the performance and reliability of circuits. Clock tree synthesis is usually involved in buffer insertion and wire sizing, while parameter optimization in skew, phase delay, and power is also considered in the meantime.

3D ICs and 2.5D ICs provide an attractive solution to improve circuit performance, where the issues of intradie routing, interdie routing, interposer routing, package routing, and flip-chip routing considering thermal and mechanical stress, timing, yield, testability, or diagnosability also need to be addressed.

The performance of analog and RF circuits is strongly affected by the interconnect parasitics. Special constraints, such as symmetry, matching, cross talk, electromigration, and other DFM intricacies, have to be seriously considered in the routing stage of analog and RF physical design. This has become increasingly essential in the nanometer regime.

Potential topics include, but are not limited to:

- Interconnect modeling in 3D IC, carbon nanotube interconnect, and silicon photonics
- Routability-driven placement
- 2D/3D global routing considering timing, layer directives, local net, and so forth and routability estimator for placement
- Detailed routing considering the optimization in delay, reliability, multipatterning lithography, and so forth
- Postrouting optimization such as gate sizing, buffer insertion, and decomposition for multipatterning lithography
- Clock tree synthesis with buffer insertion and wire sizing
- Interconnect design and optimization for 3D and 2.5D ICs
- Modeling of interconnect parasitics and routing techniques to meet the special analog/RF constraints
- IC design with interconnect optimization

Authors can submit their manuscripts via the Manuscript Tracking System at http://mts.hindawi.com/submit/journals/jece/circuits.systems/idodc/.

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