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*Research Article*

# A Novel Method to Grow Vertically Aligned Silicon Nanowires on Si (111) and Their Optical Absorption

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In this study we grew silicon nanowires (SiNWs) on Si (111) substrate by gold-catalyzed vapor liquid solid (VLS) process using tetrachlorosilane ($SiCl_4$) in a hot-wall chemical vapor deposition reactor. SiNWs with 150–200 nm diameters were found to grow along the orientations of all ⟨111⟩ family, including the vertical and the inclined, on Si (111). The effects of various process conditions, including $SiCl_4$ concentration, $SiCl_4$ feeding temperature, $H_2$ annealing, and ramp cooling, on the crystal quality and growth orientation of SiNWs, were studied to optimize the growth conditions. Furthermore, a novel method was developed to reliably grow vertically aligned SiNWs on Si (111) utilizing the principle of liquid phase epitaxy (LPE). A ramp-cooling process was employed to slowly precipitate the epitaxial Si seeds on Si (111) after $H_2$ annealing at 650°C. Then, after heating in $SiCl_4/H_2$ up to 850°C to grow SiNWs, almost 100% vertically aligned SiNWs could be achieved reproducibly. The high degree of vertical alignment of SiNWs is effective in reducing surface reflection of solar light with the reflectance decreasing with increasing the SiNWs length. The vertically aligned SiNWs have good potentials for solar cells and nano devices.

## 1. Introduction

Nanowire devices have attracted a great deal of attention recently because of their potentials for many industrial applications due to their unique properties including single crystal nature, mechanical flexibility, and high-surface areas. For example, many novel devices such as nanowire-based field effect transistors [1, 2], thermoelectric power generation [3, 4], optoelectronic devices [5], solar cells [6–9], and lithium battery [10], and so forth, have been studied due to their unique electric, optical, mechanical, thermal, and material properties that differ from their bulk or thin film counterparts. Particularly, SiNWs have good potentials for application to solar cells, the fabrication of which requires the nanowires to be vertically aligned and synthesized on a substrate. Many methods have been used to synthesize SiNWs including wet etching [11], deep reactive ion etching (DRIE) [12], chemical vapor deposition (CVD) [13, 14], electron beam evaporation (EBE) [15], molecular beam epitaxy (MBE) [16], gold-ion implantation [17], anodized alumina templates [18], oxide patterning [19], metal nanoparticles [20], block-copolymer patterning [21], nanosphere lithography [16], and nanoporous silicon substrate [22]. The catalyst-assisted vapor liquid solid (VLS) growth mechanism is still the most widely used approach for fabricating nanowires due to no requirement of patterning [6, 7]. According to this mechanism, a small eutectic particle acts as a catalyst to decompose and dissolve the gas phase reaction species, and the precursor precipitates out of the catalyst to grow nanowires after supersaturation. SiNWs were usually grown along four ⟨111⟩ family orientations on Si (111) wafers by VLS growths [17, 23–25]. Only a few groups reported the growth of vertically-aligned SiNWs. Vertically-aligned SiNWs could be grown on Si (111) at 850°C using

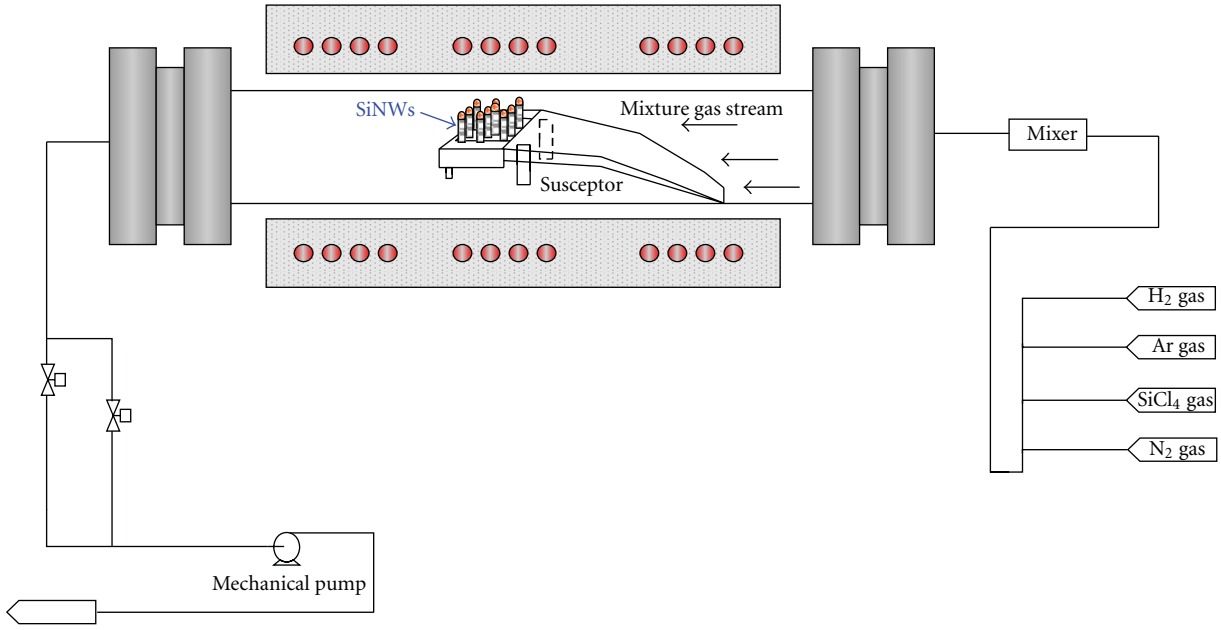



Figure 1: A schematic diagram of the hot-wall CVD system employed in this study to grow SiNWs. The substrate was placed on the boat at the center of the reactor.

$SiCl_4$ precursors since the reaction product HCl might facilitate the nucleation of vertical SiNWs by etching away the native oxide on Si substrate surface [20]. Also, vertically aligned Si microrod arrays could be grown by VLS growth at 1050°C [13]. The vertical alignment might be related with the large diameter of Si rods grown at a higher temperature using a thick catalyst layer. Furthermore, the vertical growths of germanium [26] and III–V [27] nanowires have been achieved by controlling the conditions of heat treatments during the nucleation of nanowires, suggesting the importance of initial heat treatment conditions on the alignment of nanowires.

By following the principle of liquid phase epitaxy (LPE), a high-temperature $H_2$ annealing process was first used to reduce the native oxide and form the Au-Si alloy liquid, and then a ramp-cooling process was employed to carefully precipitate the epitaxial Si seeds on Si (111). After the growth of high-density SiNWs at 850°C on the epitaxial Si seeds, the percentage of vertically-aligned SiNWs along [111] was significantly increased up to 100%, without the need of using a template or patterning the catalyst.

In this study, we used $SiCl_4$ reactants and Au catalyst to grow epitaxial SiNWs of 150–200 nm in diameter on Si (111). The effects of process parameters, including $SiCl_4$ concentration, $SiCl_4$ feeding temperature, $H_2$ annealing, and ramp cooling, on the crystal quality and growth orientations of SiNWs have been studied. The growth conditions were thus optimized. Still only a small percentage (around 30%) of vertically-aligned SiNWs could be grown. A new method was attempted utilizing the principle of liquid phase epitaxy (LPE) for controlling the vertical alignment of epitaxial SiNWs. A ramp-cooling process was employed to slowly precipitate the epitaxial Si seeds on Si (111) after $H_2$ annealing at 650°C. Then, almost 100% vertically-aligned SiNWs could be grown at a growth temperature of 850°C. To our knowledge, we are the first reporting the improvement of nanowire vertical alignment using the principle of LPE. We have already demonstrated that this is a highly reproducible method to grow vertically-aligned SiNWs on Si (111).

## 2. Experimental

A schematic diagram of the reactor used is shown in Figure 1, and the detailed growth procedures are depicted in Figures 2(a) and 2(b). A hot-wall chemical vapor deposition (CVD) system was used to grow SiNWs. The reactor consisted of a quartz tube evacuated by a rotary pump (Edwards E2M30) to attain a base pressure of $5 \times 10^{-3}$ Torr. In this study, SiNWs were grown epitaxially on a Si (111) substrate using the vapor liquid solid (VLS) growth method. Before the growth of SiNWs, the silicon wafer was cleaned by standard RCA process to remove contaminants and then flushed in de-ionized water. The wafer was further dipped in a HF buffer solution (48% HF : $H_2O$ = 1 : 10) for 30 sec to remove the surface native oxide, and then blown dry by high-purity nitrogen from a gas cylinder. Au films of 2-3 nm in thickness were deposited on the cleaned wafers at room temperature by sputtering at a deposition rate of 0.1 nm/sec. Finally, the Au-coated substrates were transferred to the hot-wall chemical vapor deposition (CVD) reactor. Before the growth of SiNWs, the reactor was always pumped to a base pressure below $1.0 \times 10^{-2}$ Torr by purging the mechanical pump with 3 sccm Ar to prevent the backstreaming of pump oil vapor [28]. In order to study the effects of heating

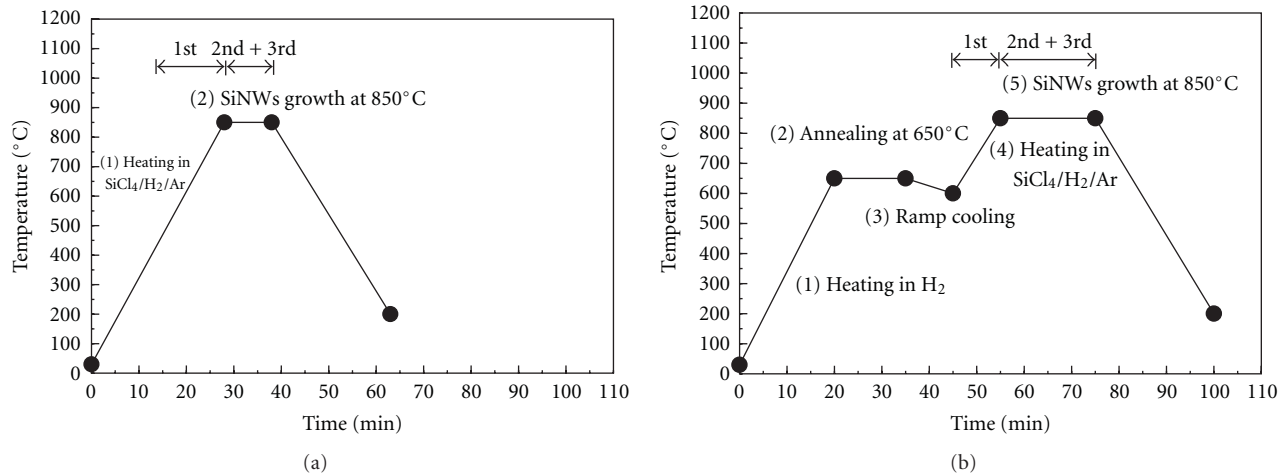



Figure 2: (a) The direct heating procedures for heating up the substrate directly to 850°C for the growth of SiNWs, and (b) the ramp-cooling procedures for annealing in $H_2$ at 650°C, followed by cooling from 650°C to 600°C at 10°C/min and further heating in $H_2$/Ar/$SiCl_4$ to 850°C for the SiNW growths.

processes on the vertical alignment of SiNWs, two processes were employed to heat the substrate to the SiNW growth temperature. For the direct-heating process, as shown in Figure 2(a), the substrate was heated directly from room temperature to 850°C to conduct SiNW growths in two stages, using two concentrations of 0.5% $SiCl_4$ in $H_2$/Ar gas (60/140 sccm) for the first stage (2 min) and 1.0% $SiCl_4$ in $H_2$/Ar gas (60/140 sccm) for the second stage (8 min). High-purity argon (99.9995%), hydrogen (99.9995%), nitrogen (99.9995%), and tetrachlorosilane (99.999%) were used in this study. For the ramp-cooling process, as shown in Figure 2(b), the wafers were annealed in flowing $H_2$ (300 sccm) at 650°C at 24 Torr for 15 min to form the Au-Si alloy melt on the surface [29]. Afterwards, the substrate was ramp cooled for 5 min in hydrogen flow (300 sccm) at the controlled rate to precipitate epitaxial Si seeds on the substrate. (In cases there was no ramp cooling, the substrate was heated up directly in $SiCl_4$/$H_2$/Ar to 850°C after $H_2$ annealing at 650°C). The substrate was then heated up to the SiNW growth temperature of 850°C at a rate of 25°C/min using 0.3% $SiCl_4$ in $H_2$/Ar (60/140 sccm) flow. The addition of a small amount of $SiCl_4$ (0.3%) in $H_2$/Ar during the substrate heating to the growth temperature was important to prevent the remelting of epitaxial Si seed. During the growth of SiNWs, the substrate was kept at a temperature of 850°C and a total pressure of 300 Torr in the gas flow containing 0.5% $SiCl_4$ in $H_2$/Ar (60/140 sccm) for 2 min and 1.0% $SiCl_4$ in $H_2$/Ar (60/140 sccm) for 18 min. Then, the SiNW growth was terminated by stopping the $SiCl_4$ reactant flow, followed by the reactor cooling to room temperature. The morphologies of the SiNWs grown were characterized by field emission scanning electron microscopy (FESEM).

## 3. Results and Discussion

Many process parameters and sequences have been studied in order to grow high-quality vertically-aligned SiNWs. Particularly, the effects of the $H_2$ annealing process and the ramp-cooling process after $H_2$ annealing were investigated.

*3.1. The Effects of $SiCl_4$ Concentrations (without the $H_2$ Annealing Process).* The effects of $SiCl_4$ concentrations were first studied using the typical process sequences to heat up the substrate from room temperature directly to the SiNW growth temperature. As shown in Figure 2(a), the Au-coated substrate was heated directly from room temperature to the SiNW growth temperature (850°C) in one step and maintained at that temperature for the growth of SiNWs. $SiCl_4$ reactant might be fed into the reactor at any temperature between room temperature and the growth temperature. The 1st stage was defined as the stage between the $SiCl_4$ feeding temperature and the SiNW growth temperature. During the SiNW growths, two stages, 2nd (2 min) and 3rd (8 min), were employed by increasing the $SiCl_4$ concentration stepwise at the growth temperature. The periods of the 2nd and the 3rd stages were 2 min and 8 min, respectively. The $SiCl_4$ reactant was always fed to the reactor at room temperature. Hence, the 1st stage always started from room temperature till the growth temperature. By starting to feed $SiCl_4$ reactant into the reactor at the growth temperature (i.e., no 1st stage), we found that the SiNWs grown exhibited poor quality. Therefore, a low concentration of $SiCl_4$ ($\geqq$ 0.3%) was fed to the reactor starting from room temperature to allow the slow reaction of Au catalyst with $SiCl_4$ upon heating, gradually forming the Au-Si alloy catalysts and nucleating the SiNWs.

The plan-view and cross-sectional SEM images of the nanowires grown under various processing conditions are shown in Figure 3. As shown in Figure 3(a), SiNWs of poor quality were grown using 0.3% $SiCl_4$ in all three stages. It seemed that insufficient silicon source at such a low concentration (0.3%) of $SiCl_4$ reactant in the SiNW growth stages, 2nd and 3rd, induced disorder, bending, and kinking to the SiNWs grown. As shown in the SEM image in Figure 3(b), by using a low concentration (0.3%) of $SiCl_4$ for

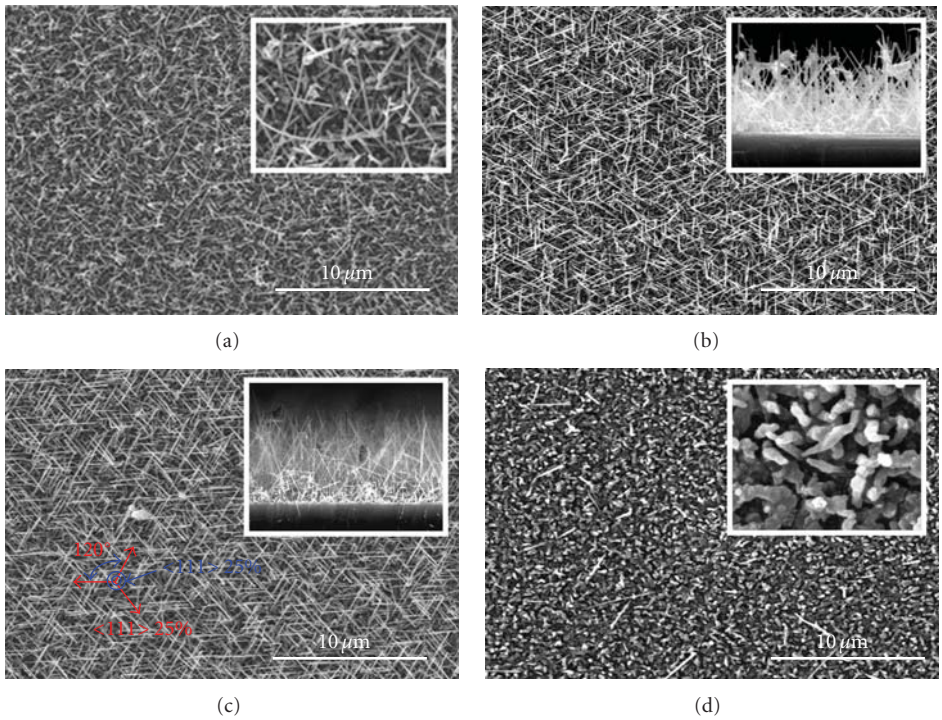



Figure 3: Plan-view and cross-sectional SEM images of the SiNWs grown employing the direct-heating procedures in Figure 2(a) using various concentrations of $SiCl_4$ at the 1st/2nd/3rd stages: (a) 0.3/0.3/0.3%, (b) 0.3/0.5/0.5%, (c) 0.3/0.5/1.0%, and (d) 1.0/1.0/1.0% without $H_2$ annealing process. The total gas flow rate was 200 sccm.

the 1st stage and a higher concentration (0.5%) of $SiCl_4$ for the 2nd and 3rd stages, good quality SiNWs along certain orientations could be grown at 850°C to a length of 3–6 $\mu$m for a period of 10 min. The percentage of vertical SiNWs along [111] orientation was around 25%. A further increase of $SiCl_4$ concentration in the 3rd stage from 0.5% (in Figure 3(b)) to 1.0% (in Figure 3(c)) could further enhance the quality of SiNWs and improve the growth orientations of SiNWs along ⟨111⟩ family. Here, the growth of SiNWs along ⟨111⟩ family indicated the epitaxial growth of SiNWs on Si (111) [17]. However, by further increasing the $SiCl_4$ concentrations up to 1.0% for the 1st, 2nd, and 3rd stages, poor-quality silicon nanorods with irregular shapes and distortion were grown, as shown in Figure 3(d). The growth of low-quality Si nanorods using a high concentration of $SiCl_4$ might be due to the poisoning of Au catalyst resulted from the excess silicon source in the 1st stage. In summary, a small concentration of silicon source (0.3% $SiCl_4$) should be used in the 1st stage during heating the substrate from room temperature to the growth temperature, and the $SiCl_4$ concentrations of two stages must be optimized (0.5% $SiCl_4$ for the 2nd and 1.0% $SiCl_4$ for the 3rd stages) to obtain good quality SiNWs with epitaxial growth orientations. The quality of SiNWs was sensitive to the concentration of $SiCl_4$ in each stage. The SiNWs deteriorated by increasing or reducing the concentrations of $SiCl_4$ at optimum.

*3.2. The Effects of $SiCl_4$ Feeding Temperature (without the $H_2$ Annealing Process).* As described previously, the nanowire quality was not good by starting to feed $SiCl_4$ into the reactor after the reach of growth temperature (i.e., feeding $SiCl_4$ only in the 2nd and 3rd stages, but not in the 1st stage) by one-step growth process. Therefore, in Section 4, a low concentration of $SiCl_4$ was fed into the reactor for the 1st stage starting at room temperature to optimize the catalytic activity of Au-Si alloy for the VLS growth. In this section, the temperature to start feeding $SiCl_4$ into the reactor was varied in order to study its effects on the SiNW growth behavior without the additional $H_2$ annealing process. The 1st stage was already defined as the period from the $SiCl_4$ feeding temperature to the SiNW growth temperature. Both the 2nd and the 3rd stages were at the growth temperature, 850°C. As shown in Figure 4, the effects of $SiCl_4$ feeding temperature on the characteristics of SiNWs grown at 850°C and 300 Torr were studied by controlling the gas reactants in each stage. Only $H_2$/Ar (60/140 sccm) gases flowed in the reactor from the room temperature to the $SiCl_4$ feeding temperature, then 0.3% $SiCl_4$ was added in the $H_2$/Ar in the 1st stage, 0.5% $SiCl_4$ was added in the $H_2$/Ar in the 2nd stage (2 min), and finally 1.0% $SiCl_4$ was added in the $H_2$/Ar in the 3rd stage (8 min). The growth of SiNWs on Au/Si above 600°C should follow the VLS growth mechanism. For the high $SiCl_4$ feeding temperatures at 850°C and 800°C in Figures 4(a) and 4(b), respectively, the silicon nanowires were not well aligned and had very rough surface due to the formation of many tiny branches on the surface, indicating the extremely poor crystal quality of the nanowires. The performance of Au-Si catalyst seemed to deteriorate due to the fast reaction of $SiCl_4$ with Au at such high temperatures.

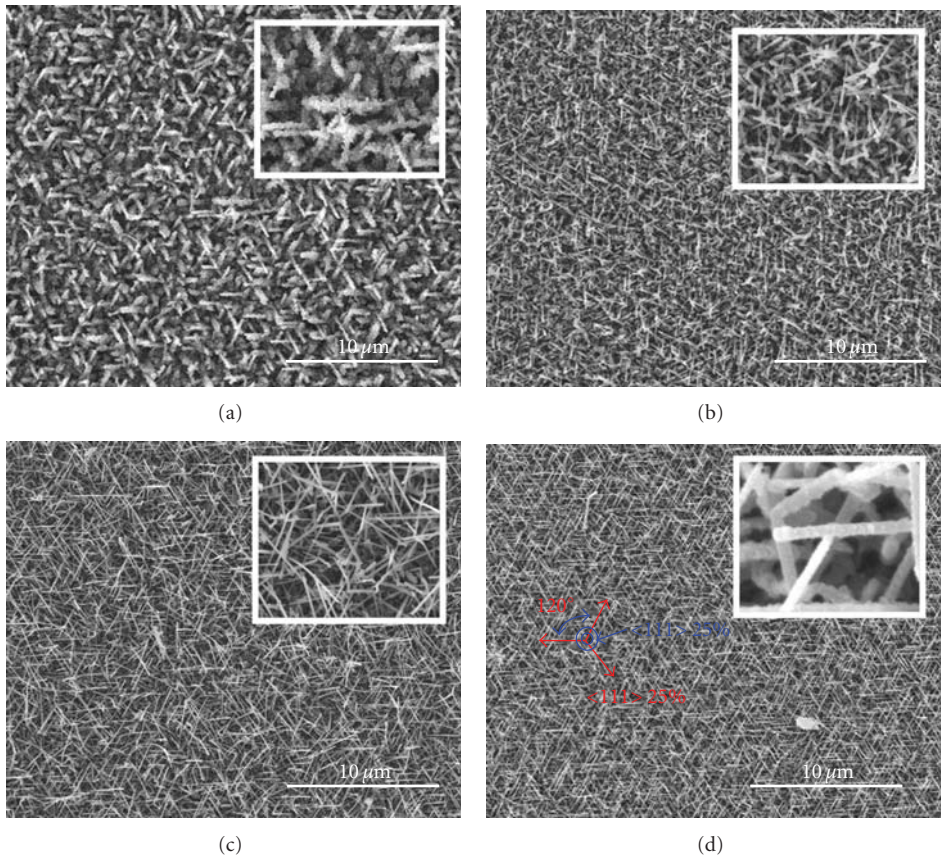



Figure 4: Plan-view SEM images of the SiNWs grown with various $SiCl_4$ feeding temperatures: (a) 850°C, (b) 800°C, (c) 700°C, and (d) 600°C employing the direct heating procedures without $H_2$ annealing.

For some reasons, most of side branches did not have catalyst particles at the tips, which are usually observed for the nanowires grown by VLS mechanism [30]. As shown in Figure 4(c), by lowering the $SiCl_4$ feeding temperature down to 700°C, good-quality SiNWs with very smooth surface could be grown. However, the SiNWs were slightly bended and not well aligned along ⟨111⟩. By further reducing the $SiCl_4$ feeding temperature down to 600°C, the high-quality and well-aligned epitaxial SiNWs (basically along the orientations of ⟨111⟩ family) with smooth nanowire surface could be grown, as shown in Figure 4(d). The SiNWs grown by feeding $SiCl_4$ from 600°C were basically the same as those by feeding $SiCl_4$ from room temperature. As shown in the inset of Figure 4(d), the modulation of the nanowire diameter along the axial direction was observed, perhaps due to the migration of Au catalyst along nanowire or the instability of supersaturation of liquid Au-Si as proposed by Givargizov [31, 32]. The results suggest that the $SiCl_4$ feeding temperature significantly affect the quality and alignment of SiNWs. The fast reaction of $SiCl_4$ with the catalyst seems to induce poor quality and poor alignment of SiNWs. The slow and gradual reaction of $SiCl_4$ with the catalyst enhances the quality and alignment of SiNWs, promoting the growths of epitaxial SiNWs on Si (111) along the orientations of ⟨111⟩ family.

*3.3. The Effects of the Annealing of Au/Si Substrate in $H_2$.* $H_2$ annealing of the Au/Si substrate was attempted to remove the surface native oxide on Si substrate for achieving the epitaxial growth of high-quality SiNWs, since the interface between Au catalyst and Si substrate should be influential on the nucleation of SiNWs. Hopefully, vertically aligned SiNWs would be obtained for clean Si surface. The Au/Si substrates were thus annealed in $H_2$ at various temperatures for 15 mins, and then heated to 850°C to perform SiNW growths. The $H_2$ annealing below 650°C was found to slightly improve the vertical alignment of SiNWs. But the SiNW growth after 700°C $H_2$ annealing was highly irreproducible. Sometimes the alignment of SiNWs was improved by annealing, sometimes a very low density of SiNWs with large diameters were grown, and sometimes only flat island-like surface structures were formed with no growth of SiNWs. After the $H_2$ annealing of Au/Si at 750°C and 800°C, we observed no growth of SiNWs at all, which was probably due to the complete dissolution of Au nanoparticles into the thick silicon substrate at a higher temperature, since only 2-3 nm Au film was deposited. For $H_2$ annealing at a really high temperature (~1,000°C), SiNWs could be grown without supplying any gas phase reactant through the solid-liquid-solid growth mechanism by first forming liquid Au-Si catalyst particles and then continuous into catalysts to

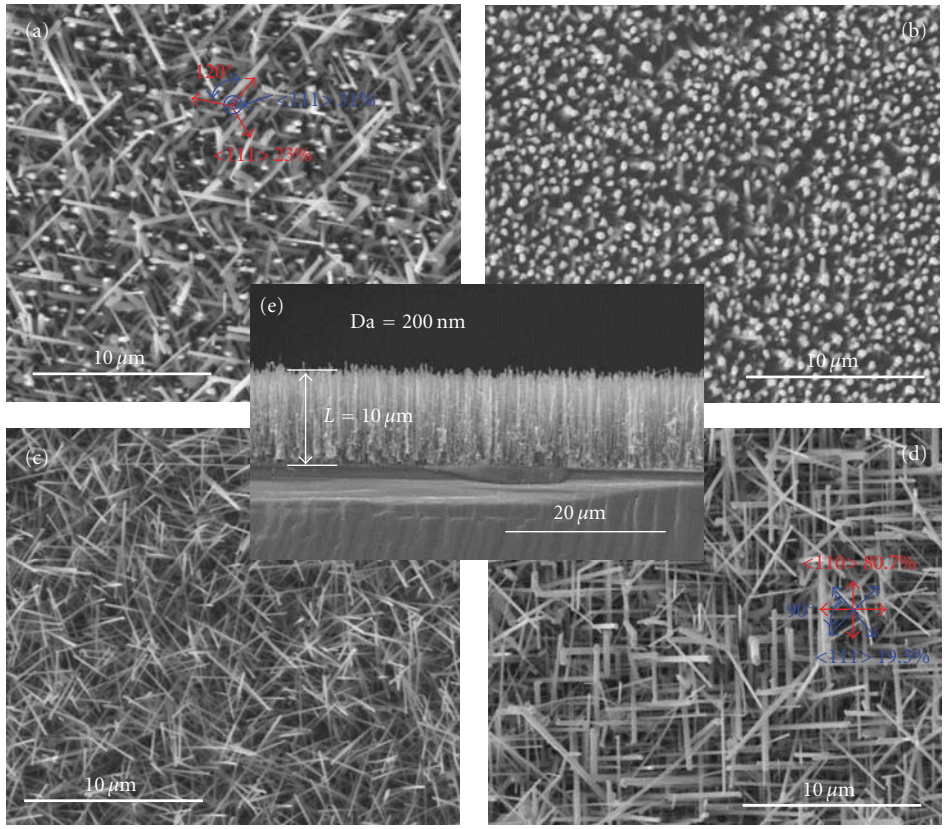
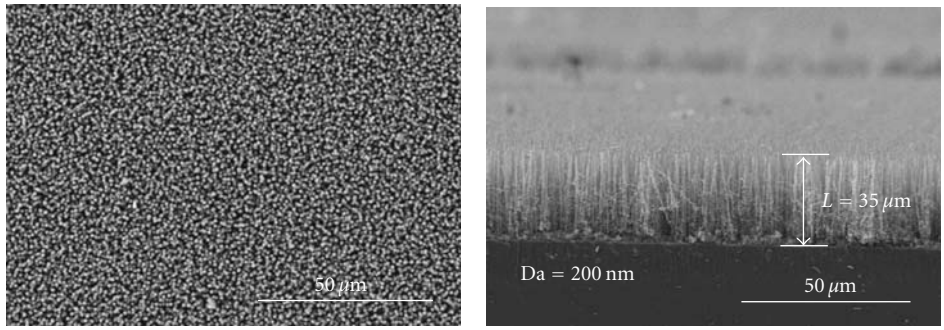



Figure 5: Plan-view SEM images of the SiNWs grown at 850°C for 20 min by employing (a) direct heating procedures, and (b), (c), and (d): ramp-cooling procedures in Figure 2(b) on the Si (111), glass, and Si (100) substrates, respectively, by $H_2$ annealing at 650°C, ramp cooling to 600°C, and heating in $SiCl_4/H_2/Ar$ to 850°C for the growth of SiNWs. Each dot represents a nanowire vertical to the substrate. The cross-sectional SEM image of sample (b) is shown in (e).

precipitate out SiNWs. Therefore, $H_2$ annealing was always performed at 650°C to maximize the density of nanopillars. The 650°C $H_2$ annealing was found to slightly improve the alignment of SiNWs grown at 850°C.

*3.4. The Effects of Ramp Cooling after 650°C $H_2$ Annealing.* After 650°C $H_2$ annealing, the Au/Si substrate was ramp cooled to 600°C for feeding $SiCl_4$, and then heated to 850°C in $SiCl_4$ to perform SiNW growths by increasing the $SiCl_4$ concentration in two steps. Without ramp cooling, the Au/Si substrate, after 650°C $H_2$ annealing, was heated in $SiCl_4$ directly to 850°C to grow SiNWs. As shown in Figure 5(a), epitaxial SiNWs were observed to grow on Si (111). The percentage of vertical SiNWs along [111] orientation was around 31%. With ramp cooling at a rate of 10°C/min, the Au/Si substrate, after 650°C $H_2$ annealing, was first cooled to 600°C in $H_2$, and then heated in $SiCl_4$ to 850°C to grow SiNWs. Figures 5(b) and 5(e) show the plan-view and the cross-sectional SEM images, respectively, of the SiNWs on Si (111) with ramp-cooling process. The small dots in the plan-view image in Figure 5(b) indicated the vertical alignment of each SiNW, and the straight SiNWs shown in Figure 5(e) indicated the high-quality SiNWs with vertical alignment. Basically, most of the SiNWs (>95%) were in vertical orientation along [111] on the Si (111) substrate. The diameter and the length of SiNWs were around 200 nm and 10 $\mu$m, respectively.

As shown in Figure 5, the ramp-cooling process significantly improved the orientation of epitaxial SiNWs on Si (111) from ⟨111⟩ family to [111] only. The ramp-cooling process was suspected to induce the formation of epitaxial Si seed favorable for vertical growths of SiNWs. $H_2$ annealing process at 650°C removed the native oxide on Si surface and formed liquid Au-Si alloy nanoparticles, which became supersaturated with Si and precipitated out Si epitaxy on the Si (111) substrate during the cooling to 600°C, similar to the liquid phase epitaxy (LPE) process. Although without the cooling process the epitaxial SiNWs were grown along the four directions of ⟨111⟩ family, the epitaxial SiNWs were grown only along the vertical direction, [111], after employing the ramp-cooling process. Besides, it was highly important to feed a small amount of $SiCl_4$ (0.3%) into the reactor during the raise of the substrate temperature from 600°C to 850°C for SiNW growths, because the small $SiCl_4$ flow would maintain the supersaturation of Au-Si alloy and prevent the dissolution of epitaxial Si seed into the liquid Au-Si alloy again in raising the temperature. The growth of SiNWs employing the ramp-cooling process was also attempted on the glass substrate under the same conditions as those on the silicon wafer (Figure 5(b)). As shown in




(a) (b)

Figure 6: (a) Plan-view and (b) cross-sectional SEM images of the SiNWs grown at 850°C for a long growth period of 120 min on Si (111) employing the ramp cooling procedures.

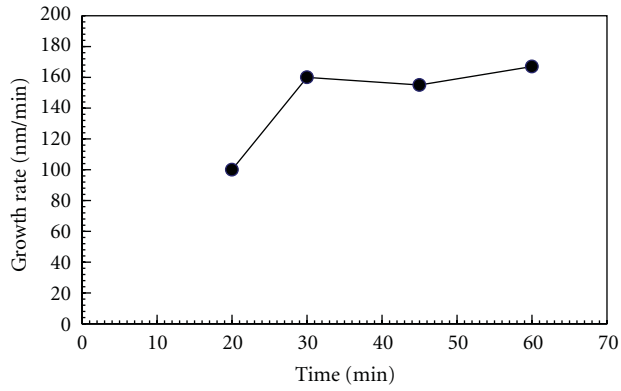



Figure 7: The growth rates of the vertically aligned SiNWs on Si (111) at various growth periods for the SiNW growth at 850°C employing the ramp-cooling procedures.

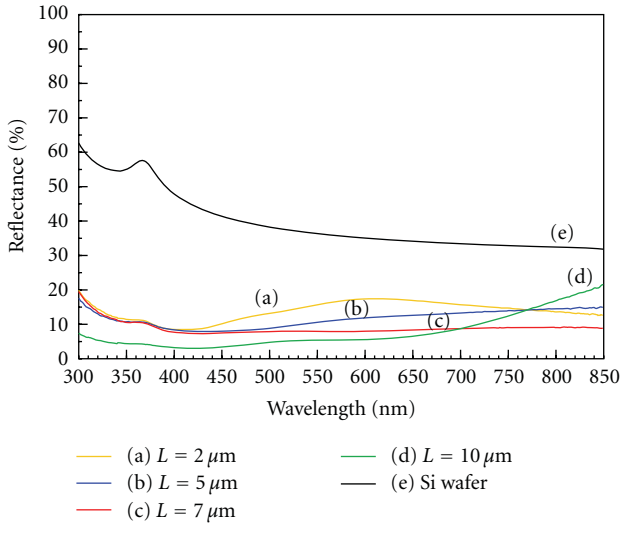



Figure 8: The reflectance spectra of the SiNWs grown on Si (111) with a height of (a) 2 $\mu$m, (b) 5 $\mu$m, (c) 7 $\mu$m, and (d) 10 $\mu$m for different growth time periods employing the ramp-cooling procedures, and those of (e) the blank silicon wafer.

Figure 5(c), the SiNWs grown on the glass substrate were around 3–6 $\mu$m in length and 20–100 nm in diameter, but not as vertical as those on Si (111). As shown in Figure 5(d), the growths of SiNWs on Si (100) wafer were further studied employing the ramp-cooling process, and the SiNWs were found to grow along the ⟨111⟩ and ⟨110⟩ families, but not along the vertical [100] direction as originally expected [33]. The percentages of SiNWs along ⟨111⟩ and ⟨110⟩ orientations were around 19% and 81%, respectively. However, the growth of vertically-aligned SiNWs on Si (111), as shown in Figure 5(b), was highly reproducible. By repeating the same procedures, much longer vertically-aligned SiNWs could be grown by increasing the growth time from 20 min to 120 min. As shown in the plan-view and the cross-sectional SEM images in Figures 6(a) and 6(b), respectively, 35 $\mu$m-long high-density SiNWs with almost perfect vertical alignment could be achieved without using a template or patterning the catalyst. The diameter of SiNW was around 200 nm, and the area density of SiNWs was $9 \times 10^8/\text{cm}^2$. By employing the ramp-cooling process, the growth rates of SiNWs were measured and plotted in Figure 7 versus the time period of the SiNW growth at 850°C. The growth rate was near 100 nm/min after 20 min growth, and then increased to reach a saturated value of 160 nm/min at 30 min.

As shown in Figure 8, the optical reflectance of the vertically-aligned SiNWs with various growth time periods was examined and compared with that of planar Si (111) wafer in the UV-visible region. The reflectance of the SiNWs (2, 5, 7, and 10 $\mu$m in length) was in the range of 5–20%, significantly lower than that of a planar Si (111) wafer (higher than 40% for the whole spectra). When encountering the film of vertically-aligned SiNWs, the photons would penetrate the surface of SiNW film to be scattered between the nanowires in parallel to be absorbed. On the other hand, the blank Si wafer would induce light reflection at a highly smooth surface due to an abrupt change of the refractive index at the interface. The lower reflectance of SiNWs indicated the lower-light loss for the vertically-aligned SiNWs than the Si wafer. As shown in Figure 8, the reflectance of SiNWs basically decreased with the increase of the SiNW growth time and thus the increasing lengths

of SiNWs. However, for the longest SiNWs (10 $\mu$m, 60 min growth, Figure 8(d)), the reflectance was the lowest (less than 10%) in a wide wavelength region (300–700 nm), but greatly increased to above 20% with increasing the wavelength range to 700–850 nm due to the high-density and uniform length of SiNWs [34]. The surface of the 10 $\mu$m vertically-aligned SiNW film became highly dense and very smooth with respect to the photons with long wavelengths (700–850 nm), so the photons started to be reflected from the surface of SiNW film. In summary, the high degree of vertical alignment of SiNWs in this study is essential for SiNWs to reduce the light reflection. The reduction of light reflectance is favorable for improving the solar cell efficiency. Further reduction of reflectance may be expected by optimizing the growth conditions of SiNWs.

## 4. Conclusions

SiNWs were grown in a hot-wall CVD reactor using $SiCl_4$ reactant by Au-catalyzed VLS process. Epitaxial SiNWs were found to grow along the orientations of all four ⟨111⟩ family on Si (111). The process conditions were optimized by studying the effects of various process parameters on the crystal quality and growth orientation of SiNWs.

A novel process utilizing the principle of LPE was developed in this study to significantly improve the vertical alignment of epitaxial SiNWs on Si (111). Here, a ramp-cooling process was employed to slowly precipitate the epitaxial Si seeds on Si (111) after $H_2$ annealing at 650°C. Then, almost 100% vertically-aligned SiNWs could be grown at a growth temperature of 850°C. The process has been demonstrated to be a highly reliable method to grow vertically-aligned SiNWs on Si (111). The vertically-aligned SiNWs have good potentials for solar cells and nano-devices. This method may be applicable to other nanowire materials for controlling the orientation of nanowires on single-crystal substrates. To our knowledge, we are the first reporting the improvement of vertical alignment of nanowires using the principle of LPE.

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