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Research Article

Influence of Weight Ratio of Poly(4-vinylphenol) Insulator on Electronic Properties of InGaZnO Thin-Film Transistor

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Spin-coated organic PVP layers were used as dielectric layers in a-IGZO TFTs. Weight ratios of 20 : 1, 10 : 1, and 5 : 1 for PVP and PMF, a cross-linking agent, were used. The a-IGZO TFTs with the PVP : PMF ratio of 20 : 1 showed a large hysteresis in the *I-V* curve and *C-V* curve, the hysteresis increases with the increase of hydroxyl groups and also deteriorated the gate leakage current. In contrast, the devices with the PVP : PMF ratio of 5 : 1 dielectric displayed only small hysteresis. According to our experimental results, preventing the possible diffusion of hydroxyl-contained species in polymeric dielectrics is a very important factor in improving the electrical properties of high-performance a-IGZO TFT devices.

1. Introduction

Previously, hydrogenated amorphous silicon (a-Si:H) was widely used for the fabrication of the channel layer of thin-film transistors (TFTs); however, some of the inherent characteristics of these films, such as lower mobility ($\sim 1\,cm^2/Vs$) and poor transparency, have limited their applications. In recent years, amorphous indium-gallium-zinc oxide (a-IGZO) has been widely used for the above-mentioned purpose; this is because it affords advantageous properties such as high field-effect mobility, wide band gap, and high uniformity over large areas, and it can be used to form films via a low-temperature process (<200°C) [1–3]. In fact, Hosono indicated that an a-IGZO system has high mobility ($>10\,cm^2/Vs$) because of the isotropic shape of the s-orbitals of metal cations in a-IGZO [1, 4]. Additionally, thin films formed using a-IGZO feature high electron mobility and good controllability over the carrier concentration. Recently, high-performance a-IGZO TFTs with high mobility, high I_{on}/I_{off} ratio, and very good subthreshold swing (SS) have been reported [5–7].

Poly(4-vinylphenol) (PVP), an organic dielectric, has been widely utilized in organic thin-film transistors (OTFTs) because it is inexpensive and can be used for the fabrication of films having a large area, making it particularly useful for applications to flexible electronics. Klauk et al. [8] reported that pentacene TFTs with spin-coated PVP gate dielectric layers had better electrical properties than TFTs with thermally grown SiO_2 gate dielectric layers. Lee et al. [9] reported on the fabrication of pentacene-based thin-film transistors (TFTs) with poly-4-vinylphenol (PVP)/yttrium oxide (YO_x) double-gate insulator films. However, we also can obtain lower roughness and high performance electric properties of TFTs. Bang et al. [10] reported they compared the characteristics of bottom-gate ZnO-thin film transistors using poly-4-vinylphenol (PVP) and PVP/Al_2O_3 dielectrics. Overall, alternative methods for the fabrication of organic gate dielectrics, such as printing, spray coating, and spin coating, have attracted considerable attention because these are inexpensive and flexible techniques. The use of PVP as a polymer insulator has enabled numerous advancements, and some studies have focused on the effects of the dielectric properties of polymer insulators on device performance [11]. However, several groups have investigated the hysteresis effect with different weight ratios of polymer gate dielectric layer [12, 13]. Such studies have been reported to clarify the relationship between the weight ratio of the constituents of the PVP insulator and the electric properties of the device.

Utilizing of polymer gate dielectric layer almost was applied to organic thin film transistors (OTFTs) that it had poor mobility and instability of devises. Besides, OTFTs were very sensitive with H_2O, oxygen, and ultraviolet light, especially, the performance of devices were deteriorated as current crossed organic materials. Therefore, we are interested in the performance and hysteresis effect of inorganic thin film transistor devices with PVP : poly(melamine-coformaldehyde) methylated (PMF) different weight ratios. In addition, the influence of the dielectric roughness on the performance of TFT, which may contribute to the lowering of the mobility with increasing roughness, has been reported in some papers [14–17].

In this study, we report on the fabrication of TFTs using organic PVP : PMF dielectric layers and inorganic a-IGZO active layers. In order to investigate the effects of varying the PVP : PMF weight ratio of the insulator on the electric properties of TFTs. We discuss the effects of different weight ratios of PVP and the cross-linking agent on the TFTs. Consequently, different weight ratios of the polymer dielectric layer with large hysteresis were observed. In a-IGZO TFT devices were confirmed to be strongly related to the hydroxyl bonds existing inside of polymeric dielectrics.

2. Experimental Details

An aluminum (Al) gate electrode was deposited on a glass substrate by thermal evaporation. The polymer solution for the dielectric layers was prepared by dissolving PVP and poly(melamine-coformaldehyde) methylated (PMF), a cross-linking agent, in propylene glycol monomethyl ether acetate (PGMEA) (approximately 80∼90 wt%) with weight ratios of 20 : 1, 10 : 1, and 5 : 1. The PVP solution was spin-coated on the substrate at 1000 rpm for 60 s and was cross-linked by heating in an oven for 90 minutes at 200°C. The thickness of the dielectric layers was determined to be approximately 550 nm by field-emission scanning electron microscopy (FE-SEM) at 10 keV. 50 nm thick active layers of a-IGZO were then deposited by radio frequency (RF) sputtering. An a-IGZO thin films was fabricated on a glass substrate by rf magnetron sputtering with pure IGZO (atom ratio $In_2O_3 : Ga_2O_3 : ZnO = 1 : 1 : 1$ mol%, 99,99% pure) with a diameter of 3 inches. The RF power, chamber pressure, and $O_2/Ar + O_2$ ratio were 112 W, 20 mTorr, and 0.16%, respectively. Finally, Al layers were thermally evaporated onto the a-IGZO films to serve as the source and drain electrodes. The gate length, L, and gate width, W, of the fabricated a-IGZO TFTs were 100 and 1000 μm, respectively. The current-voltage (I-V) characteristics of our devices were measured using a B1500 semiconductor parameter analyzer.

3. Results and Discussion

Fourier-transform infrared (FTIR) spectroscopy is a powerful technology for studying intermolecular interactions in polymers. PVP : PMF layers with weight ratios of 20 : 1, 10 : 1, and 5 : 1 were spin-coated on glass substrates for FTIR measurement. Figure 1 illustrates the infrared spectra

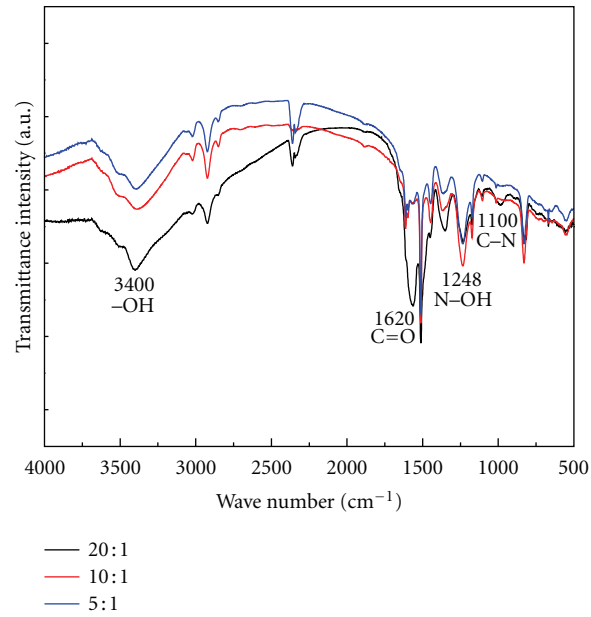

Figure 1: FTIR spectrum of thin films with different PVP : PMF ratios.

of these PVP layers in the range of 500–4000 cm^{-1}. In the PVP : PMF FTIR spectrum, the band corresponding to the C–N stretching vibration at 1019 cm^{-1} [12] and the strong band corresponding to the C=H stretching vibration at 1380 cm^{-1} and 1447 cm^{-1} which are assigned to the inner face bending vibration of hydroxyl group [13]. The bending vibration mode of hydrogen-bonded H_2O appears at 1620 cm^{-1} [14]. A broad and intense band in the range 3100∼2500 cm^{-1} is ascribed to the stretching vibration of the associated hydroxyl group. The band at 2900 cm^{-1} is attributed to the characteristic stretching vibration of C–H band [12]. It is found that an increase in the PVP : PMF weight ratio with decrease in the intensity of the OH peak at 3400 cm^{-1}, indicating there are effectively a higher number of hydroxyl groups, in the 20 : 1 which absorb the IR radiation and decrease the transmittance. This indicates that there are more hydroxyls in the 20 : 1 ratio than the others. PVP contains many hydroxyl groups, as evidenced by its chemical formula [8] is in agreement with our PVP : PMF FTIR spectrum. Lee et al. [12] reported that electron trappings related to the hydroxyl groups were increased, causing a large gate leakage current. Therefore, a PVP : PMF ratio of 20 : 1 could accommodate much a more number of hydroxyl groups inside and at the surface of the gate dielectric interface defect. Due to mobile charges in the gate dielectric or a low trap density at the interface between the PVP dielectrics and the a-IGZO semiconductor layer.

However, in order to clarify and characterize the dielectric properties of various polymers with different amount of hydroxyls groups, the capacitance-voltage (C-V) characteristics for devices containing PVP : PMF layers are measured at 1 MHz and shown in Figure 2. The capacitor structure is Au/insulator PVP : PMF layers/n-Si. The C-V curves exhibit significant strong accumulation, accumulation, and depletion regions as well as an obvious hysteresis effect.

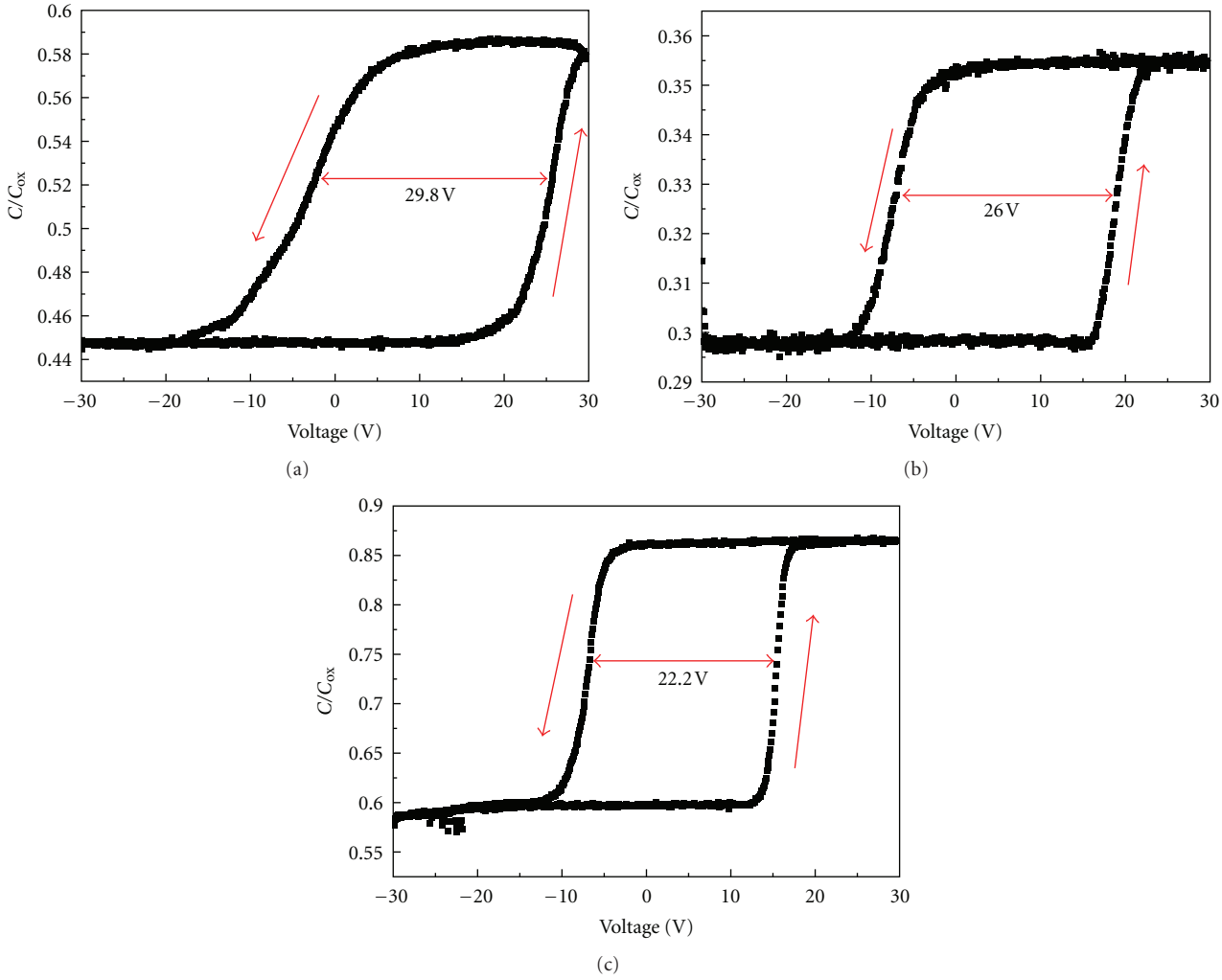

Figure 2: Capacitance-voltage characteristics of n^+Si/PVP/Au MIS diode at 1 MHz. The arrows indicate the sweep direction of the gate bias voltage with PVP : PMF ratios of (a) 20 : 1, (b) 10 : 1, and (c) 5 : 1.

When the voltage is swept from −30 V to 30 V across the MOS capacitor, the semiconductor surface moves from the depletion region to the accumulation region and finally to the strong accumulation region; the voltage is then swept back from 30 V to −30 V, and a large hysteresis was observed. The hysteresis curves were apparent, that for PVP : PMF of 20 : 1, 10 : 1, and 5 : 1, the voltage shifts were 29.8 V, 26 V and 22.2 V, respectively.According to the *C-V* results, the hysteresis characteristic of polymer dielectric has a high content of hydroxyl groups to correspond with the FTIR spectra. The gate bias was swept back to check the amount of hysteresis originating from the bulk or interface charge trapping. A significant amount of hysteresis was observed for the sample which was PVP : PMF of 20 : 1 and hysteresis increase with the increase of hydroxyl groups. The hysteresis curves indicate the presence of charges trapped at or near the interface between the semiconductor and gate insulator [18]; they are charged when the devices are driven into the depletion region and discharged when they move into the strong accumulation region. Therefore, we observed that the hysteresis of PVP : PMF dielectric was mainly caused by hydroxyl groups from bulk material not from interface between the semiconductor and gate insulator. This demonstrates that the large hysteresis was introduced by the PVP : PMF layers which possible to consider the application for nonvolatile memory devices.

The *C-V* characteristics of Al/PVP/Au are shown in Figure 3. Cross-section images were observed by a field emission scanning electron microscope (FESEM) operated at 5 keV (not shown). Hence, the thicknesses of PVP layers are about 550 nm, 520 nm, and 600 nm for mole ratio of 20 : 1, 10 : 1, and 5 : 1, respectively. The dielectric constants k of the polymer insulators are as obtained with the following equation [19]:

$$k = \frac{C \cdot d}{\varepsilon_0 A}, \tag{1}$$

where C is the capacitance of the insulator, A is the dot area 0.04 cm^2, d the insulator thicknesses 550 nm, 520 nm, and 600 nm, respectively. ε_0 is the permittivity in vacuum 8.85×10^{-14} F/cm. The capacitance, C, was obtained from *C-V* measurements Agilent 4284A. PVP : PMF layers with

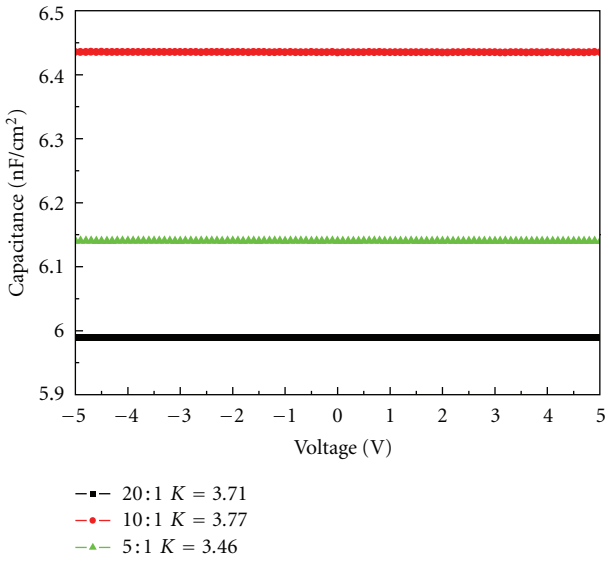

Figure 3: C-V characteristics of Al/PVP/Au gate capacitors having different PVP layers with weigh ratios of 20 : 1, 10 : 1, and 5 : 1.

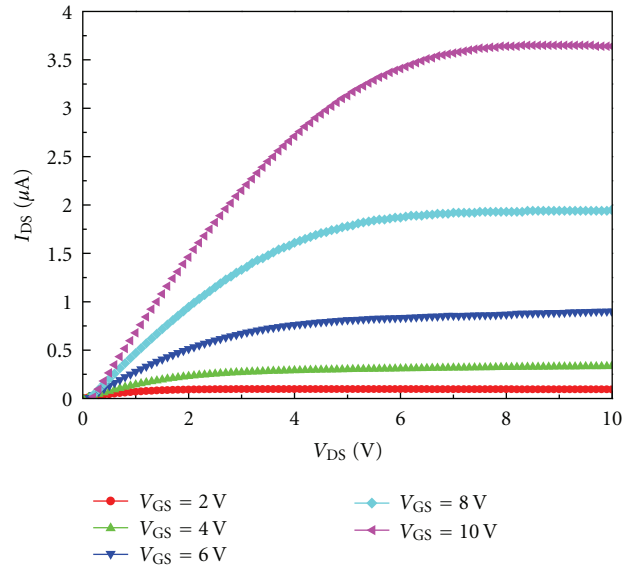

Figure 4: I_{DS}-V_{DS} characteristics of TFTs having dielectric layers with PVP : PMF ratios of 10 : 1.

weight ratios of 20 : 1, 10 : 1, and 5 : 1 produced measured capacitance densities of 5.9, 6.4, and 6.1 nF/cm^2, and k values of 3.71, 3.77, and 3.46 in the PVP : PMF dielectric layers, respectively.

The I-V characteristics of our devices were measured using a B1500 semiconductor parameter analyzer. Figure 4 shows the drain current (I_{DS}) versus drain voltage (V_{DS}) characteristics obtained for TFTs fabricated with PVP : PMF ratios of 10 : 1. The figure shows the typical output characteristics of transistors with clear pinch-off and current saturation and indicates that the saturation drain current, I_{DS}, is approximately 3.5 μA when V_{DS} = 10 V in this case with an applied gate bias, V_{GS}, of 10 V for transistors with PVP : PMF ratios of 10 : 1.

Figure 5 Transistor characteristics of polymeric dielectrics with various PVP : PMF ratios measured at a constant V_{DS} of 10 V. The values of μ_{FE} and V_T were determined from the linear $I_D{}^{1/2}$ versus V_G plot. The effective mobility, μ_{eff}, was estimated in the saturation regime as follows under the drain-source voltage of 10 V:

$$I_{D\,sat} = \left(\frac{WC_i\mu_{eff}}{2L}\right)(V_{GS} - V_t)^2, \quad (2)$$

where C_i is the gate dielectric capacitance per unit area of the gate dielectrics and W and L are the width and length of the channel, respectively. Once we obtained the values of W, L, and C_i, we could calculate the values of the field-effect mobility. SS is defined as the gate voltage required to increase the drain current by a factor of 10. From the transfer characteristics, we can also determine the gate voltage swing, SS, through the relation. SS is given by the following expression:

$$SS = \frac{\partial V_{GS}}{\partial \log(I_{DS})}. \quad (3)$$

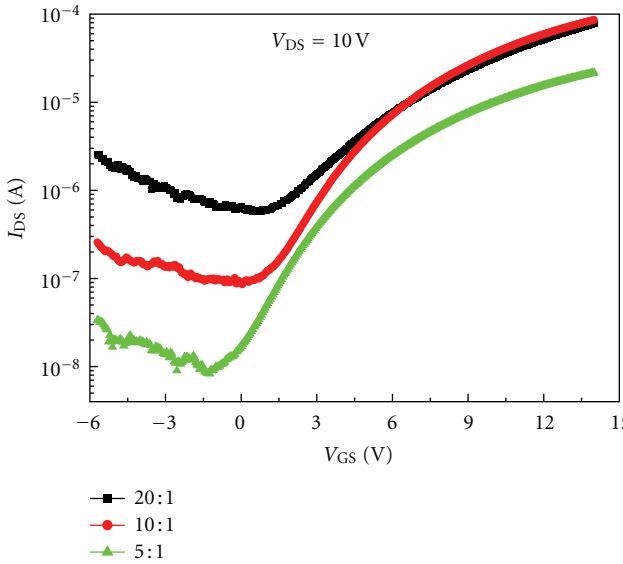

Figure 5: Transistor characteristics of polymeric dielectrics with various PVP : PMF ratios measured at a constant V_{DS} of 10 V.

It was found that the SS of our devices increases, but the mobility decreases, with a decrease in the PVP : PMF ratio.

This correspondingly increased the I_{off} current in transistor characteristics as exhibited in Figure 6. According to published current-voltage results the increase of hydroxyl groups in polymer dielectric causing large hysteresis affect and also deteriorated the gate leakage current.

Figure 7 shows the drain current (I_{DS}) versus gate voltage curves (V_{GS}) scanned from −6 to +14 V and then from +14 V to −6 V, which fixed V_{DS} at 10 V. The maximum difference of V_G for a constant current in the forward and reverse scans was designated as the amount of hysteresis (V_{hys}) described. ΔV_{hys} of the I-V curve is quite apparent,

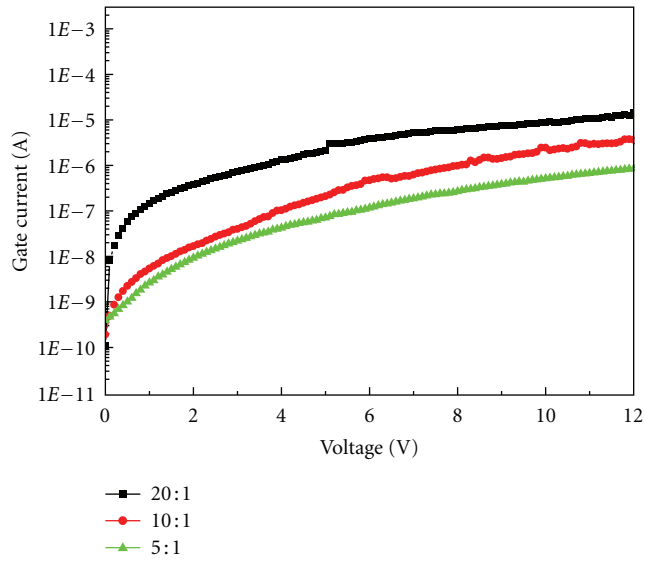

Figure 6: The gate leakage current characteristics of polymeric dielectrics with various PVP : PMF ratios.

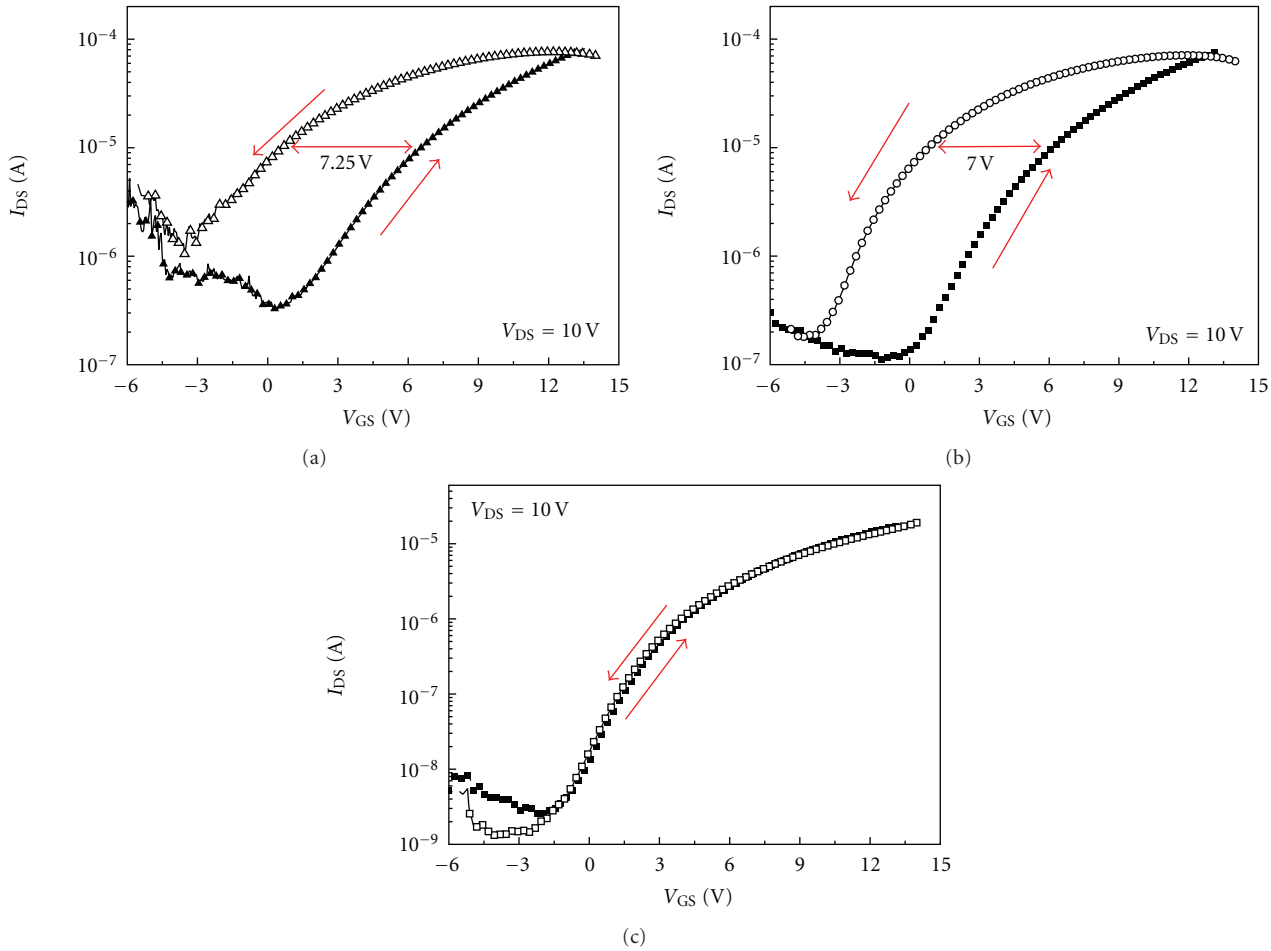

Figure 7: The drain current (I_{DS}) versus gate voltage curves (V_{GS}) scanned from −6 to +14 V and then from +14 V to −6 V, which fixed V_{DS} at 10 V with various PVP : PMF ratios PVP : PMF ratios of (a) 20 : 1, (b) 10 : 1, and (c) 5 : 1.

Table 1: Summary of SS, mobility, I_{ON}/I_{OFF} ratio, and V_T of a-IGZO TFTs with PVP dielectric layers.

Sample (PVP : PMF)	Dielectric constant	μ_{eff} (cm^2/Vs)	I_{ON}/I_{OFF}	SS (V/dec)	V_T (V)
20 : 1	3.71	36.6	8.2×10^2	2.72	3
10 : 1	3.77	42.4	1×10^3	2.71	4.1
5 : 1	3.46	9.53	2.4×10^3	3	3.4

being about 7.25 V with PVP : PMF of 20 : 1, while that with PVP : PMF of 10 : 1 is about 7 V. However, PVP : PMF of 5 : 1 is almost have no hysteresis voltage. Hysteresis is known to be caused by the impurities and trapped charges at the semiconductor/dielectric interface and/or those in the bulk of the dielectric and the inherent properties of the dielectric [20]. The results indicate that the reduction of the hydroxyl group in PVP might be a useful solution to the hysteresis problem.

The electronic properties of the three devices are listed in Table 1. The polymer dielectrics, with a low number of hydroxyl groups, exhibited very low carrier mobility as calculated in Table 1. The electronic mobility of IGZO very much depends on the number of hydroxyl group content in the dielectric films. Jang et al. reported that the traps originating from hydroxyl bonds mainly consist of bulk trapping sites rather than interface trap sites which predominantly affect the carrier mobility in the channel layer. However, PVP : PMF of 20 : 1 with higher field-effect mobility for insulators but some properties are not good enough to optimize condition. PVP : PMF of 10 : 1 with higher dielectric constant may be enhanced polarization, which increases the number of electronic-carriers at the insulator-semiconductor interface [13]. Therefore, one needs to understand the exact origin of the improvement of carrier mobility, and optimize the concentration profile of hydroxyl groups in polymer dielectric films, in order to improve the performance of a device.

4. Conclusion

In summary, we reported that a-IGZO TFTs having dielectric layers with different weight ratios (20 : 1, 10 : 1, and 5 : 1) of PVP and PMF, a cross-linking agent, have been fabricated. It was observed that by controlling the effect of the PVP : PMF weight ratio on dielectric and TFT characteristics were investigated. The a-IGZO TFTs with the PVP : PMF ratio of 20 : 1 showed a large hysteresis in the I-V curve and C-V curve, the hysteresis increase with the increase of hydroxyl groups and also deteriorated the gate leakage current.

According to our experimental results, preventing the possible diffusion of hydroxyl-contained species in polymer dielectrics is a very important factor in improving the electrical properties of high-performance a-IGZO TFT devices. As a result, we believe that a-IGZO TFTs with PVP dielectric layers can be widely used the application for nonvolatile memory devices.

Acknowledgments

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References

[1] H. Hosono, "Ionic amorphous oxide semiconductors: material design, carrier transport, and device application," *Journal of Non-Crystalline Solids*, vol. 352, no. 9–20, pp. 851–858, 2006.

[2] M. Nakata, K. Takechi, T. Eguchi, E. Tokumitsu, H. Yamaguchi, and S. Kaneko, "Flexible high-performance amorphous $InGaZnO_4$ thin-film transistors utilizing excimer laser annealing," *Japanese Journal of Applied Physics*, vol. 48, no. 8, pp. 0816071–0816077, 2009.

[3] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, "Temperature-dependent transfer characteristics of amorphous $InGaZnO_4$ thin-film transistors," *Japanese Journal of Applied Physics*, vol. 48, no. 1, Article ID 011301, 2009.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[5] J. B. Kim, C. Fuentes-Hernandez, and B. Kippelen, "High performance InGaZnO thin-film transistors with high-k amorphous $Ba_{0.5}$ $Sr_{0.5}$ TiO_3 gate insulator," *Applied Physics Letters*, vol. 94, no. 11, Article ID 119901, 2009.

[6] J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, X. H. Zhang, and B. Kippelen, "Low-voltage InGaZnO thin-film transistors with Al_2O_3 gate insulator grown by atomic layer deposition," *Applied Physics Letters*, vol. 94, no. 14, Article ID 142107, 2009.

[7] Y. J. Cho, J. H. Shin, S. M. Bobade, Y. B. Kim, and D. K. Choi, "Evaluation of Y_2O_3 gate insulators for a-IGZO thin film transistors," *Thin Solid Films*, vol. 517, no. 14, pp. 4115–4118, 2009.

[8] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, "High-mobility polymer gate dielectric pentacene thin film transistors," *Journal of Applied Physics*, vol. 92, no. 9, pp. 5259–5263, 2002.

[9] K. Lee, J. H. Kim, S. Im, C. S. Kim, and H. K. Baik, "Low-voltage-driven top-gate ZnO thin-film transistors with polymer/high-k oxide double-layer dielectric," *Applied Physics Letters*, vol. 89, no. 13, Article ID 133507, 2006.

[10] S. Bang, S. Lee, S. Jeon et al., "Al_2O_3 buffer in a ZnO thin film transistor with poly-4-vinylphenol dielectric," *Semiconductor Science and Technology*, vol. 24, no. 2, Article ID 025008, 2009.

[11] R. Parashkov, E. Becker, G. Ginev, T. Riedl, H. H. Johannes, and W. Kowalsky, "All-organic thin-film transistors made

of poly(3-butylthiophene) semiconducting and various polymeric insulating layers," *Journal of Applied Physics*, vol. 95, no. 3, pp. 1594–1596, 2004.

[12] S. Lee, B. Koo, J. Shin, E. Lee, H. Park, and H. Kim, "Effects of hydroxyl groups in polymeric dielectrics on organic transistor performance," *Applied Physics Letters*, vol. 88, no. 16, Article ID 162109, 2006.

[13] Y. Jang, D. H. Kim, Y. D. Park, J. H. Cho, M. Hwang, and K. Cho, "Influence of the dielectric constant of a polyvinyl phenol insulator on the field-effect mobility of a pentacene-based thin-film transistor," *Applied Physics Letters*, vol. 87, no. 15, Article ID 152105, pp. 1–3, 2005.

[14] D. Knipp, R. A. Street, A. Völkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: morphology, structural properties, and electronic transport," *Journal of Applied Physics*, vol. 93, no. 1, pp. 347–355, 2003.

[15] S. Steudel, S. D. Vusser, S. De Jonge et al., "Influence of the dielectric roughness on the performance of pentacene transistors," *Applied Physics Letters*, vol. 85, no. 19, pp. 4400–4402, 2004.

[16] T. Khan, D. Vasileska, and T. J. Thornton, "Effect of interface roughness on silicon-on-insulator-metal-semiconductor field-effect transistor mobility and the device low-power high-frequency operation," *Journal of Vacuum Science and Technology B*, vol. 23, no. 4, pp. 1782–1784, 2005.

[17] A. R. Völkel, R. A. Street, and D. Knipp, "Carrier transport and density of state distributions in pentacene transistors," *Physical Review B*, vol. 66, no. 19, Article ID 195336, 2002.

[18] G. Gu, M. G. Kane, J. E. Doty, and A. H. Firester, "Electron traps and hysteresis in pentacene-based organic thin-film transistors," *Applied Physics Letters*, vol. 87, no. 24, Article ID 243512, 2005.

[19] N. Arora, *MOSFET Models for VLSI Circuit Simulation Theory and Practice*, chapter 4, Springer, New York, NY, USA, 1993.

[20] D. K. Schroder, *Semiconductor Material and Device Characterization*, chapter 6, Wiley, New York, NY, USA, 2nd edition, 1998.