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Research Article

Improving the RF Performance of Carbon Nanotube Field Effect Transistor

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Compact model of single-walled semiconducting carbon nanotube field-effect transistors (CNTFETs) implementing the calculation of energy conduction subband minima under VHDLAMS simulator is used to explore the high-frequency performance potential of CNTFET. The cutoff frequency expected for a MOSFET-like CNTFET is well below the performance limit, due to the large parasitic capacitance between electrodes. We show that using an array of parallel nanotubes as the transistor channel combined in a finger geometry to produce a single transistor significantly reduces the parasitic capacitance per tube and, thereby, improves high-frequency performance.

1. Introduction

Carbon nanotubes belong to the fullerenes family and are sheets of graphite rolled in the shape of a tube. Depending on the direction in which the nanotubes are rolled (chirality), they can be either metallic or semiconducting [1]. Semiconducting nanotubes have been used in high-performance transistors where the channel is the nanotube itself. Since the first demonstration of carbon nanotube field-effect transistors (CNTFETs) in 1998 [2, 3], there has been an immense research concerning the electrical properties and the physical understanding of CNTFET [1, 4, 5]. The manufacturing of CNTFET processes progress continually: one of the most advanced is the chemical vapor deposition technique (CVD). The CNTFET can be characterized by high carrier mobility, low leakage current, important on state current relatively to the applied voltages, and low inverse subthreshold slope. These properties allow us to consider the design of high-speed and high-performance electronic circuits. High-performance CNTFET operating close to the ballistic limit has been reported in [6–8]. However, due to the large size of the probe pads relative to the CNT device, the parasitic capacitance of the pads can dominate the measured frequency response and inhibit measurement of the intrinsic response of CNT transistors. Moreover, the low current drive and high-input/output impedance of single CNTFET make it difficult to perform direct measurements of high-frequency electrical properties using instrumentation based on a reference impedance of 50 Ω. In order to make a direct measurement of a recognized high-frequency figure of merit, such as f_T small signal S-parameter measurements were achieved by a newly developed multiple-channel CNTFET structure whose output impedance is much lower than the usual single-channel CNTFET and a deembedding scheme that removes existing errors in measured S-parameters [9]. The authors of [9] measure $f_T = 10.3$ GHz after de-embedding. More recently, using one individual 100 μm long single-walled carbon nanotube, 100 individual nanotube top-gated field effect transistors are combined in a finger geometry to produce a single transistor with a cutoff frequency (after deembedding parasitic capacitance of the finger structure) of 7.6 GHz; before deembedding the cutoff frequency is 0.2 GHz [10].

In this work, we use compact model, in a quasi-static approach simulations to examine the high-frequency performance potential for a state-of-the-art CNTFET. Using an array of parallel nanotubes as the transistor channel combined in a finger geometry to produce a single transistor significantly reduces the parasitic capacitance per tube and, thereby, improves high-frequency performance. The results presented here should prove useful for understanding and

optimizing high-frequency characteristics of CNTFET and assessing the potential of CNTFET for nanoelectronic RF applications.

This paper is organized as follows. In Section 2, the compact model is presented. In Section 3, the results of our model using VHDL-AMS simulator in the quasistatic approach are shown and discussed. In Section 4 a new architecture is proposed and the results of the proposed architecture are presented. The conclusions are summarized in Section 5.

2. Approach

A simple model for ballistic nanotransitors is described in [11, 12]. For details about this model, we refer the reader to [13–15]. In this model, the gate voltage V_{gs} induces charge in the CNTFET channel Q_{cnt}. It also modulates the top of the energy band between the source and the drain by an amount V_{cnt}. As the source-drain barrier is lowered, current flows between the source and the drain. The electrons coming from the source fill $+k$ states and the electrons coming from the drain fill up the $-k$ states. The control potential V_{cnt} is computed self consistently using

$$V_{cnt} = \frac{LC_I V_{gi} + C_{SE} V_{si} + C_{DE} V_{di} - Q_{cnt}}{LC_I + C_{DE} + C_{SE}}, \tag{1}$$

where V_{gi}, V_{si}, and V_{di} are the intrinsic gate, source, and drain potential respectively. C_{SE}, and C_{DE} are the contact capacitance of the source and drain, C_I, is the gate oxide capacitance (see Table 1), Q_{cnt} depends on the number of carriers in the channel n_{cnt} which is the sum of the energy subband contributions, and L is the nanotube length. The drain current equation is derived from the Landauer formula which describes ballistic transport with ideal contacts:

$$I = \frac{4ek_BT}{h} \sum_p \left[\ln\left(1 + \exp\frac{-V_{si} - \Delta_p + V_{cnt}}{k_BT}\right) - \ln\left(1 + \exp\frac{-V_{di} - \Delta_p + V_{cnt}}{k_BT}\right)\right], \tag{2}$$

where Δp is the minima of the pth energy subband. The subbands minima can be calculated using zone folding method of the graphene electron dispersion:

$$\epsilon_\nu(\mathbf{k}) = \epsilon_{graphene}\left(|\mathbf{k}|\frac{\mathbf{K_2}}{|\mathbf{K_2}|} + \nu\mathbf{K_1}\right) \tag{3}$$

with

$$\nu = -\left(\frac{N}{2} + 1\right), \ldots, \frac{N}{2}, \quad -\frac{\pi}{|\mathbf{T}|} < |\mathbf{k}| < \frac{\pi}{|\mathbf{T}|}, \tag{4}$$

where $|\mathbf{T}|$ is the unit vector for the carbon nanotube (CNT), N is the number of hexagons in CNT unit cell, and $\mathbf{K_1}$ and $\mathbf{K_2}$ define the CNT reciprocal unit cell [16].

Table 1: CNTFET parameters (see text for discussion about the used values of the parameters).

Parameter	Name	Value	Unit
n	Helicity parameter	19	
m	Helicity parameter	0	
d	Diameter	1.49×10^{-9}	m
T	Temperature	300	K
R_d	Drain contact resistance	17×10^3	Ω
R_s	Source contact resistance	23×10^3	Ω
R_g	Gate contact resistance	10	Ω
L	Nanotube length	100×10^{-9}	m
V_{FB}	Flat band potential	-40×10^{-3}	V
C_I	Gate oxide capacitance	100×10^{-12}	F/m
C_{DE}	Drain capacitance	0.1×10^{-18}	F
C_{SE}	Source capacitance	0.1×10^{-18}	F

3. Quasistatic Approach and Results of Simulation

In the quasistatic approach to transistor modeling, dynamic behavior is predicted by employing static equations for charge (or carrier density) and transport current, but with static voltages replaced by their time-dependent counterparts:

$$\begin{aligned} Q(V_G, V_D, V_S) &\longrightarrow Q(V_G(t), V_D(t), V_S)(t), \\ I(V_G, V_D, V_S) &\longrightarrow I(V_G(t), V_D(t), V_S)(t), \end{aligned} \tag{5}$$

where Q is charge, I is current, t is time, and V_G, V_D, and V_S are the gate, drain, and source voltages, respectively. Employing the model presented in the last section with the quasistatic assumption, one can determine the ac behavior of CNTFET. The standard procedure is to assume sinusoidal excitation, write each time-dependent quantity in (5) in terms of static (dc or bias) and dynamic (ac, or small-signal) parts, for example, $V(t) = V_c + V_a \exp(jwt)$ where V_c refers to the dc value and V_a refers to the complex ac amplitude, and then make simulation to solve the equations for the ac terminal currents in terms of the ac terminal voltages.

3.1. VHDL-AMS Implementation. The MOSFET-like CNTFET compact model introduced in last section using the quasistatic approach is implemented with VHDL-AMS simulation tool. The main quantities used in the model are the control potential V_{cnt}, the subbands energy level Δp, and the source (drain) Fermi level $\mu_{S(D)}$. A maximum of 12 intrinsic parameters are necessary as input of this model: the chirality vector (n, m), the diameter, the flatband voltage V_{FB}, the contact resistances (R_s, R_d, R_g), the contact drain (source) capacitance C_{DE} (C_{SE}), and the gate oxide capacitance per unit length C_I. (The values of the parameters shown in Table 1 are estimated under the assumption that the compact model results for I-V characteristics should be compatible with the results of the model based on Boltzmann transport equation.) The value of C_I can be calculated from, $C_I = 2\pi\epsilon_0\epsilon_{ox}/((2h + d)/d)$, for a nanotube surrounded by

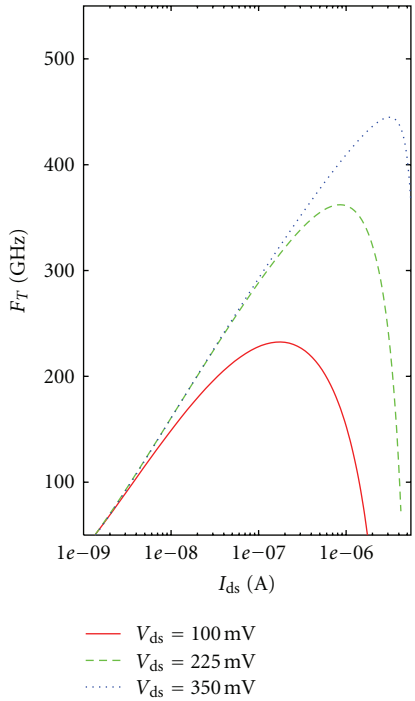

Figure 1: Intrinsic f_T as function of I_{ds} for V_{ds} = 100 mV (solid line), V_{ds} = 225 mV (dotted line), and V_{ds} = 350 mV (dashed line).

a coaxial gate, both separated by an oxide of thickness h with permittivity ϵ_{ox}. The device parameters used in the simulation for the I-V characteristics are summarized in Table 1. In Figure 1, we show the results of simulation based on our model for the intrinsic F_T as function of I_{ds} for V_{ds} = 100 mV (solid line), V_{ds} = 225 mV (dotted line), and V_{ds} = 350 mV (dashed line). The variation of F_T with I_{ds}, which is apparent in Figure 1, can be divided into three regions. region I is the low current region where F_T decreases as I_{ds} decreases, region II is midcurrent region where F_T is approximately constant, and region III is the high-current region where F_T decreases as I_{ds} increases. The reasons for this behavior of F_T with I_{ds} can be appreciated by plotting I_{ds} as function of V_{gs} at constant V_{ds} where $g_m = \partial I_{ds}/\partial V_{gs}|_{V_{ds}}$ is zero in the high-current region. The results of the simulation are very promising: the maximum obtained value of $f_T \sim 450$ GHz. However, if the extrinsic parasitic capacitance was included the RF performance of the carbon nanotube transistor will be reduced significantly. This will be our goal in the next section where we propose a new architecture to improve the performance of the CNTFET in the RF regime.

4. Multifinger Multitube Field-Effect Transistors

In this section, a new architecture "multifinger multitube field-effect transistor" (MMFET) is proposed that expected to increase the performance of the nanotube in high-frequency applications [10]. In the proposed architecture, using an array of parallel nanotubes as the transistor channel

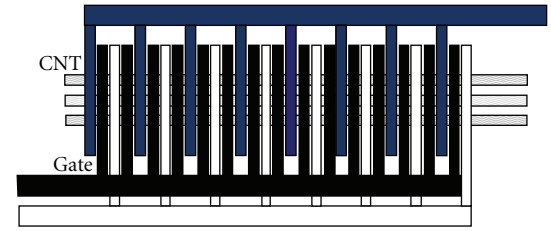

Figure 2: Schematic indication of MMFET device geometry (not to scale). In total, there are 16 tubes and 25 fingers (gates) in our design.

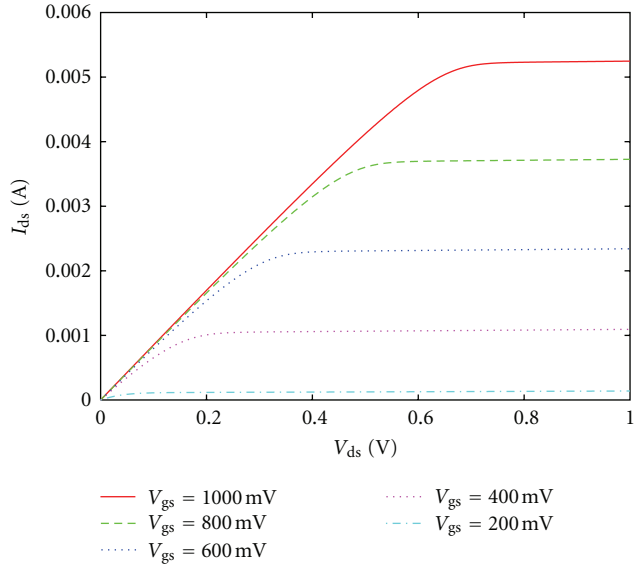

Figure 3: I_{ds}-V_{ds} for the (19,0) CNTFET (color online).

combined in a finger geometry to produce a single transistor significantly reduces the parasitic capacitance per tube and, thereby, improves high-frequency performance. Shown in Figure 2 a schematic indication of the MMFET geometry (not to scale). In total, there are 16 tubes and 25 fingers (gate) in our design. The distance between two nanotubes is taken to be $2d$ [17]. In the next two subsection we will study the DC performance and dispersion of this new architecture, and in the last two subsections, we will study the RF performance and applications of such architecture in RF circuits like ring oscillator.

4.1. DC Performance of MMFET. Figure 3 shows the simulated I_{ds}-V_{ds} characteristic for constant V_{gs} (see figure) at room temperature of our device. The device parameters used in the simulation are summarized in Table 1. The simulation has taken into account the series resistances. As one can expect, the current found for MMFET is 400× the single CNTFET current for the same characteristics.

4.2. Dispersion. Many physical parameters values vary in a wide range when nanotubes are manufactured. The most important impact is due to diameter dispersion. Here we will study the impact of the dispersion on the obtained diameters

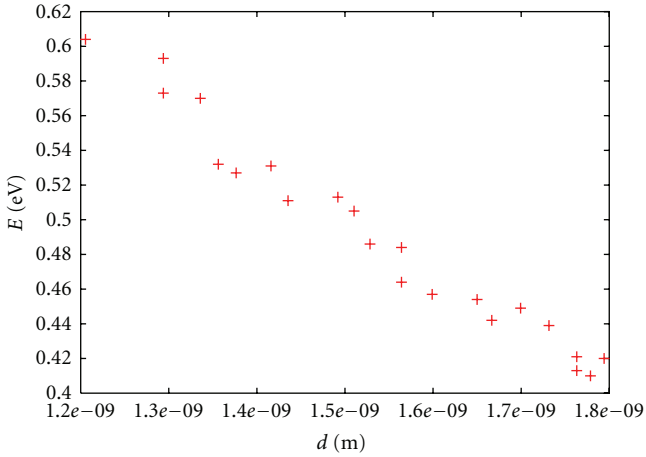

FIGURE 4: Minimum of the nanotube energy subband versus tube diameter.

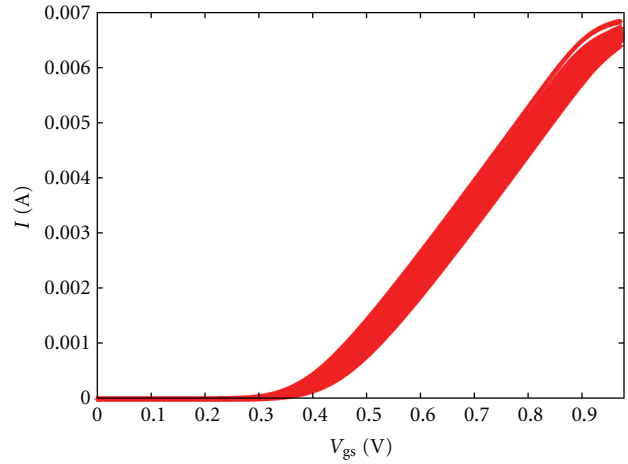

FIGURE 5: Impact of the diameter dispersion on the I_{ds}-V_{gs} characteristic at $V_{ds} = 800$ mV.

based on chirality vectors. The simulation is done using the following steps.

(1) Find all chirality vectors (m, n) which produce a diameter between 1.2 nm and 1.8 nm.

(2) Eliminate those vectors that give a metallic nanotube. 22 chirality vectors are found after elimination.

(3) Generate a uniform random number to pick up 16 chirality vectors out of the 22 chirality vectors. (Note that, the 16 chirality vectors correspond to the 16 nanotubes used in our simulation in the new architecture.)

(4) Generate another uniform random numbers for each trial.

In Figure 4, we show the minimum sub-band energy of the nanotube versus tube diameter for each chirality vector. The impact of the diameter dispersion on the I_{ds}-V_{gs} characteristic at $V_{ds} = 800$ mV is shown in Figure 5. According to the results shown in Figure 5, we can conclude that the I_{on}/I_{off} ratio is very sensitive to diameter spreading. To see the distribution of I_{ds} for fixed $V_{ds} = 0.8$ V, we show the current versus number of events that fall within I_{ds} and $I_{ds} \pm \Delta I_{ds}$ with $\Delta I_{ds} = 0.2$ mA. This distribution, as one can expect, can be compared to gaussian distribution with, in this case, a mean value $I_{ds}^{mean} \sim 3.4$ mA and $\sigma \sim 0.21$ mA. Figure 6 shows the number of trial versus the current at $V_{ds} = 800$ mV.

4.3. RF Response with Parasitic Capacitance of MMFET. From Section 3 we conclude that intrinsic device delay metric of CNTFET has high performance. However, from a circuit/system perspective, a realistic scenario should incorporate all the necessary parasitics. For the sake of comparison, we have studied the MMFET device with same characteristics as Si MOSFETs of the 65 nm technology. The parasitic capacitance per nanotube C_{tube} (C_{tube} is the capacitance added when a one nanotube is added to our device) between the gate and the source (drain) electrode is computed using Fastcap [18]. The thickness of the Pd source (drain) film is

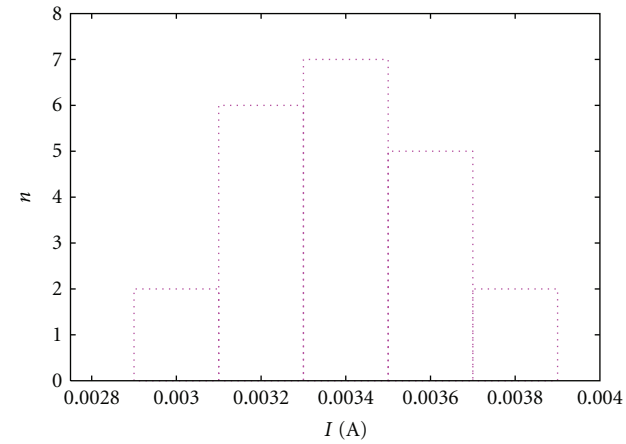

FIGURE 6: The number of trial versus the current at $V_{ds} = 800$ mV.

100 nm thick and 60 nm of length, the gate insulator Al_2O_3 thickness is 65 nm with dielectric constant ~9, and the Al gate is 150 nm thick and 140 nm length. It is assumed that each nanotube introduces a 4 nm width. Using Fastcap, with the geometries shown in Figure 7, we obtain $C_{tube} \sim 0.1$ fF. In Figure 10 we show the discretization used in Fastcap for the geometries that we proposed. (For the sake of clearness we give details on the simulation of the capacitor by Fastcap:

(i) we generate two cuboid with cubegen;

(ii) the generated objects are combined in a list were we define their position with respect to each other and the dielectric material;

(iii) we run Fastcap on the *l*st file with the option *l*. To produce a picture of the capacitor the *m* option should be used.)

In this simulation, we have used the measured parasitic capacitance for the multifinger device found in [10] as our

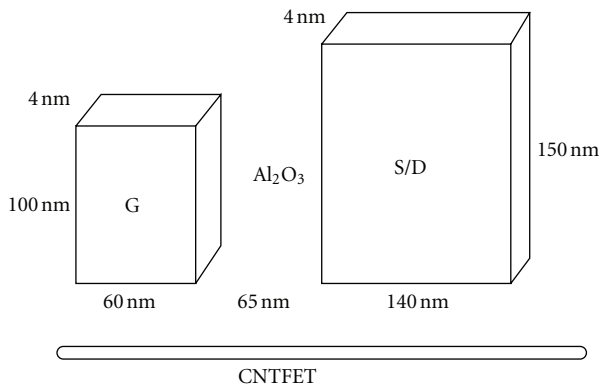

FIGURE 7: The used geometries for calculating the parasitic capacitance per nanotube C_{tube} in the MMFET.

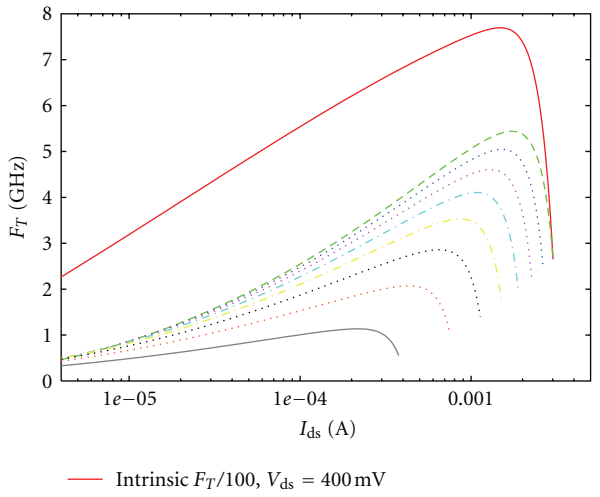

FIGURE 8: RF response with parasitic capacitance of MMFET at $V_{\text{ds}} = 400\,\text{mV}$: from top down the number of nanotube changes from 16 to 2 by step of 2. Intrinsic $F_T/100$ solid line. Same parameters as CMOS 65 nm technology are used (see text).

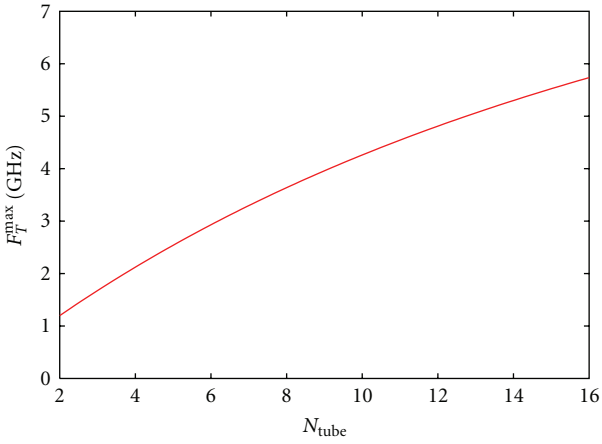

FIGURE 9: The maximum value of extrinsic F_T of the MMFET at $V_{\text{ds}} = 400\,\text{mV}$ versus number of nanotubes, n_{tube}.

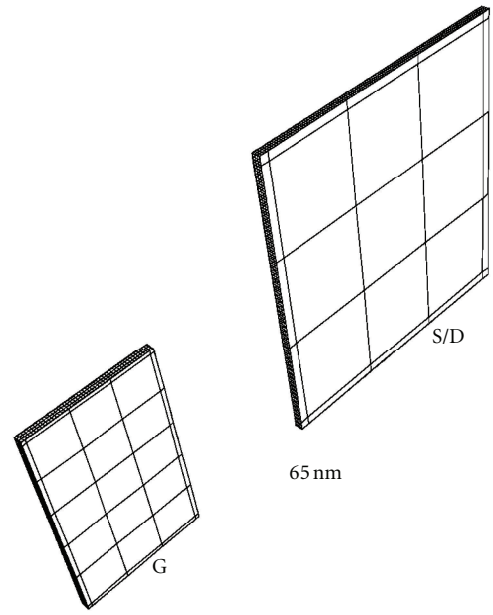

FIGURE 10: Discretization used in Fastcap.

initial value $C_{\text{exp}} \sim 50\,\text{fF}$, and for each nanotube we have introduced C_{tube} in such way:

$$C_{\text{total}} = C_{\text{exp}} + (N_{\text{tube}} - 1)N_{\text{finger}}C_{\text{tube}}, \tag{6}$$

where N_{tube} and N_{finger} are the number of tubes and fingers in the device, respectively. (With a new technology this value can be reduced significantly.)

In Figure 8, we show the results of simulation based on our model for the F_T as function of I_{ds} for $V_{\text{ds}} = 400\,\text{mV}$: the intrinsic $F_T/100$ (solid line), and from top down extrinsic MMFET where the number of nanotube change from 16 to 2 by step of 2. The device parameters used in this simulation are summarized in Table 2. As expected, the MMFET device that we propose improves the performance of the carbon nanotube in the RF regime where we found the maximum extrinsic $F_T^{\text{ex}} \sim 6\,\text{GHz}$ (see Figure 9) and the maximum intrinsic $F_T^{\text{in}} \sim 800\,\text{GHz}$ value that has to be compared to the maximal measured value $F_T^{\text{in}} \sim 10.2\,\text{GHz}$ [9].

4.4. Ring Oscillator with Carbon Nanotube. The parasitic capacitors play important role in the delay characteristics of a MMFET-based circuit. Simulations have been done with a three-stage ring oscillator (see Figures 11 and 12) and the effect of these parasitics has been studied. Figure 13 shows the effect on the natural oscillation frequency of parasitic capacitors with the parameters summarized in Table 2. (Of course the parasitic capacitance is not taken from Table 2.) It can be concluded from Figure 13 that in the range studied here, the parasitics dominate the performance. It should be noted, however, that the accurate estimation of the parasitics would be possible only when the layout geometry and a fabrication process of the MMFETs will be known. Further, it is worthwhile to mention that, for long channel MMFET under high bias, the effects of scattering with phonon are important and have to be considered.

Table 2: CNTFET parameters.

Parameter	Name	Value	Unit
n	Helicity parameter	19	
m	Helicity parameter	0	
d	Diameter	1.49×10^{-9}	m
T	Temperature	300	K
R_d	Drain contact resistance	17×10^3	Ω
R_s	Source contact resistance	23×10^3	Ω
R_g	Gate contact resistance	10	Ω
L	Nanotube length	8250×10^{-9}	m
V_{FB}	Flat band potential	-40×10^{-3}	V
C_I	Gate oxide capacitance	100×10^{-12}	F/m
C_{DE}	Drain capacitance	0.1×10^{-18}	F
C_{SE}	Source capacitance	0.1×10^{-18}	F
C_{GS}	Gate-source capacitance	87.5×10^{-15}	F
C_{GD}	Gate-drain capacitance	87.5×10^{-15}	F
n_{tube}	Number of tubes	16	—
n_{finger}	Number of finger	25	—

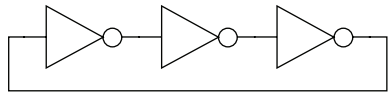

Figure 11: Three-stage ring oscillator.

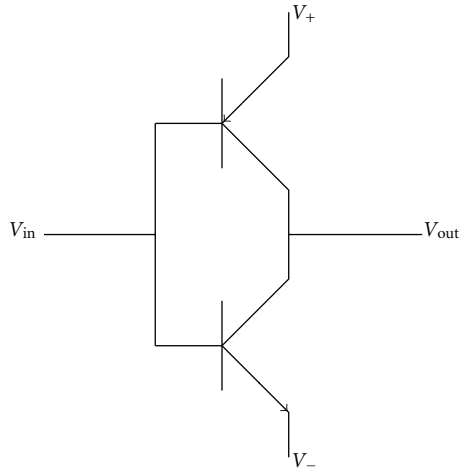

Figure 12: Schematic representation of a single inverter with $V_+ = 0.4$ V and $V_- = 0.4$ V.

5. Conclusions

This paper use circuit-compatible modeling technique for the ballistic CNTFET for applications to radio frequency circuits. Results of simulation for radio frequency circuits using VHDL-AMS simulator in the intrinsic case are presented. A new architecture was proposed to improve the performance of the CNTFET. We found that the extrinsic F_T and the natural oscillation frequency of a three-stage ring oscillator are ∼10 Ghz in the cases considered here. An experimental validation for the obtained results is necessary. From our analysis on the high-frequency performance of CNTFET, we conclude the following.

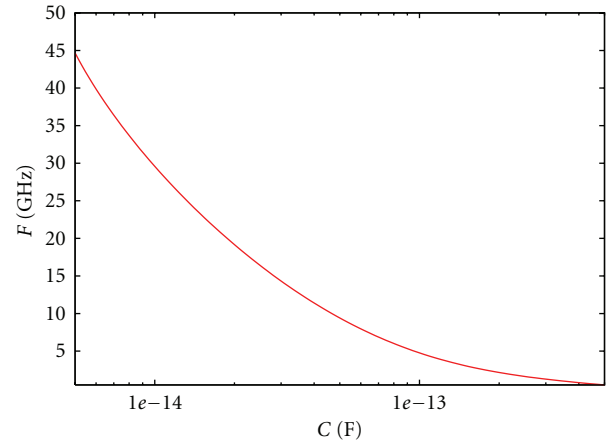

Figure 13: Natural oscillation frequency as function of C_{para} under ballistic transport.

(i) Classical lithography reproduces the same problem as CMOS. To overcome this problem we propose a metallic nanotube contacts.

(ii) Effect of phonon scattering can be important and have to be considered in the RF regime.

(iii) Non-quasistatic effects may not be very important.

We hope to address some of these issues in the near future.

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