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Review Article

Carbon Nanotubes for Thin Film Transistor: Fabrication, Properties, and Applications

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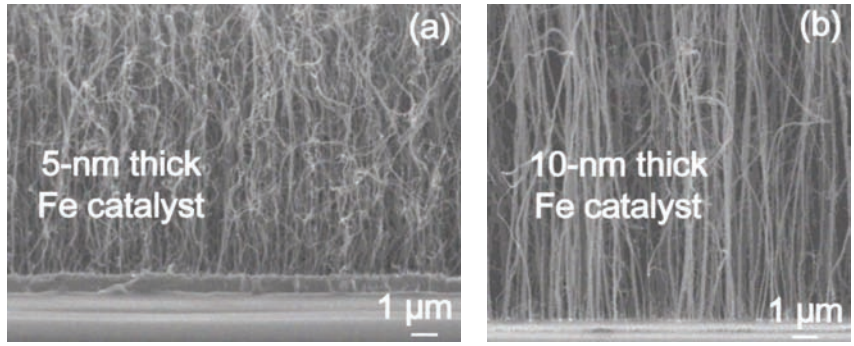
We review the present status of single-walled carbon nanotubes (SWCNTs) for their production and purification technologies, as well as the fabrication and properties of single-walled carbon nanotube thin film transistors (SWCNT-TFTs). The most popular SWCNT growth method is chemical vapor deposition (CVD), including plasma-enhanced chemical vapor deposition (PECVD), floating catalyst chemical vapor deposition (FCCVD), and thermal CVD. Carbon nanotubes (CNTs) used to fabricate thin film transistors are sorted by electrical breakdown, density gradient ultracentrifugation, or gel-based separation. The technologies of applying CNT random networks to work as the channels of SWCNT-TFTs are also reviewed. Excellent work from global researchers has been benchmarked and analyzed. The unique properties of SWCNT-TFTs have been reviewed. Besides, the promising applications of SWCNT-TFTs have been explored. Finally, the key issues to be solved in future have been summarized.

1. Introduction

Carbon nanotube (CNT) is considered as a cylinder formed by rolling a piece of graphene [1]. It has been studied for many aspects in recent years. Researchers have demonstrated that CNTs possess unique properties such as high current density exceeding 10^9 A/cm^2 [2], excellent thermal conductivity of about 6600 W/m·K [3], ballistic transport [4, 5], high mechanical flexibility with extremely high Young's modulus, about 1.2 TPa [6], and high photo transparency which can be higher than 90% [7, 8]. Because of these remarkable properties, CNTs, especially the single-walled carbon nanotubes (SWCNTs), have been expected to work as wiring and interconnect material, as well as alternative channel material for field effect transistors [9, 10]. They are the candidates for very large-scale integration circuits. Carbon-based nanoelectronics have been considered as the most promising emerging research device (ERD) technologies targeting for commercial demonstration in the 5–10-year horizon [9].

Thin film transistors (TFTs) are widely used for flat panel display, flexible electronics [11], and sensor applications [12]. The most common TFTs are using amorphous silicon (α-Si) or polysilicon as transistor channel [12]. Amorphous silicon TFTs can satisfy the requirements of large area, low-to-middle displaying speed [13], good uniformity, and fair stability. Poly-silicon TFTs own an advantage of high mobility. However, either of these two types of TFTs has its critical limitation so that neither of them can be widely applied in the more advanced displays. Amorphous silicon is sensitive to light. Also, the carrier mobility of the α-Si device is less than 2 cm^2/V·s [14], which cannot satisfy the requirement of the high-speed display with a frame rate of 120 Hz or higher [15]. Though poly-silicon TFT's mobility is large enough, it lacks flexibility and transparency, which is fatal for flexible devices. Metal oxide TFT is one of the innovations to meet the requirements of mobility and transparency simultaneously [16]. However, present metal oxide TFT is instable because it is sensitive to light, temperature, and water vapor. Also, it is instable and subjects to the negative bias illumination stress (NBIS) which can cause threshold voltage to shift to the negative voltage direction [17].

Single-walled carbon nanotubes possess high mobility, high transparency, and good flexibility simultaneously. These attractive properties satisfy the requirements of thin film transistors, making CNTs the most promising candidates as the high-performance TFT channel material. This research field has attracted much attention and intensive efforts since



(a) (b)

Figure 1: SEM images of the CNTs grown by thermal CVD. (a) and (b) show CNTs grown from different catalyst thickness. (a) 5 nm thick Fe catalyst thin film; (b) 10 nm thick Fe catalyst thin film [18].

2004. The number of published papers on carbon nanotube thin film transistors has increased year by year.

Here, we review the present status for the fabrication technologies and the applications of single-walled carbon nanotube thin film transistors. Their electrical properties, mechanical properties, and flexibility are studied. Their problems to be solved are also addressed.

2. SWCNT-TFT Fabrication

2.1. CNT Fabrication. Traditional processes to synthesize carbon nanotubes include arc discharge, laser ablation, and chemical vapor deposition (CVD). Among these methods, CVD is the most widely adopted due to its advantages of low cost, controllable synthesis, and high throughput. By controlling the parameters of catalyst, carbon source, gas pressure, and reaction temperature, researchers can control the location, the orientation, and the diameter of CNTs for the specific applications. CNTs were first discovered in arc-evaporation of fullerene in 1991 [1]. Laser ablation was used by Guo et al. to grow SWCNT in 1995 [19]. Arc discharge was first used to synthesize carbon nanotubes in large scale by Ebbesen and Ajayan in 1992 [20]. The laser and arc methods require very high temperature (1200°C or above) to fabricate CNTs, while the location and alignment of the CNTs are difficult to control.

Carbon nanotubes for thin film transistors are usually synthesized by thermal CVD or plasma-enhanced chemical vapor deposition (PECVD). Floating catalyst chemical vapor deposition (FCCVD) is also an alternative for CNT growth.

Thermal CVD is a traditional approach for CNT growth. Many groups have utilized the method in the experiments [10, 18, 21–23]. In thermal CVD, CNTs grew on Fe or its salt catalyst at temperature of 900°C or higher [10]. Huczko tried a low-temperature process ranging from 500 to 750°C [23]. The catalyst thickness is a key factor to determine the density and the diameter of the CNTs. Figure 1 shows a picture of the CNTs grown from different catalyst thickness. Thinner catalyst produces CNTs with smaller diameter and higher density.

PECVD has been used to synthesize CNTs since 1992 [24]. Li et al. obtained high ratio of semiconducting CNTs using this method [25]. Carbon nanotubes were grown on the SiO_2/Si wafer at 600°C in Ar, with monodispersed ferritin particles and Fe thin film as catalyst. The CNT diameters are from 0.8 nm to 1.5 nm with a mean of ~1.2 nm. One of the advantages for PECVD is that the products are mainly semiconducting nanotubes, with the ratio as high as 90%. The semiconducting CNT ratio is very critical for fabricating thin film transistors. Figure 2 shows that the as grown CNTs are high-quality single-walled nanotubes.

Liu et al. proposed to use FCCVD to fabricate CNTs [26]. They have demonstrated that it is possible to use FCCVD to grow high quality CNTs even at a low temperature. This method is cheap and it suits for mass production of CNTs with different diameters. Though the products in Liu's experiment are multiwalled carbon nanotubes, Moisala et al. demonstrated SWCNTs grown from ferrocene and carbon monoxide (CO) in the temperature ranging 891–928°C using FCCVD [27].

2.2. Metallic Semiconducting CNTs Separation. Metallic nanotubes and semiconducting nanotubes coexist in the synthesized carbon nanotubes all the time. This is a fatal obstacle impeding the development of SWCNT-based electronics because the metallic CNTs lack gate control and degrade the ON/OFF ratio of devices. Separating metallic and semiconducting nanotubes is a very critical technology, which also have attracted extensive research efforts. Different innovative approaches have been proposed to solve this problem, including electrical breakdown [28], density gradient ultracentrifugation [29], gel-based separation [30], dielectrophoresis [31], and DNA sequence separation [32]. Each of them has its advantages. For example, utilizing electrical breakdown to separate nanotubes does not need any extra-process step during the device fabrication. Using density gradient ultracentrifugation to separate CNTs can achieve 98% purity of semiconducting carbon nanotubes [33]. Here, we review several commonly used CNT purification methods.

2.2.1. Electrical Breakdown: VLSI-Compatible Metallic CNT Removal. Patil et al. proposed a method to separate metallic tubes from semiconducting ones, which is called VLSI-compatible Metallic CNT Removal (VMR). It is a process

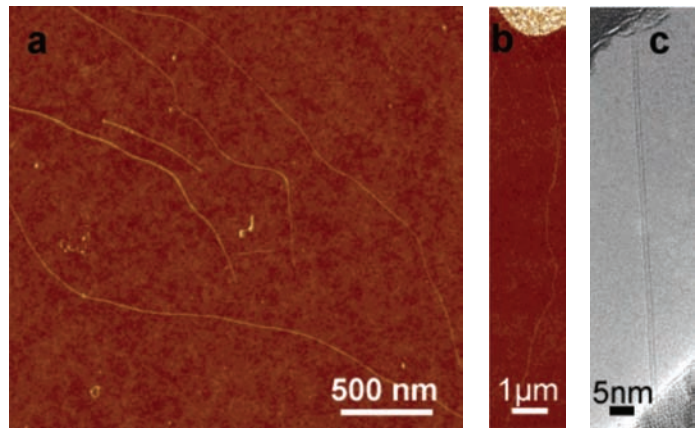


Figure 2: AFM and TEM views of SWCNTs grown by PECVD. (a) AFM image of nanotubes grown from low-density ferritin catalyst. (b) AFM image of a tube grown from a catalyst particle. (c) TEM image of an SWCNT with diameter of 1.2 nm [25].

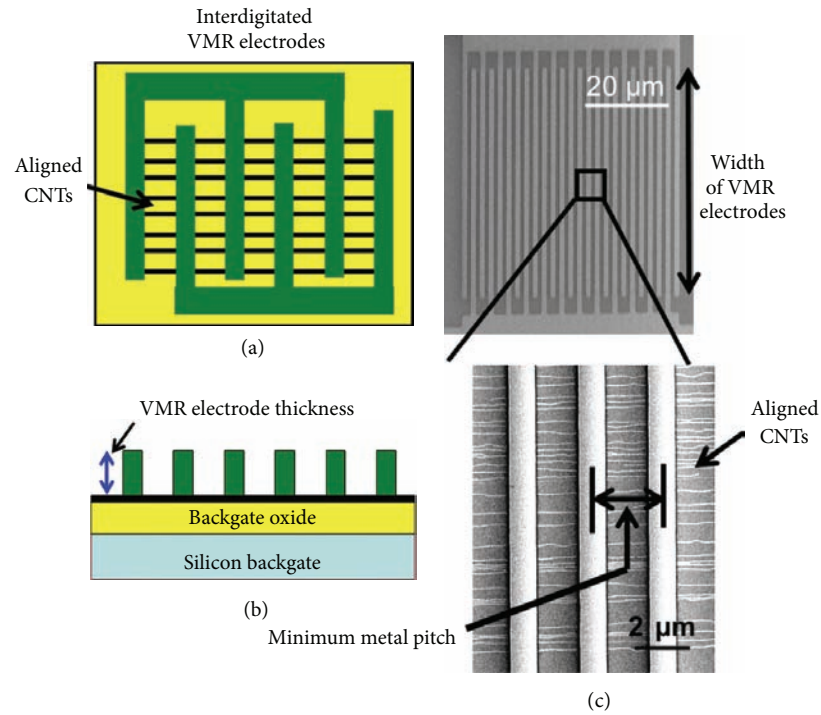


Figure 3: View of VLSI compatible Metallic CNT Removal (VMR) structure. (a) Top view. (b) Cross-sectional view. (c) SEM image (top view). The high voltage is applied to the interdigitated electrodes. The silicon backgate with an appropriate voltage turns off the semiconducting CNTs. Metallic CNTs between digitation will breakdown [28].

of using electrical field to break metallic nanotubes in a CNT integrated circuit. In their approach, an oxide layer of 100 nm worked as backgate oxide. Nanotubes were deposited on the oxide and then the interdigital VMR electrodes were fabricated on them to complete the structure, as shown in the Figure 3. Finally, a breakdown voltage was applied between the two electrodes and the backgate turns off the semiconducting CNTs. As a result, the metallic tubes were electrically removed at high electrical current [28].

2.2.2. Density Gradient Ultracentrifugation. Arnold et al. adopted an approach of density gradient ultracentrifugation, which is widely used in biochemistry, to separate two kinds of SWCNTs. The method is based on the differences in the buoyant densities of different SWCNTs to separate metallic and semiconducting nanotubes. In this method, carbon nanotubes with different diameters, bandgaps, and electronic types (metallic or semiconducting) were surrounded by surfactants. Nanotubes were spatially separated under the effect of centripetal force, as shown in Figure 4 [29].

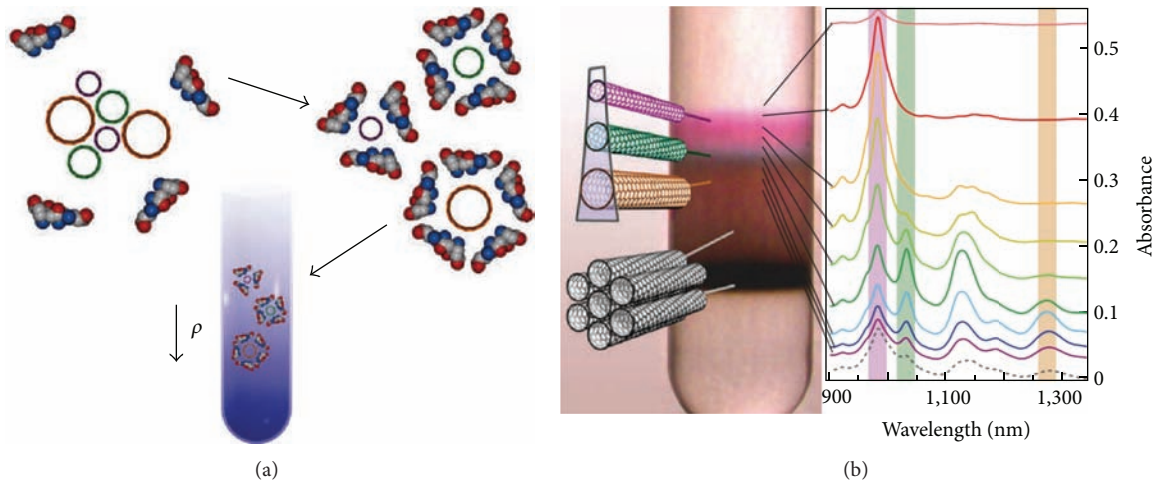


Figure 4: (a) Schematic of SWCNTs surrounded by surfactant and their sorting. (b) Picture of SWCNTs after separation and the optical absorbance spectra. SWCNTs were sorted evidently [29].

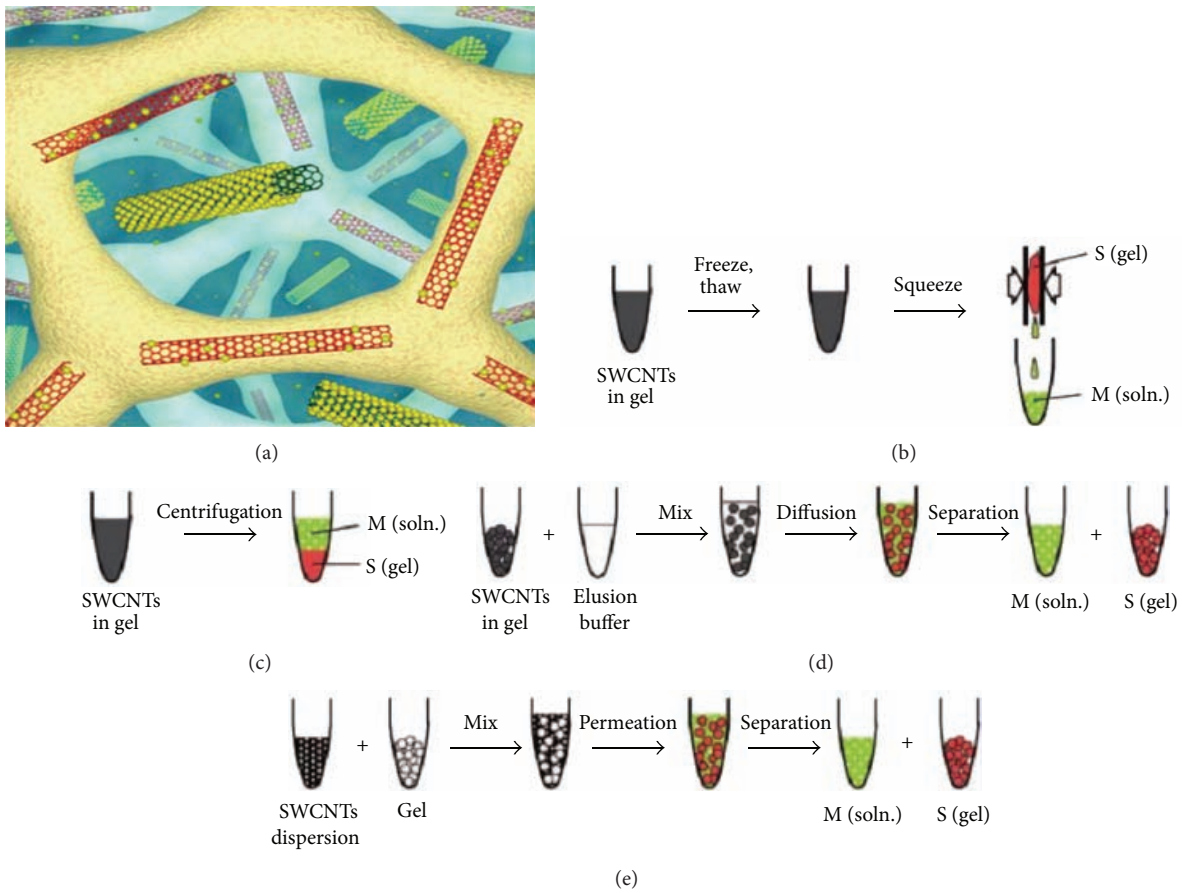
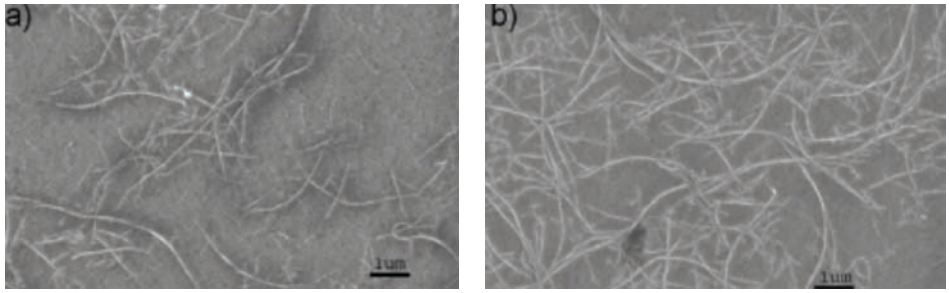


Figure 5: Schematic of gel separation. (a) Model of MS separation using agarose gel. Red, semiconducting SWCNTs; beige, agarose gel matrix; green, metallic SWCNTs; yellow, SDS. (b) Freeze and squeeze. (c) Centrifugation. (d) Diffusion. (e) Permeation [30].

2.2.3. Gel-Based Separation. Tanaka et al. discovered that metallic semiconducting (MS) separation occurred during electrophoresis of an SWCNT-containing agarose gel. SWCNTs were dispersed in sodium dodecyl sulfate (SDS) solution, and then agarose was added to form gel. The reason why using gel method can sort nanotubes is that the gel adsorbs semiconducting SWCNTs while the metallic ones are left in the solution. Figure 5 shows the steps of the gel separation [30].



(a) (b)

Figure 6: SEM images of the CNTs on alumina membrane. (a) and (b) show different density of the network [34].

Besides the main previous approaches, still other methods were also reported to sort nanotubes. For example, Liyanage et al. have reported a chirality-based sorting technique that relied on regioregular poly (3-dodecylthiophene) to aid the dispersion of semiconducting single-walled carbon nanotubes [35].

2.3. CNT Film Fabrication Process. After purification of CNTs, the semiconducting ones can be used to fabricate field effect transistors or thin film transistors. For thin film transistors, CNTs are used in form of CNT film, which is composed of random networks.

There are various methods to fabricate carbon nanotube random networks, including filtration [34], dip coating [36], transfer printing [37–39], ink-jet printing [40, 41], spray coating [42, 43] or spray deposition [44], and direct dry transfer [45]. These methods are mainly by means of transferring CNTs from one substrate to a target substrate. Most target substrates are polymers and therefore cannot sustain high temperature.

Each method has its specialty. Using filtration process can form uniform CNT films, and the films allow to be transferred to the other substrates. However, the process is relatively complicated. Dip coating, spray coating, and transfer printing are all low-temperature processes [36, 39, 42]. Okimoto et al. have fabricated devices by ink-jet printing with a temperature as low as 80°C [40]. Spray coating and dip coating are both simple fabrication processes. However, spray coating cannot be used for large area or mass production. Films fabricated by spray coating lack uniformity. Dip coating lacks controllability [34, 46]. Here, we review several main purification methods in detail.

2.3.1. Filtration. Hu et al. used a vacuum filtration method to produce uniform films of single-walled carbon nanotubes [34]. They dissolved the sonicated CNTs in the chloroform, obtaining a carbon nanotube suspension with a concentration of 0.2 mg/L. Then, the diluted CNT suspension was vacuum filtered over a porous alumina filtration membrane. After the filtration, nanotubes were trapped on the filtration membrane, forming an interconnected network [34], as shown in Figure 6.

2.3.2. Dip Coating. Dip coating is a conventional method to get thin film. Figure 7 is the process of dip coating and device fabrication by Xiong et al. [36]. They used modified parylene-C as adhesive layer on the silicon substrate and then defined microchannel by optical lithography. After that, the chip was dipped into the aqueous SWCNT solution which was terminated with carboxylic acid groups and pulled up slowly. The SWCNTs adhering to the surface of the parylene-C formed stripe structure, as shown in Figure 7. It has been demonstrated that SWCNT thin films formed by dip coating show good electrical and optical properties [46].

2.3.3. Ink-Jet Printing. Ink-jet printing was used to fabricate organic light-emitting diode (OLED) by Hebner et al. in 1998 [47]. After that, this technology has been widely used in electronic device fabrication. Ink-jet printing fabricates devices by a printer with objective material in it as ink. SWCNT printing uses SWCNT solution as ink and prints nanotube onto the substrate to form thin film channel. Other parts of the device can be fabricated by the standard fabrication processes like deposition, optical lithography, etch, liftoff, and so forth, or, as an alternative, they can also be fabricated directly by printing. Ink-jet printing results in little material waste and it is friendly to the environment. Therefore, it has the potential to reduce the ecological impact and energy consumption during manufacturing and also to reduce the costs in production [40]. Besides, it may be used in industrial scale production [48].

2.3.4. Transfer Printing. Transfer printing has been widely used to transfer CNTs grown by CVD at a high temperature on quartz or silicon substrate. In transfer printing process, the CNTs are adhered to some sacrificial layer, then transferred to an objective substrate, and the sacrificial layer is removed afterwards. Transfer printing technology is quite mature. Using transfer printing can form random CNT network or aligned CNTs. And another advantage of transfer printing is that it can be applied to nonplanar substrates [37].

Besides the previous methods, Ma et al. and Zhu and Wei have developed technologies to synthesize CNT films *in situ* using floating catalyst CVD growth [49, 50]. It is a direct and efficient method, but it requires a high temperature of at least 600°C. Therefore, it is not compatible to the standard flexible thin film transistor fabrication process, which can only sustain a low temperature because the substrates are usually glass or polymer.

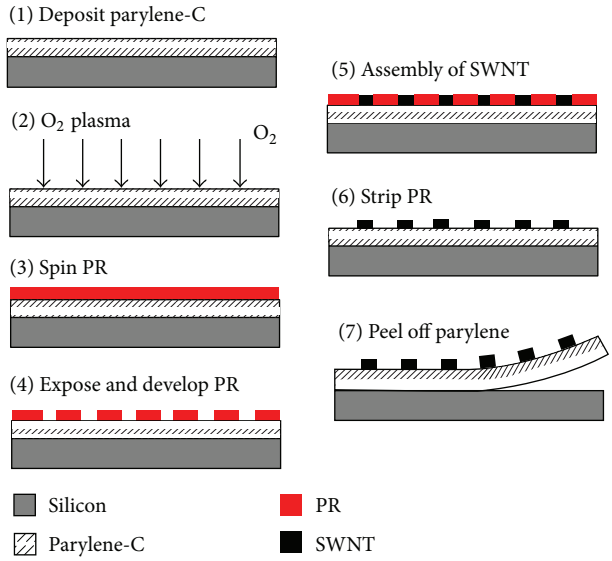


Figure 7: Schematic drawing of the direct patterning of SWCNTs onto a flexible substrate by Xiong et al [36]. The parylene-C film was disposed by O_2 plasma for 30 s to change hydrophobic surface into hydrophilic and defined microchannel by optical lithography. Then dipped the chip into aqueous SWCNT solution and pulled it up slowly with a speed of 0.1 mm/min. Photoresist was removed by acetone after completing dip coating. The flexible parylene-C SWCNT film could be peeled off from the substrate.

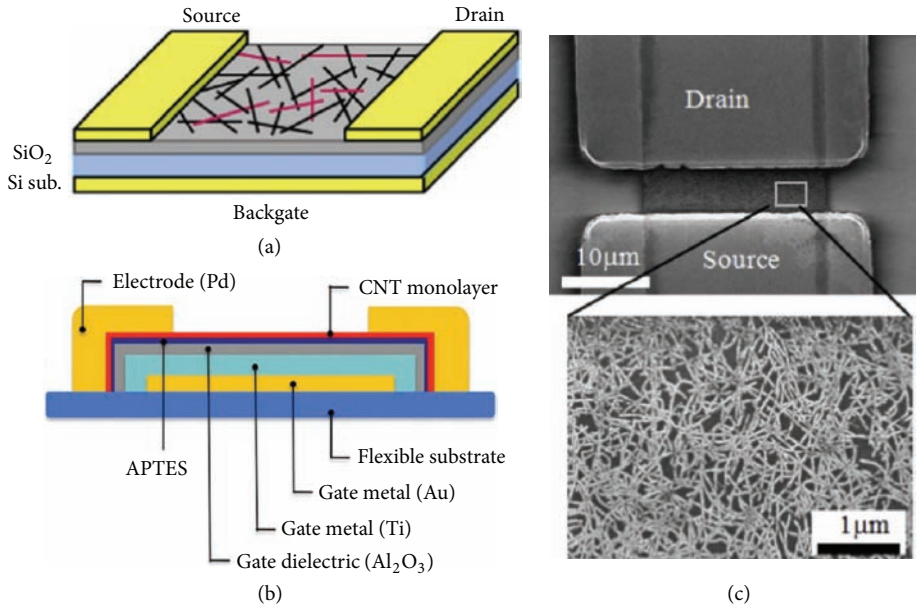


Figure 8: Typical structure of SWCNT-TFT. (a) Schematic diagram 1 [51]. This type of TFT is fabricated on silicon wafer. The silicon substrate works as the backgate and SiO_2 works as the gate dielectric. (b) Schematic diagram 2 [52]. The other type of TFT is fabricated on flexible substrate like polyamide. (c) SEM image of a TFT fabricated on silicon substrate with SWCNT network as its channel [51].

There is another form of SWCNT film besides the aforementioned. Liu et al. proposed a novel amorphous indium zinc oxide/ carbon nanotube (IZO/CNT) hybrid film to be used for thin film transistors [11]. The major difference between the aforementioned SWCNT network film and the hybrid film is that the former utilizes semiconducting CNTs to fabricate devices while the later uses metallic CNTs to provide a superior transporting channel. Experimental results show that IZO/CNT hybrid film possesses better electrical and mechanical performance.

2.4. SWCNT-TFT Structure and Fabrication. Figure 8 shows the typical structure of a single-walled carbon nanotube thin film transistor. The substrate is silicon wafer or flexible polymer. The channel is a network consisting of random CNTs.

In Figure 8(a), the device has silicon substrate as the backgate and SiO_2 as the gate dielectric. In Figure 8(b), the device uses polymer as substrate. The commonly used polymers are Polycarbonate (PC), Polyimide (PI), Polynaphthalene two formic acid glycol ester (PEN), and so forth.

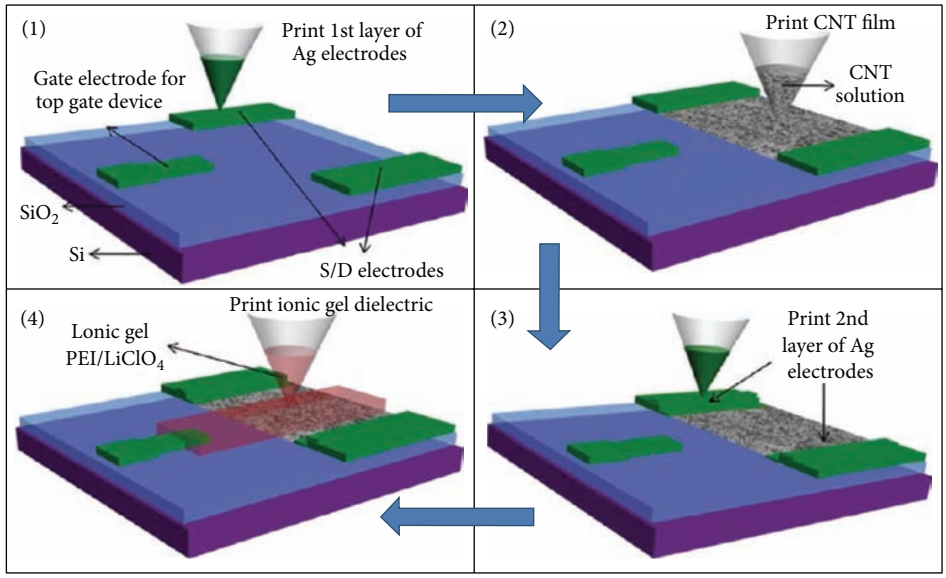


Figure 9: Schematic for fabrication process of a SWCNT-TFT by ink-jet printing [53]. The whole device was fabricated by printing. First, a layer of silver ink was printed on the substrate to form source and train electrode. The silver layer was sintered at a temperature of 180°C to obtain low resistance. Then SWCNT solution was used as ink to print the channel. After that, another layer of silver ink was printed to improve the contact between SWCNT and silver electrode. Finally, the gate dielectric and gate electrode were fabricated.

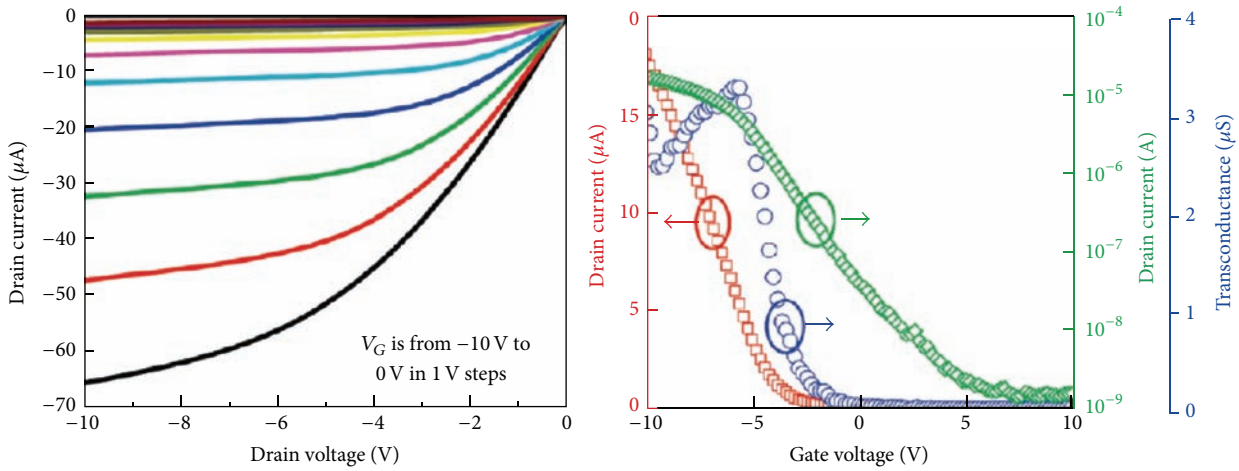


Figure 10: Drain current and transconductance versus voltage characteristics of SWCNT-TFTs [54].

For the polymer substrate device, at the beginning of the fabrication, the flexible substrate was affixed on a silicon wafer to keep the interface flat. Then, titanium (Ti) and Gold (Au) were defined on the substrate as backgate electrodes. A layer of aluminum oxide (Al_2O_3) with thickness ranging from 20 to 40 nm, sometimes with a thin layer of SiO_2, was formed over the gate electrodes using atomic layer deposition, serving as the gate dielectrics. To enhance the adhesion between SWCNTs and the dielectric layer, the wafer was immersed in the solution of 3-aminopropyltriethoxysilane (APTES) in deionized (DI) water for 30 min. After that, SWCNTs were transferred to the interface. The last step was forming source and drain electrodes by deposition of Ti/Palladium (Pd) [52].

We have introduced the ink-jet printing technique to produce CNT films previously. Another innovative process has been proposed to fabricate the whole device with ink-jet printing technology [40, 53]. As shown in Figure 9, the device, including source and drain electrodes, is completely fabricated by ink-jet printing.

3. Electronical, Optical, and Mechanical Properties

3.1. Electrical Properties of SWCNT-TFTs. The electrical properties of a SWCNT-TFT sample are shown in Figure 10. From the drain current-drain voltage curve, the transistor shows typical p-type characteristics.

There is a peak in the transconductance curve, and it suggests a near linear subthreshold slope. When drain voltage is small, the device shows a linear relationship between drain

Table 1: Benchmarking for properties of SWCNT-TFTs reported by different groups.

No.	L_{ch} (μm)	I_{on}/W (μA/μm)	μ (cm^2/V·s)	I_{on}/I_{off}	g_m/W (μS/μm)	Reference
1	10	15	50	3×10^3	4	[12]
2	4	10	52	$>1 \times 10^4$	0.033	[54]
3	100	0.01	35	6×10^6	—	[55]
4	50	0.356	67	482	0.046	[56]
5*	20	—	140	1×10^7	—	[11]
6#	0.12	125	—	—	40	[57]
7#	1	0.8	3500	$>1 \times 10^3$	~0.096	[58]
8#	50	0.6	1300	3×10^4	—	[59]

*Note: sample No. 5 is metallic SWCNT/IZO-TFT sample, while others are semiconducting SWCNT-TFTs; #Note: sample Nos. 6, 7, and 8 are aligned CNT channels, while others are random CNT network films.

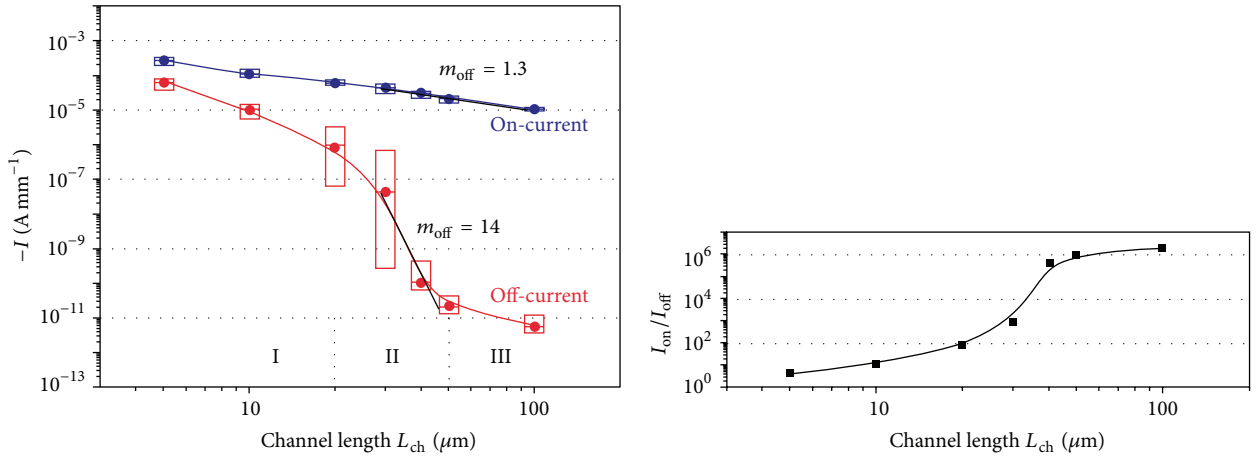


Figure 11: Plot of current and on /off ratio of SWCNT-TFT [55]. (a) On-current and Off-current versus channel length; (b) I_{on}/I_{off} ratio versus channel length.

current and voltage. With the increase of drain voltage, it shows semiconducting characteristics and acts as a p-type transistor. Drain current is influenced by channel length. With the increase of channel length, the on current decreases, as well as the off current. As shown in Figure 11(a). The current density changes as well with the change of channel length.

The current on/off ratio of the SWCNT-TFT device is closely related to the CNT purity. The existence of metallic CNTs provides a percolation path. The off current increases drastically and degrades the on/off ratio. The on/off ratio also depends on the channel length, shown in Figure 11(b) by Sun et al. [55]. The on/off ratio increases with channel length increase in most experiments, due to the presence of a small amount of metallic nanotubes in the channel [51]. The highest on/off ratio reported is 6×10^6 [55]. It is large enough to operate devices such as OLED.

The properties of SWCNT-TFTs reported by different research groups are benchmarked in Table 1. From the comparison, properties of the SWCNT-TFTs by different processes vary a lot from each other.

From Table 1, I_{on}/W of sample No. 6 can reach 125 μA/μm. The on/off ratio can be higher than 6×10^6. Mobility (μ) for aligned carbon nanotube thin film transistors (CNT-TFTs) can be as high as 3500 cm^2/V·s. The transconductance (g_m/W) can reach 40 μS/μm. The comparison in this table is relative because their I_{on}, g_m, and mobility were measured in different working voltage and different conditions. Different channel lengths also affect their measured electrical parameters.

In the random CNT network devices, the mobility can be calculated through the equation $\mu = g_m L_{ch}/C_{ox} V_{DS} W_{ch}$ [51, 52, 54] here C_{ox} is the channel capacitance of the random CNT networks. It can be calculated using the method of reference [54]. From Table 1, the highest mobility can be 67 cm^2/V·s [56]. Chandra et al. show that the mobility decreases as the channel length increases. The explanation for the result is that the device performance is dominated by the electron scattering in the channel region rather than at the metal nanotube contacts [52]. For transistors of similar channel length, using longer nanotubes would lead to less nanotube-nanotube junctions and consequently higher mobility [54]. The mobility is also related to the density of CNTs in the network. The mobility increases with increasing the density of CNTs.

For aligned SWCNT-TFTs, the mobility is extremely higher than that of the random CNT network TFTs. It is

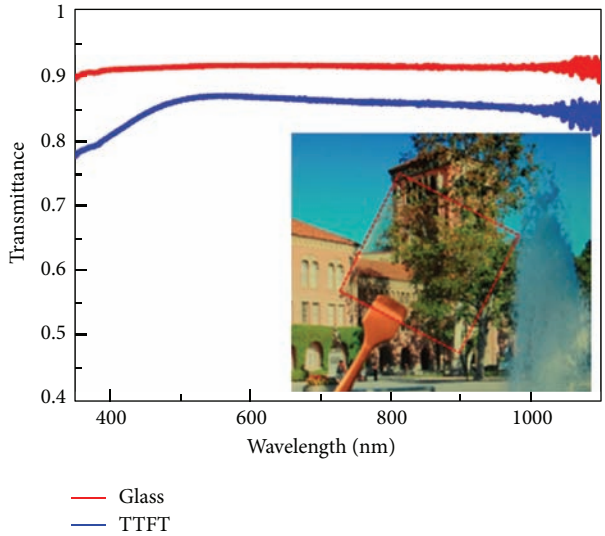


FIGURE 12: Transmittance curve of carbon nanotube thin film transistors. The red curve is the transmittance of the glass substrate; the blue curve is the transistors. Inset: the image of the devices on a 2 in. square glass substrate [60].

because the aligned CNTs drastically decrease the tube-to-tube junctions. The carriers can transport by ballistic in some degree. The existence of metallic CNTs increases the mobility too.

There is also a relationship between channel length L_{ch} and nanotube length L_{CNT}. When L_{CNT} is comparable to L_{ch}, or when density of the metallic nanotubes exceeds the percolation threshold $\rho_{th} = 4.24^2/\pi L_{CNT}^2$, the metallic nanotubes can connect the source and drain directly, resulting in a drastic increase in the device mobility, as well as both the on and the off current. Thus, there is a trade-off between mobility and the on/off ratio [55].

To describe the device performance, g_m is another important parameter. g_m/W is the normalized transconductance, which was reported as high as 4 μS/μm [12]. From Cao's recent work, the value can reach 40 μS/μm [57]. g_m/W is inversely proportional to channel length. It is similar to the device mobility.

From the benchmarking in Table 1, the CNT/IZO hybrid thin film transistors has much higher device mobility (140 cm^2/V·s) than that of CNT network TFTs [11], because the active CNTs in its channel are metallic nanotubes, which can provide a high-speed path. The on/off ratio of CNT/IZO hybrid thin film transistors can reach 1.3×10^7. In CNT/IZO hybrid thin film transistors, both on/off ratio and device mobility depend on CNT weight concentration. In the range of 0 wt% to 1 wt%, the on/off ratio increases as CNT weight concentration increases, as well as the mobility [11]. However, when the CNT weight concentration is larger than 2 wt%, the TFT cannot be switched off.

3.2. Optical Properties of SWCNT-TFTs. SWCNT-TFTs have a good performance on optical transmittance. Wu et al. have obtained 50 nm thick CNT thin films by filtration process, with transmittance greater than 70% over visible range and 90% in the near infrared at 2 μm wavelength [7]. Zhang et al. have fabricated carbon nanotube thin film transistor with high transparency of 82% in the visible range [60]. Figure 12 is the transmittance curve of the thin film transistor and the inset is image of the devices on a 2 in. square glass substrate.

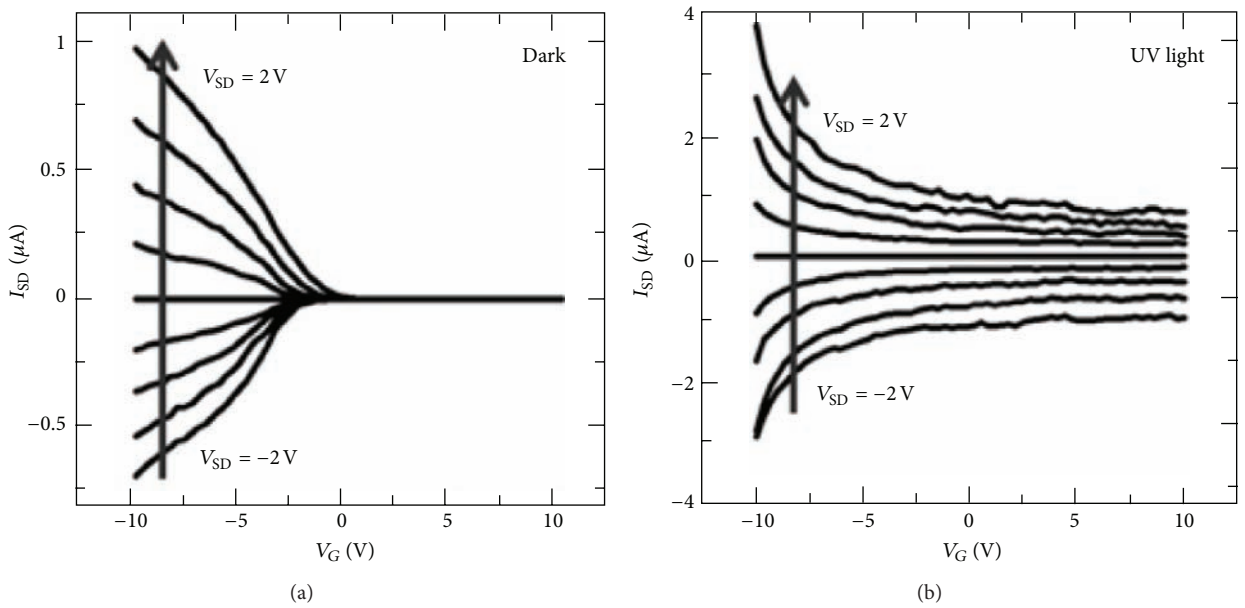
Besides high transparency, the SWCNT-TFTs have a high photosensitivity to the exposure of UV/visible light. In Park et al.'s research, they measured the photo response over visible and UV light [61]. Experimental results are shown in Figure 13. When the transistor was exposed to UV light, the drain current increased obviously due to the photo-induced charge carriers.

3.3. Mechanical Properties of SWCNT-TFTs. Carbon nanotubes have a good property of mechanical flexibility with extremely high Young's modulus of about 1.2 TPa. Many researchers have done bending test to demonstrate the high mechanical flexibility of carbon nanotube thin film transistors [12, 45, 52, 62]. The bending test shows that the thin film transistors perform well even after bending to a small radius. In Chandra et al.'s experiment, the on current remains nearly unchanged and shows reliability [52]. Chae et al. showed that their SWCNT/graphene thin film transistor remained in high performance after stretching and releasing it more than 1,000 times [63].

For CNT/IZO hybrid thin film transistors, the dynamic loading test shows that after the transistors were bended to a minimum radius of 700 μm, the devices remained in high performance and stability. The repeated bending test shows that after 300 cycles, the normalized resistance varied by less than 8% [11].

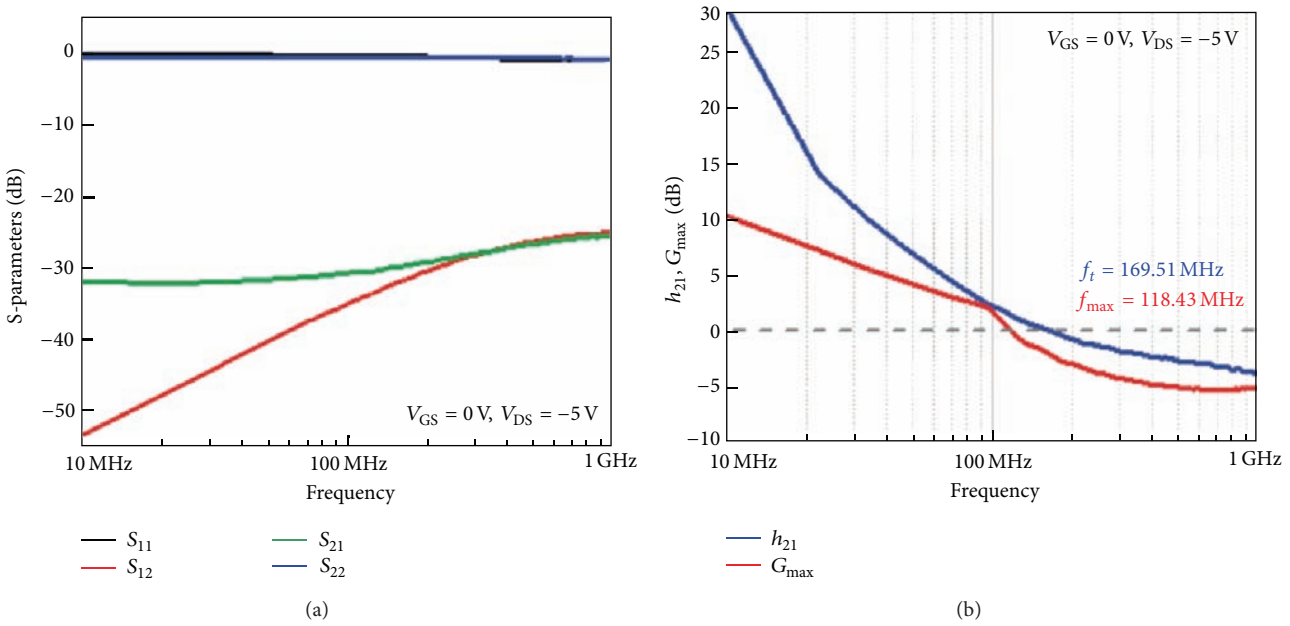
4. SWCNT-TFT for Promising Application

Single-walled carbon nanotubes are promising for a diverse range of applications including high-strength hybrid nanocomposites, growth platforms for neuronal circuits, highly sensitive chemical/biological sensors, electrode material for solar cells, and channel of active elements in electronic devices [64].



(a) (b)

FIGURE 13: Current-voltage curves of a transistor with drain voltage from −2 to 2 V. (a) without UV light irradiation; (b) with UV light irradiation [61].



(a) (b)

FIGURE 14: Carbon nanotube TFT's RF characteristic. (a) Measured S-parameters from 10 MHz to 1 GHz. The transistor is biased at V_{GS} = 0 V and V_{DS} = −5 V for optimal performance. (b) Intrinsic current gain h_{21}, and maximum available gain G_{max} derived from the S-parameters by Wang et al. [12].

SWCNT-TFTs have been a potential candidate for the future electrical and photonic applications, including integrated circuits, control circuits for liquid crystal display (LCD) and OLED displays, and flexible and transparent display. Because SWCNT-TFTs are sensitive to UV/visible light, they can be used as photo devices as well.

4.1. Integrated Circuits: Digital, Analog, Radio Frequency Applications. In the work of Wang et al. in the University of California, Berkeley [12], the SWCNT-TFT showed a cutoff frequency of 170 MHz, as shown in Figure 14, which can meet the requirements of certain wireless communication.

Zhang et al. measured the RF transmission properties of SWCNT in field effect transistors using S parameter and found the CNT transmission showed no degradation until 12 GHz [65]. The result indicates that there is further room for the cutoff frequency of SWCNT-TFT to improve.

Other researchers have used SWCNT-TFTs to fabricate integrated circuits successfully, such as digital logic gates,

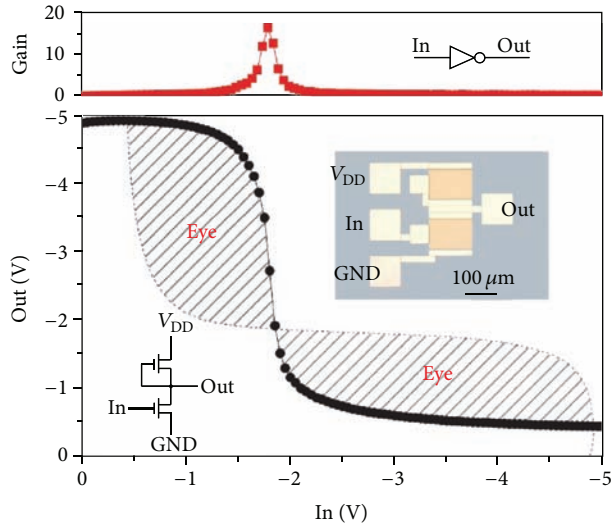


Figure 15: Inverter realized by SWCNT-TFTs and its transfer curve [55].

including inverter, NAND, and NOR gates [55]. Figure 15 shows the inverter circuit and its transfer characteristics.

4.2. OLED and Liquid Crystal Display (LCD) Control Circuits. Thin film transistors have been widely used in LCD and OLED displays. Nowadays, the popular TFT channel materials used in mass production are α-Si and poly-silicon. α-Si TFTs have been used in many display products. However, this kind of TFTs cannot meet the requirements of high-precision and high-frame rate for advanced LCD and OLED display circuits in the future. The three-dimensional (3D) displays appearing on the market require frame rates of 240 Hz [66]. Even higher frame rates, 480 Hz or above, are further required to improve the picture quality. To meet these requirements, SWCNT-TFT is a promising candidate with higher carrier mobility and on/off ratio.

Recently, a SWCNT-TFT driving OLED circuit has been proposed [54]. In this design, the SWCNT-TFT is connected to an OLED, and V_{DD} (<0 V) is applied to the cathode of the OLED, as shown in Figure 16. SWCNT-TFT's on/off ratio can meet the requirement of OLED switching. The output light intensity modulation is over 10^4.

4.3. Photonic Device. SWCNT-TFTs have a high sensitivity to light ranging from infrared to ultraviolet, so they are promising to be used as photo devices, such as photo detector and light-harvesting devices [56].

5. Summary and Outlook

Though lots of studies have been conducted for single-walled carbon nanotube thin film transistors, some issues remain to be solved before their practical applications in the near future. They are summarized as follows.

5.1. Alignment. The resistance of the contacts between tube and tube is high and varies with different contact situations. From Hu et al., the intertube contact resistance is as high as 100 MΩ, which is 4 orders of magnitude larger than the resistance of the tubes themselves, 10 kΩ [34]. So, it is important to reduce the tube-to-tube contacts. Using better aligned carbon nanotubes can solve the problem so as to reduce the contact resistance. Some researchers have achieved higher device mobility with aligned nanotube arrays [58, 59, 67]. Figure 17 is one of the device schematics [67]. CNTs were *in situ* grown on the quartz substrate at 900°C. From the picture, CNTs were aligned very well. Although the density is low (about 0.5 tubes/μm), devices fabricated by this method performed well, with effective mobility of ~3500 cm^2/V·s and on/off current ratio higher than 10^3. However, this *in situ* growth process was operated at a temperature of 900°C, which cannot fit for flexible TFT fabrication.

A preferable design has been proposed by Ishikawa et al. [58]. They used a transfer process to transfer aligned CNTs synthesized on quartz to a flexible substrate. They used Au as a sacrifice layer to transfer CNTs. The final CNTs on the flexible substrate reached a density of 2-3 tubes/μm. The mobility is 1300 cm^2/V·s and on/off ratio is 3×10^4. The CNT array density and alignment can be further improved. Ding et al. have obtained CNT density of higher than 50 tubes/μm [68], and Cao et al. have obtained more than 500 tubes/μm by using the Langmuir-Schaefer method in their recent work [57].

5.2. Metal Contact. The contacts between nanotubes and metal electrodes are not perfect ohmic contact. The widely used metals to contact CNTs include Ti, Pd, Au, and Pt. Their work functions are close to those of CNTs. Xu et al. have demonstrated that the contact between Pt and CNT films has the lowest resistance [69]. However, the barrier still exists. Chai et al. inserted graphitic interfacial layer between the metal and the CNT so as to reduce the contact resistance [70]. A new material/composite whose work function matches well with a nanotube is expected to avoid the Schottky barrier and to reduce the resistance.

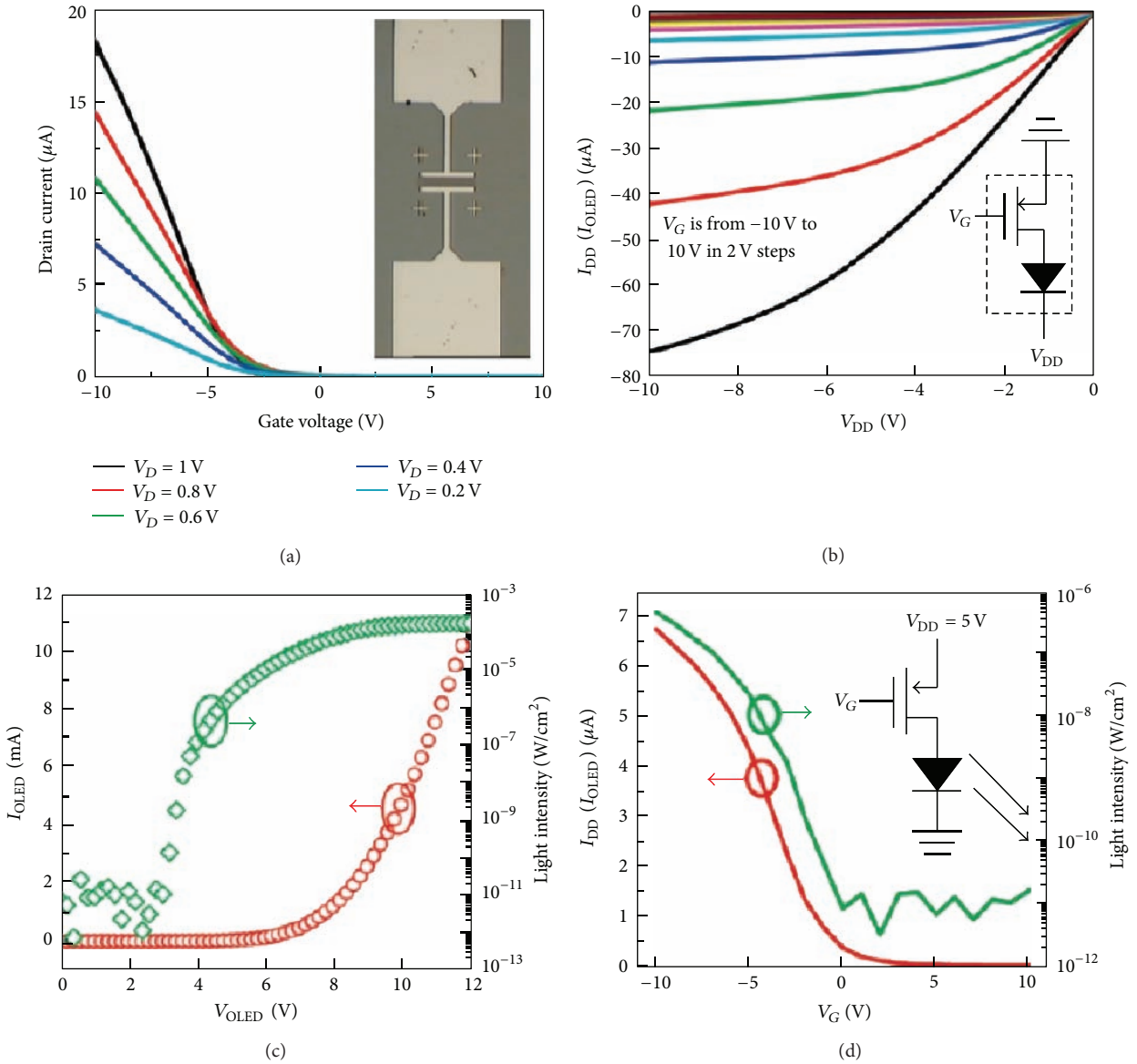


Figure 16: An OLED control circuit using SWCNT-TFTs (a) Transfer characteristics under different drain voltages for the device, Inset: optical microscope image of the device. (b) Characteristics of the OLED control circuit. (c) The OLED current and light intensity versus the OLED voltage. (d) The OLED current and light intensity versus V_G [54].

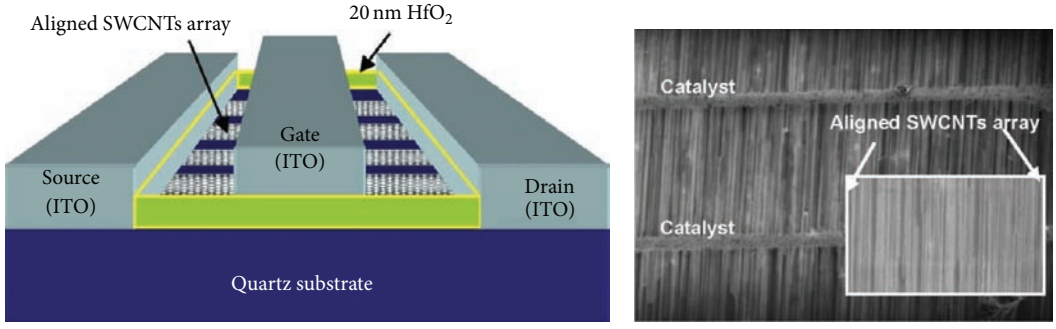


Figure 17: View of well-aligned SWCNT-TFT. (a) Schematic of the device. Aligned SWCNTs were synthesized on the quartz substrate at 900°C. Source, drain, and gate electrodes were deposited ITO at room temperature with HfO_2 gate dielectric. (b) SEM image of aligned SWCNT arrays [67].

5.3. Semiconducting CNT Purity. The coexistence of metallic and semiconducting carbon nanotubes is still an obstacle for carbon nanotube applications. Although there are some technologies to separate the two types of nanotubes, none of them can obtain absolutely 100% pure semiconducting tubes. It is expected to further improve the purification technology or to develop a better method for purer semiconducting CNT growth.

5.4. N-Type Device. The electronic properties of SWCNT are sensitive to environment [71]. Devices fabricated by SWCNTs without any special disposition exhibit typical P-type characteristics. Shim [72], Wei [73], and some other researchers have achieved N-type carbon nanotube field effect transistors with different methods. They used low work function metals [74–76], doping potassium [77], or Polyetherimide (PEI) [78], covering with polymers [72] or aluminum thin films [73] to obtain N-type devices. Devices fabricated by using low work function metals or doping potassium are still sensitive to the environment, while those fabricated by covering with aluminum thin films or polymers are relatively stable and insusceptible to the physical condition change. Only few works on N-type CNT-TFTs [79] have been done. However, the performance has much room to improve. It is worthwhile trying to fabricate N-type SWCNT-TFTs using the similar technologies as those for N-type field effect transistors.

5.5. Integration. Inverters, ring oscillators, NOR and NAND gates, and flip-flops are basic components of integrated circuits [55]. To fabricate high performance, low power and stable integrated circuits is the ultimate target for integration researchers. To fabricate stable and repeatable CNT-TFT circuit units requires researchers to put further efforts.

6. Conclusion

The paper has reviewed the state-of the-art technologies for SWCNT production and purification. Also, the fabrication technologies of SWCNT-TFTs have been discussed.

PECVD is still the most advanced technology to produce single-walled CNTs. Electrical breakdown, density gradient ultracentrifugation, and gel-based separation are the main technologies to purify the semiconducting CNTs. Filtration, dip coating, ink-jet printing, and transfer printing are the most popular used technologies to form SWCNT thin film. The SWCNT-TFTs are normally fabricated with back-silicon-gate structure on silicon substrate or TFT flat structure on flexible substrate.

Besides, the properties of SWCNT-TFTs have been analyzed and benchmarked. Compared with a-Si TFTs and poly-Si TFTs, SWCNT-TFTs show better electrical performance. Their mobility is larger than that of the a-Si by dozens of times. CNT/IZO owns even better mobility and on/off performance. SWCNT-TFTs with CNTs *in situ* grown show even better electrical performance than the CNT network TFTs do. However, they cannot be applied in the flexible substrate due to the high temperature during CNT growth.

CNT-TFTs have very wide applications including flexible display, logic or driver circuits, and photo devices. The critical issues to be solved in the future research include improving alignment, contact, and semiconducting CNT purity; realizing stable N-type SWCNT-TFTs; realizing repeatable and stable circuit blocks so as to meet the mass production requirement. Nevertheless, a bright future for SWCNT-TFTs is waiting for us to explore.

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