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Research Article

Anomalous Threshold Voltage Variability of Nitride Based Charge Storage Nonvolatile Memory Devices

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Conventional technology scaling is implemented to meet the insatiable demand of high memory density and low cost per bit of charge storage nonvolatile memory (NVM) devices. In this study, effect of technology scaling to anomalous threshold voltage (V_t) variability is investigated thoroughly on postcycled and baked nitride based charge storage NVM devices. After long annealing bake of high temperature, cell's V_t variability of each subsequent bake increases within stable V_t distribution and found exacerbate by technology scaling. Apparent activation energy of this anomalous V_t variability was derived through Arrhenius plots. Apparent activation energy (Eaa) of this anomalous V_t variability is 0.67 eV at sub-40 nm devices which is a reduction of approximately 2 times from 110 nm devices. Technology scaling clearly aggravates this anomalous V_t variability, and this poses reliability challenges to applications that demand strict V_t control, for example, reference cells that govern fundamental program, erase, and verify operations of NVM devices. Based on critical evidence, this anomalous V_t variability is attributed to lateral displacement of trapped charges in nitride storage layer. Reliability implications of this study are elucidated. Moreover, potential mitigation methods are proposed to complement technology scaling to prolong the front-runner role of nitride based charge storage NVM in semiconductor flash memory market.

1. Introduction

With the advancement of lithography techniques, conventional technology scaling that aggressively scaled down physical dimension of nonvolatile memory (NVM) devices has always been the key strategy to meet the demand for high memory density, low cost per bit, and excellent reliability charge storage NVM devices. Floating gate (FG) and nitride based charge storage NVM devices are among the front runners of NVM devices in the rapid evolution of smart consumer electronics. Figure 1 shows the typical cell structures of floating gate (FG) and nitride storage device [1]. The storage media of FG device is conductive polysilicon, and the storage media for nitride based charge storage NVM device is the low conductivity nitride layer sandwiched between oxide layers. As reported in [1], the Achilles' heel for FG devices is susceptible to point defects that may drain out all charges from conductive polysilicon layer through percolation paths formed by these point defects in tunnel oxide. Nevertheless, the discrete charge trap nature of nitride storage layer localized charges due to its inherent intrinsic defects. Evidently as reported by Honda and Cho, electrons were observed in nitride layer of ONO film, while holes were found in nitride layer and also tunnel oxide layer by using scanning nonlinear dielectric microscopy (SNDM) [2]. The trapped charges do not migrate much laterally due to the low conductivity behavior of silicon nitride that causes nitride based charge storage NVM immune to point defects that plagues FG devices [3]. During P/E cycling, both injected electrons and holes coexisted within nitride storage layer while only holes exist in tunnel oxide layer [2].

Threshold voltage (V_t) variability of post program/erase (P/E) cycled and baked are reliability challenges for nitride based charge storage NVM devices. V_t decay of nitride based charge storage NVM device has been comprehensively studied by Janai et al. [4–6]. Figure 2 shows the peak of program (PGM) V_t distribution decay of nitride based charge storage NVM cells which adhere to Stretched Exponential

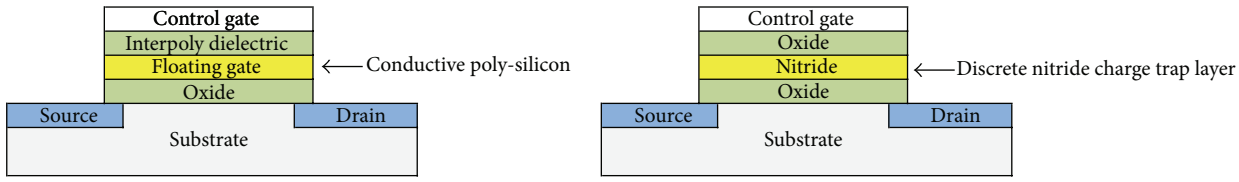

Figure 1: Typical device structure for (a) FG and (b) nitride based charge storage NVM device.

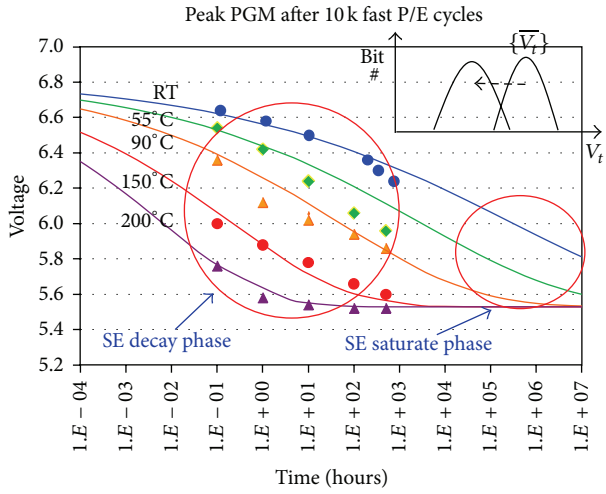

Figure 2: Typical SE decay functions fits to the peak V_t distribution decay of program nitride based charge storage NVM cells (1 Mbits) after rapidly program/erase (P/E) for 10,000 cycles and baked at various temperatures [19].

(SE) decay function [4–7]. SE decay function typically is used to elucidate the dispersive transport behavior of disordered materials [7]. The inset of Figure 2 shows the typical uniform V_t shift of all cells which is in contrast to typical shift of tail cells exhibited by FG devices due to trap assisted tunneling (TAT) [8–10].

V_t distribution broadening and shifting during SE decay phase are attributed to the contributions of two main proposed charge transport models, that is, vertical [8–12] and lateral charge transport [4–6, 13–17] and combination of both models [18]. As reported in [8–12], the decay of nitride based charge storage NVM cells' V_t distribution during SE decay phase can be elucidated through vertical detrapping of holes and electrons trapped in tunnel oxide [8–12]. On the other hand as reported in [4–6, 13–17], the broadening and shifting of nitride based charge storage NVM cells during SE decay phase can be explained through lateral redistribution of fraction of holes towards the channel which yielded annihilation of electrons localized over channel [4–6, 13–17]. As reported by Shapira et al., a unified retention model is proposed to elucidate retention loss behavior of charge trapping non-volatile memory devices through combinational contributions of lateral displacement of charges inside nitride charge storage layer and generation/annihilation of P/E cycling induced interface states [18]. However, the debate of whether vertical or lateral charge transport model or combination of both models in unified retention theory emerge as the main contributor of retention loss of nitride based charge storage NVM cells is still ongoing.

The primary focus of this study is on the V_t variability effect exhibited by nitride based charge storage NVM cell at SE steady phase, and the effect of technology scaling onto the cells' V_t variability effect at SE steady phase after high temperature preparation bake of 150°C for 500 hours was administered. At SE steady phase where V_t distribution stopped decaying and saturates, V_t of nitride based charge storage NVM cell did not stay frozen but rather exhibited anomalous fluctuation as reported in [19]. This anomalous fluctuation is attributed to lateral displacement of trapped charges in nitride storage layer that modulates the electrostatic effect onto the channel and varies the V_t level [19]. However in [19], the effect of technology scaling onto anomalous V_t variability was not further elucidated. Cell's V_t variability behavior for various technology node at SE steady phase is yet to be discovered. Therefore, the scope of this study is to analyze the effect and impact of technology scaling onto the anomalous V_t variability of nitride based charge storage NVM devices.

2. Methodology

This experiment was performed on functional samples of nitride based charge storage NVM of 110 nm, 90 nm, and 65 nm. Program/erase (P/E) mechanisms are done through Channel Hot Electron Injection (CHEI) and hot hole injection (HHI). Total 10,000 P/E cycles at room temperature were administered onto the 524,288 cells of the samples to speed up the tunnel oxide degradation process since every P/E cycle contributes to (1) generation of cycling induced defects in tunnel oxide [8–10] and (2) building up internal dipole in nitride storage layer due to the mismatch of spatial distributions of injected holes and electrons [4, 5, 13–16, 19]. After the completion of P/E cycling stress, 50% of total number of cells are kept at blank state, while 50% of total number of cells are programmed up to targeted program verify (PV) level as shown in Figure 3. Since the goal is to study the anomalous V_t variability at steady phase, these samples will be baked to 150°C for 500 hours to fully anneal all sample devices to force V_t of tested samples to saturate as shown in Figure 2. The bake duration and temperature were set based on estimation made from SE fit as shown in Figure 2 [6].

Cell's V_t measurement was carried out by measuring drain-to-source current of each cell while sweeping gate

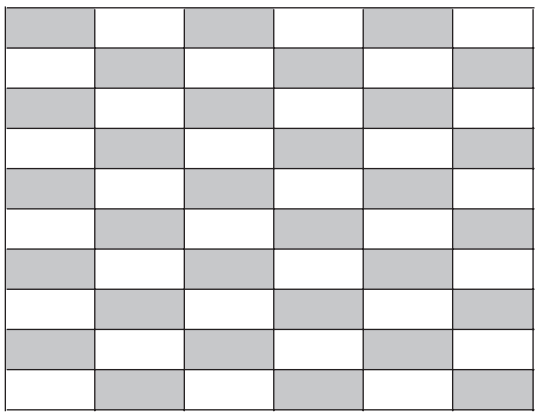

Figure 3: Typical program pattern applied to maximize the marginality of flash memory devices, for example, FG and nitride based charge storage NVM.

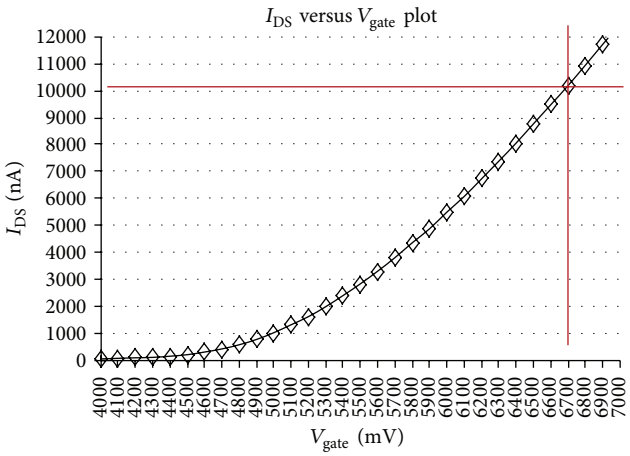

Figure 4: Interpretation of cell's V_t based on gate voltage applied on NVM cell that produces 10 μA sensing current.

voltage from 2 V to 8 V with steps of 25 mV and equalizing it to predetermined sensing current value at 10 μA. Thus, cell's V_t is equivalent to the gate voltage that produces 10 μA current as shown in Figure 4. V_t measurements of all 524,288 cells are taken after each subsequent bake of time durations 0, 0.1, 1, 10, 100 hours bake of 25°C. Then, V_t measurements of all 524,288 cells are repeated for 90, 150, 125, and 175°C to track the evolution of V_t variability of each cell after each subsequent bake. For each bake duration at each bake temperature, sigma (σ) and mean V_t shift were calculated based on V_t data collected to study the evolution of V_t variability. Apparent activation energy (Eaa) based on time to achieve equal degradation is derived for samples of each technology node. Figure 5 shows the block diagram of this experiment flow.

3. Results and Discussions

In order to study the evolution of anomalous cell's V_t variability at SE steady phase, 10,000 P/E cycles followed by

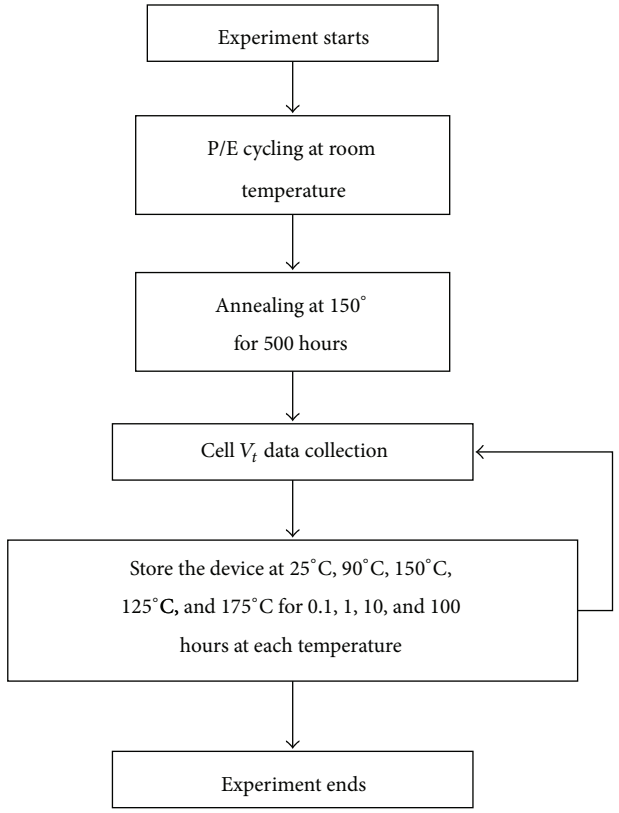

Figure 5: Block diagram of experiment flow.

high temperature annealing bake of 150°C for 500 hours are administered onto all tested functional samples of nitride based charge storage NVM devices of various technology nodes. Figure 6 exhibited cumulative normalized V_t distribution plots measured on all tested samples of all three technology nodes overlay for each bake read point. Figure 6 evidently show that V_t distribution of all three tested functional samples have reached saturation level since the peak of V_t distribution did not exhibit any significant shift for each subsequent bake administered. The high temperature annealing bake is to force the samples to reach SE steady phase by annihilating all P/E cycling induced damages. If the limitation of V_t decay depends on P/E cycling induced damages, then charge loss induced V_t shift should have halted at its native V_t level as reported in [8–11], and this was not however observed in our study. This instead indicates that vertical charge leakage through Frenkel-Poole (FP) emission followed by trap assisted tunneling (TAT) is ruled out as contributor to anomalous V_t variability at SE steady phase [8–11]. At the steady phase, V_t saturation level of 110 nm/90 nm/65 nm samples is found to be higher than their native V_t which is the baseline V_t level without any P/E history. This phenomenon corroborates with findings reported in [4–6, 13–16, 19], and the saturation level is attributed to the self-limiting characteristics of internal dipole's magnitude due to extensive P/E cycles [6].

Figure 6 confirms that V_t distribution of all tested samples is in SE steady phase. To track the evolution of V_t

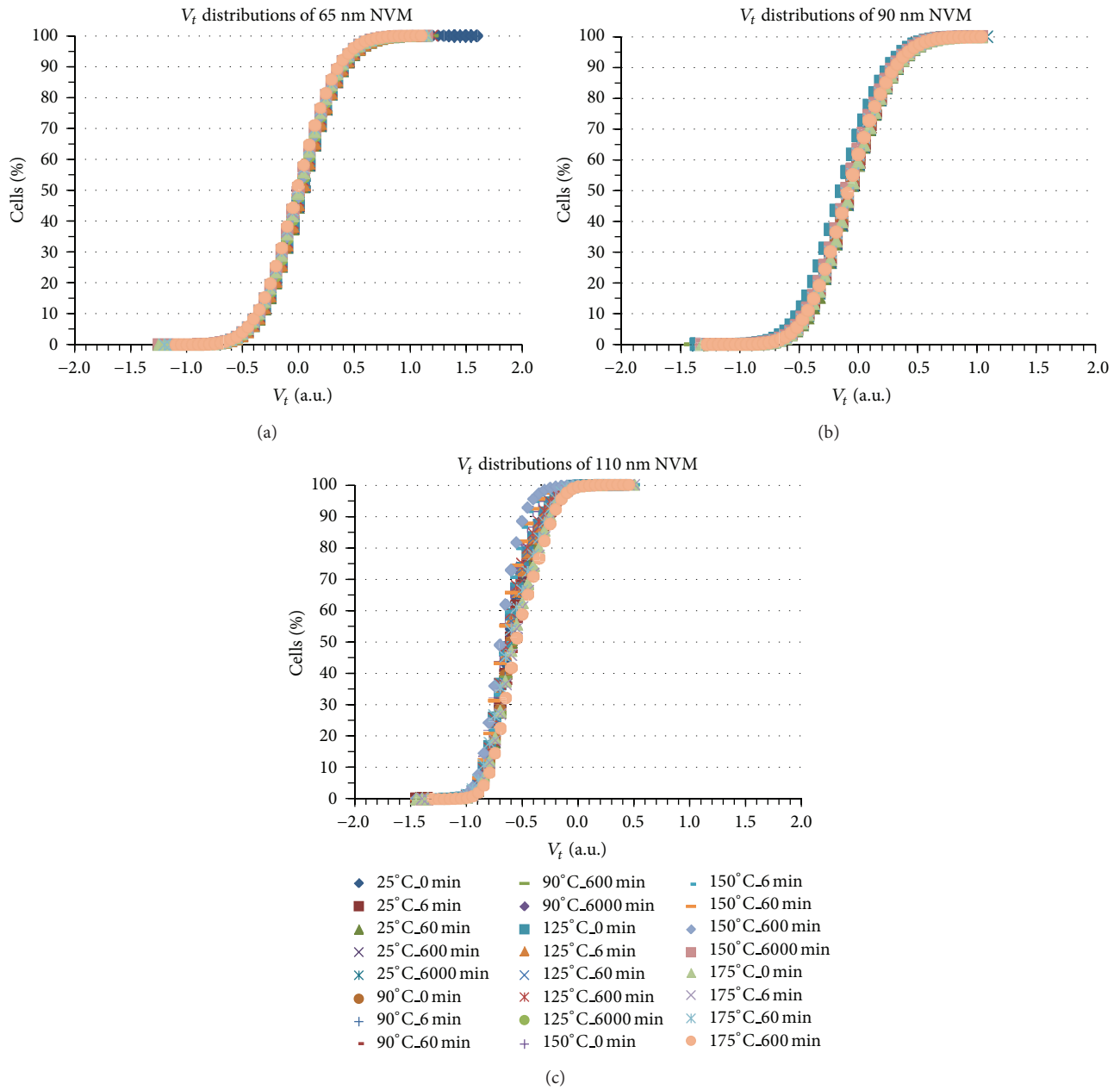

Figure 6: Cumulative V_t plots of all cells measured at each subsequent bake read point on tested good samples of (a) 65 nm, (b) 90 nm, and (c) 110 nm devices after high temperature annealing bake of 150°C for 500 hours.

variability, sigma broadening of cells with initial identical V_t level was tracked and computed for each measurement after each bake duration at each bake temperature. For all three samples of different technology nodes, sigma computed for each subgroup of cells with initial identical V_t level was found to continue to increase after each subsequent bake. This indicates that cells' V_t variability continue to increase and exhibited self-limiting effect which did not cause any significant shift of peak V_t distribution as shown in Figure 6. In other words, cell's V_t continues to vary at SE steady phase and does not lock in at a specific V_t level. This contradicts to vertical charge loss model which indicates that there is no significant V_t variability for fully annealed cell [9]. Moreover, this could well indicate that the evolution of sigma broadening of cells at peak of PGM V_t distribution is solely attributed to lateral charge loss model [4–6, 13–16, 19]. To further quantify V_t fluctuation across all three technology nodes, the evolution of sigma broadening of cells at peak of PGM V_t distribution (as shown in Figure 2) was calculated based on equation as shown in the following [19] and plotted for samples from each technology node as shown in Figure 5:

$$\Delta\sigma_{n,T}^2 = \sigma_{n,T}^2(t) - \sigma_{n,0}^2 \quad (1)$$

$\Delta\sigma_{n,T}$ is a function of time t at bake temperature T, $\sigma_{n,T}(t)$ is the calculated sigma value of cells (n) at time t, $\sigma_{n,0}$ represents

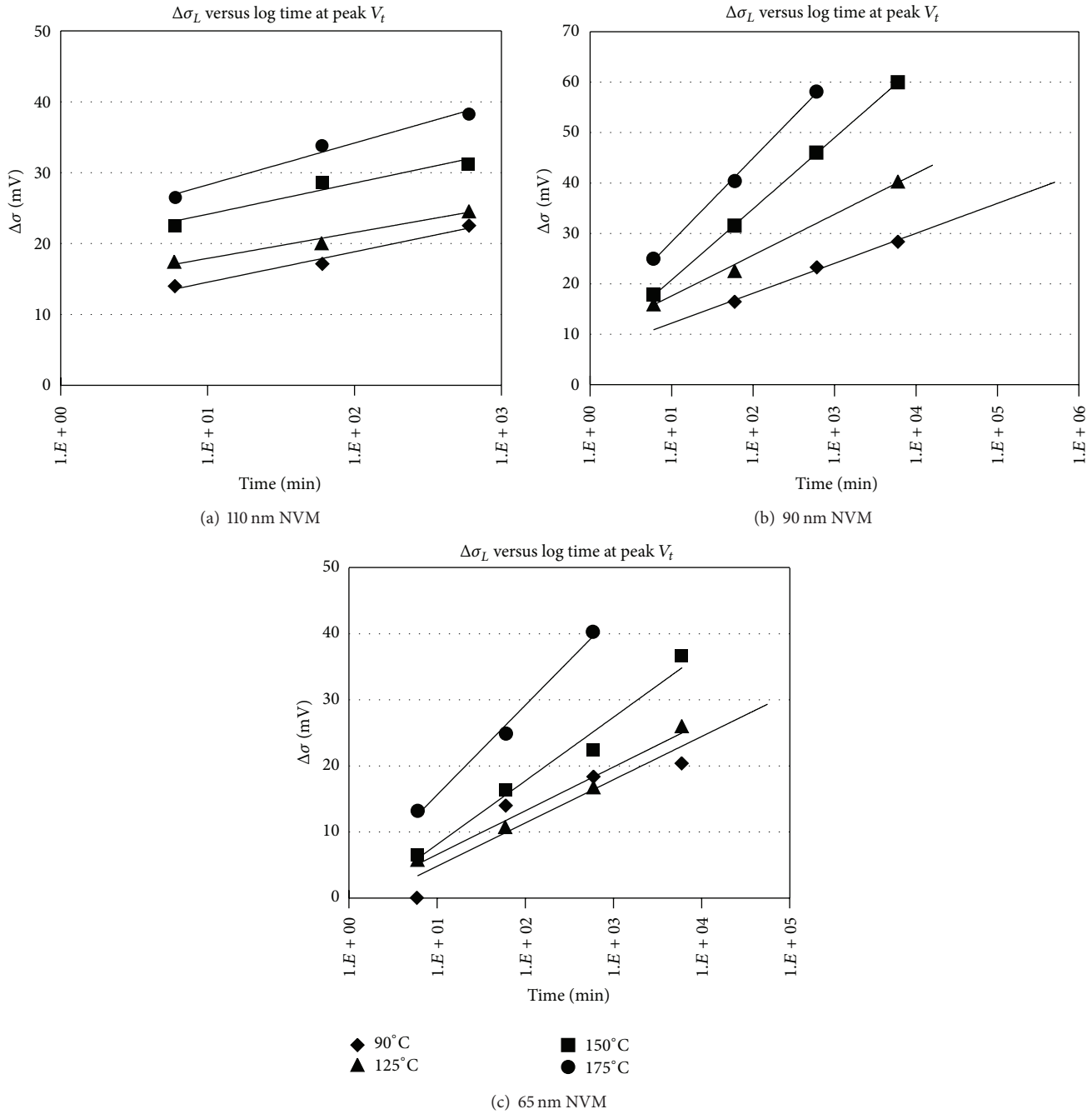

Figure 7: $\Delta\sigma$ calculated based on peak of V_t distribution for samples of each technology node, that is, (a) 110 nm, (b) 90 nm, and (c) 65 nm.

sigma at time zero which includes various temporal noises such as sensing noise and random telegraph noise (RTN) [19]. Figure 7 shows the relationship of sigma of V_t variability against time.

Based on Figure 7, time to achieve arbitrarily target $\Delta\sigma$ at 30 mV was computed for each temperature. Then, apparent activation energy of V_t variability in the form of sigma broadening is computed through Arrhenius relationship [20] as shown in Figure 8. Figure 9 exhibited the trend of Eaa of anomalous V_t variability against technology nodes of the tested samples. Larger technology node has higher Eaa as compared to lower technology node as shown in Figure 9(a). Figure 9(b) shows the smaller technology node at sub 40 nm with apparent activation energy of this anomalous V_t variability to be about 0.67 eV. Thus based on Figures 9(a) and 9(b), this clearly shows that as cell dimensions are further scaled through imminent technology scaling, number of electrons required to bring cell's V_t to target PV level reduces. Furthermore, this causes the number of tolerable electron loss to reduce correspondingly as reported by Kinam and Jungdal

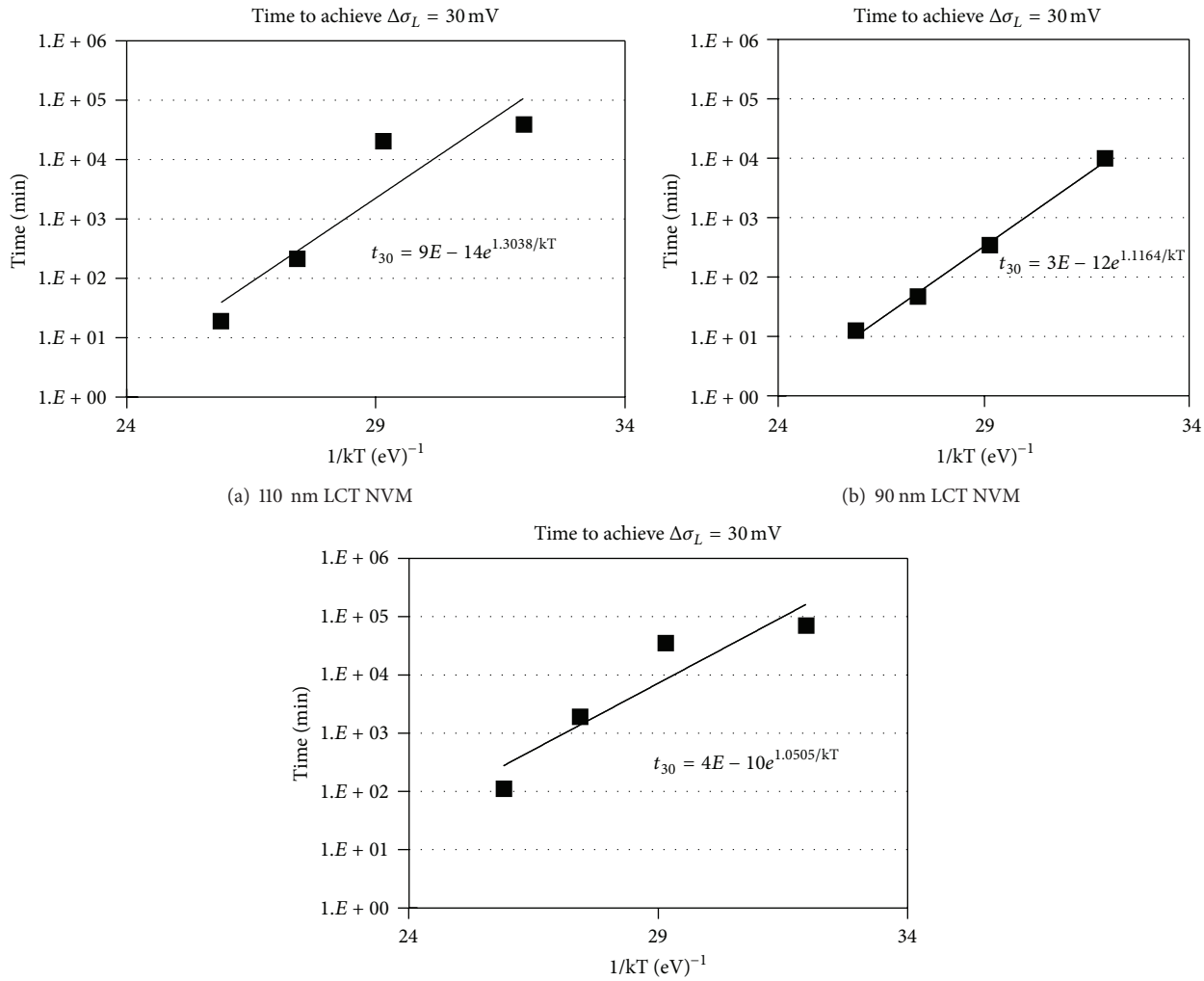

FIGURE 8: Arrhenius plots for samples of each technology node, that is, (a) 110 nm, (b) 90 nm, (c) 65 nm.

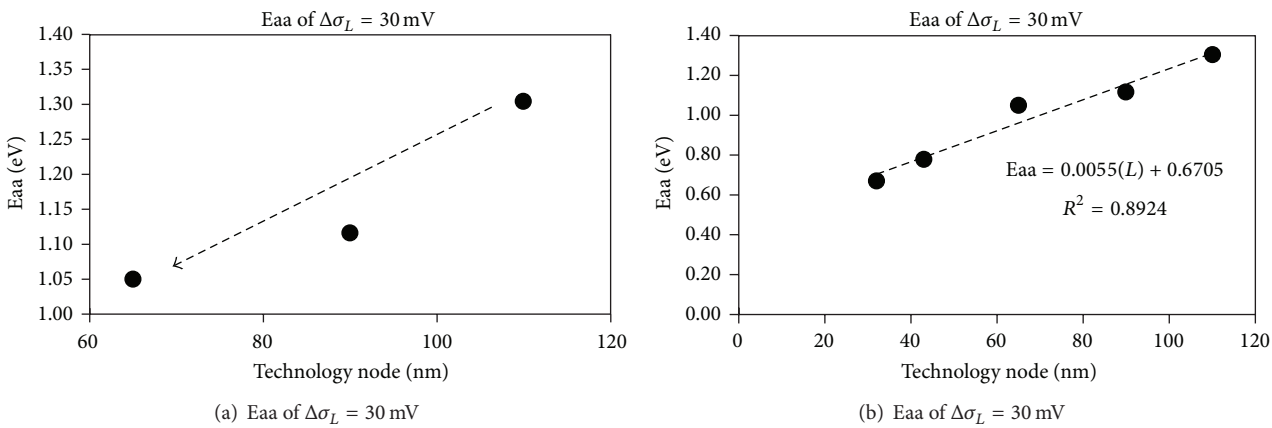

FIGURE 9: Plot of Eaa versus technology nodes of nitride storage devices tested.

[21]. Due to the reduction in number of electrons stored in nitride storage layer through technology scaling, single electron fluctuation effect becomes more prominent, and this effectively increase the V_t variability on nitride storage layer.

It is generally known that Random Telegraph Noise (RTN) in small MOSFET device is able to cause stochastic fluctuation of V_t or drain current between two distinct levels due to the capture and emission of single electron by switching oxide trap [22, 23]. Nonetheless, the results of our experiment have ruled out RTN as the primary contributor of this anomalous V_t variability at SE steady phase based on the following justifications: (1) increase in V_t distribution width was not observed as shown in Figure 6 for all technology nodes; (2) $\sigma_{n,0}$ which represents temporal noises and RTN has been subtracted, and thus, the remaining calculated sigma value is purely contributed by lateral displacement of charges in nitride storage layer [19]. Vertical charge leakage through FP emission and subsequent TAT of charges [8–11] is ruled out because cycling induced defects were annihilated through long annealing high temperature bake before the start of this experiment. Furthermore as elucidated in Figure 1, all charges were confined in nitride storage layer because it is sandwiched by high energy barrier of oxide dielectrics [16]. As shown in Figure 6 that after long annealing bake, there was no significant shift in V_t distribution of all tested samples observed, but V_t variability of each individual cell indicates that displacement of electrons still occur at SE steady phase. This is due to variability in drain current density through local electrostatic effect of stored electron location on the control of channel inversion [24]. The drain current can percolate through favorable regions of potential variability in channel [25]. Therefore based on these evidence, anomalous V_t variability observed in the form of sigma broadening is attributed to lateral displacement of trapped charges [6] instead of vertical leakage of charges through cycling induced defects [8–11] or RTN [22, 23, 26, 27]. However, this study does not rule out the possible combinational contributions of vertical [8–12] and lateral charge transport [4–6, 13–16] to retention loss of nitride based charge storage NVM cells along SE decay phase.

The reliability implications of our study indicate that anomalous V_t variability is a critical factor to consider during the design of V_t level for reference cells of nitride based charge storage NVM and for strict V_t control applications such as multilevel cell (MLC) or multibit-per-cell NVM. Anomalous V_t variability can be considered as the baseline variability that nitride based charge storage NVM must sustain to produce reliable read data output. Apparent activation energy (Eaa) of this anomalous V_t variability is close to 0.6 eV for advance technology nodes at sub-40 nm which is a reduction of nearly 2 times from 110 nm. Thus, this is a great reliability challenge for future development of nitride based charge storage NVM. Our study also shows that further technology scaling increases the significance of anomalous V_t variability. Thus, this also corroborates with the trend proposed by Kinam et al. that conventional technology scaling should be supplemented with novel approaches for future development of nitride based charge storage NVM [21, 28]. These novel approaches include (1) tunnel barrier engineering, for example, variable oxide thickness (VARIOT) [29] and tunnel oxide nitridation [30, 31]; (2) cutting-edge flash cell structure, for example, Fin-FET [32]; (3) emerging flash technologies, for example, nanocrystal memory [33] and PRAM [34].

4. Conclusions

In this study, we have successfully demonstrated that technology scaling trend of nitride storage device exacerbated anomalous V_t variability and the trend of Eaa versus technology node has shown reduction of approximately 2 times in Eaa for nitride based charge storage NVM at sub-40 nm technology node. Our findings from the series of experiments carried out indicated that the anomalous V_t variability at SE steady phase observed in this study is attributed to the lateral displacement of trapped charges in nitride storage layer instead of vertical charge leakage through tunnel oxide defects induced by extensive P/E cycling and RTN. The trend of Eaa versus technology nodes has indicated that further technology scaling will exacerbate charge retention performance of nitride based charge storage NVM which implies foreseeable reliability challenges. Anomalous V_t variability is crucial for strict V_t control applications, for example, reference cell that enables internal verify algorithm and multilevel cell (MLC) NVM. Hence, new approaches to couple with conventional technology scaling are essential to mitigate anomalous V_t variability and further improve retention performance of nitride based charge storage NVM.

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